THESIS FOR THE DEGREE OF DOCTOR OF PHILOSOPHY

Millimeter and Sub-Millimeter Wave Integrated Active Frequency Down-Converters

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Abstract

In recent years, the increasing amount of data transmission, the need for automotive radars, and standoff imaging for security applications are the main factors that accelerate research in the millimeter and sub-millimeter wave frequency ranges. The semiconductor industries have continuously developed their processes, which have opened up opportunities for manufacturing monolithically integrated circuits up to a few hundred GHz, based on transistor technologies. In this thesis, a 100 nm GaAs mHEMT technology, a 250 nm InP DHBT technology, and a 130 nm SiGe BiCMOS technology, which show a typical $f_i / f_{\text{max}}$ of 200/300 GHz, 375/650 GHz, and 250/400 GHz, respectively, are verified for analog circuit design. In the above mentioned applications, the frequency mixer is one of the most important components. Consequently, a study of millimeter/sub-millimeter wave mixers is important for the choice of technology and topology.

Aiming for either the next generation of high-speed communication or standoff imaging applications, different mixer topologies are studied, designed and fabricated as candidates for further integration in receivers. The presented mixer topologies include the self-oscillating mixer, the resistive FET mixer, the Gilbert mixer, and the transconductance mixer. All these topologies have been realized in given technologies, and cover the frequencies around ~145 GHz, ~220 GHz, and ~340 GHz. The designed 340 GHz Gilbert mixer with IF buffer amplifier and on-chip patch array antenna demonstrated the first fully integrated receiver in HBT technology at such high frequencies as well as a reasonable noise figure of 17 dB. A novel 110~170 GHz transconductance mixer is characterized in $\times 1$, $\times 2$, $\times 3$, and $\times 4$ harmonic mixing modes, which allows for flexibility in the overall system design.

Apart from the mixer designs, a transceiver, which operates as an amplifier for transmitting and simultaneously as a down-converting mixer for receiving, is designed for the frequency range of 110~170 GHz, aiming for sub-cm resolution in multipixel standoff imaging systems. It is successfully demonstrated in a FMCW radar setup for distance measurements.

Keywords: millimeter wave, sub-millimeter wave, THz, 145 GHz, 220 GHz, 340 GHz, GaAs, mHEMT, InP, DHBT, SiGe, BiCMOS, monolithic, mixer, self-oscillating mixer, resistive mixer, Gilbert mixer, transconductance mixer, harmonic, conversion gain, noise figure, transceiver, FMCW, radar.
List of Publications

Appended publications

This thesis is based on the following papers.


Other publications


Notations and Abbreviations

Notations

\( B \) Bandwidth
\( \beta \) dc current gain of bipolar transistor in common emitter configuration
\( BV_{CEO} \) Common-emitter breakdown voltage
\( c \) Speed of light
\( \varepsilon_r \) Relative permittivity
\( F \) Noise factor
\( f \) Frequency
\( f_{\max} \) Power gain cutoff frequency
\( f_t \) Current gain cutoff frequency
\( G \) Gain
\( g_m \) Transconductance
\( I_C \) Collector current
\( I_D \) Drain current
\( k \) Boltzmann’s constant
\( L \) Loss
\( P \) Power
\( T \) Temperature
\( V_{CE} \) Collector to emitter voltage
\( V_t \) Threshold voltage
Abbreviations

AM          Amplitude modulation
Au          Gold
BCB         Benzocyclobutene
CMOS        Complementary metal-oxide-semiconductor
Cu          Copper
CW          Continuous wave
dc          Direct Current
DDS         Direct digital synthesizer
DHBT        Double-heterojunction bipolar transistor
DSB-NF      Double-sideband noise figure
DUT         Device under test
EM          Electromagnetic
FET         Field effect transistor
FFT         Fast Fourier transform
FMCW        Frequency modulated continuous wave
GaAs        Gallium Arsenide
HBT         Heterojunction bipolar transistor
HEMT        High electron mobility transistor
IF          Intermediate frequency
ILD         Interlayer dielectric
IM2         Second-order intermodulation
InP         Indium phosphide
LED         Light-emitting diode
LNA         Low noise amplifier
LO          Local oscillator
mHEMT       Metamorphic high electron mobility transistor
MIM         Metal-insulator-metal
MMIC        Monolithic microwave integrated circuit
MOS         Metal-oxide-semiconductor
NF          Noise figure
PCB         Printed circuit board
RF          Radio frequency
Rx          Receiver
SHM         Sub-harmonic mixer
Si          Silicon
SiC         Silicon carbide
SiGe        Silicon germanium
SNR         Signal-to-noise ratio
SOM         Self-oscillating mixer
TEM         Transmission electron microscopy
TFR         Thin film resistor
Tx          Transmitter
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Chapter 1

Introduction and Motivation

The millimeter wave portion of the electromagnetic spectrum is defined as frequencies from 30 GHz to 300 GHz, corresponding to a range of wavelengths from 10 millimeters to 1 millimeter in vacuum. The sub-millimeter wave or terahertz (THz) is commonly defined from 300 GHz to 3 THz, with correspondent wavelengths from 1 millimeter to 0.1 millimeter in vacuum. So far, the frequencies below 100 GHz have been relatively well explored, and the research interest at higher frequencies has been boosted by many applications, in which the high-speed data transmission and THz imaging are the two main accelerators.

In data transmission fields, 1.8 zettabytes (1 zettabytes=10^{21} bytes) of data was created in the year 2011 alone. According to the International Data Corp (IDC) Digital Universe study [1], the amount of data created globally will reach 40 zettabytes by 2020, in which the unstructured information (e.g. files, emails and videos) will account for 90%. As the amount of information to be transferred increases drastically, the millimeter wave becomes very attractive as a medium for data transfer.

In imaging application fields, different ranges of the electromagnetic spectrum from acoustic waves to gamma-rays have been employed for a variety of applications. In recent years, growing terror threats have required more effective security scanning. Ever since a number of experiments showed that the THz signal has the ability to detect certain hidden substances (e.g. plastic explosives, chemical threats and biological threats) from their characteristic spectra with very low levels of non-ionizing radiation [2], increasing research activities have been and will continuously be carried out on THz imaging technologies.

For either high-speed data transmission or standoff imaging, the receiver is an essential component. Fig. 1.1 shows the block diagram of a traditional receiver front-end. The noise figure (NF) is one of the most important figure-of-merits for receivers, and the noise factor of a cascaded network can be calculated by the Friis formula [3]:

$$F_{tot} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \cdots + \frac{F_n - 1}{G_1 G_2 \cdots G_{n-1}}$$

(1.1)

where the noise factor $F$, and the power gain $G$ are in linear scale.

As can be seen from the Friis formula, the noise figure and power gain of the first stage
play a dominant role. Therefore, a low noise amplifier (LNA), which is featured by low noise and high gain, is often preferred at the first stage.

In the Friis formula, if only the noise contribution from the first two stages are taken into account, Fig. 1.2 shows the noise figure of the overall receiver chain dependence on the $NF_{LNA}$ (noise figure of the LNA), the $GLNA$ (power gain of the LNA), and the $NF_{Mixer}$ (noise figure of the mixer). Take the $NF_{tot}=10$ dB surface as an example, only if the $GLNA$ is greater than $\sim 10$ dB, the $NF_{LNA}$ is dominant. On the other hand, when the $NF_{LNA}$ is comparable to the $NF_{Mixer}$, the LNA becomes less important.

At millimeter wave range, commercial LNAs are available up to $\sim 130$ GHz with a typical gain of $10$ dB and a typical noise figure of $8$ dB [4]. At frequencies above $100$ GHz, research activities on LNAs have been carried out for years and continuous development is still ongoing at different semiconductor technologies. Fig. 1.3 shows the state-of-the-art small signal gain and the room temperature noise performance of integrated LNAs at frequencies above $100$ GHz in recent years. In Fig. 1.3 (a), the trend of reported gain is not clear, because different topologies and amplifier stages were chosen in different works.
CHAPTER 1 — INTRODUCTION AND MOTIVATION

But from Fig. 1.3 (b), it can be seen that the best noise figures reported from heterojunction bipolar transistor (HBT) technologies are around 5 dB higher than the ones from high electron mobility transistor (HEMT) technologies, and the noise figure increases proportionally with the working frequency in general.

For a receiver, it is definitely preferable to have a LNA at the first stage. However, at the time when the work presented in this thesis was done, most of them are pioneer research in given technologies and frequencies. Considering the relative high noise figure (especially for the LNAs in HBT technologies) and the design risk, such as center frequency shift, the LNA and the mixer are developed separately in the first phase. For this reason, my research is mainly millimeter and sub-millimeter wave active mixers, either stand-alone or integrated with antennas.
For situations where the LNA is omitted in a receiver front-end, Fig. 1.4 shows the noise figure dependence on the $NF_{\text{Mixer}}$ (noise figure of the mixer), the $G_{\text{Mixer}}$ (conversion gain of the mixer), and the $NF_{\text{IF,amp}}$ (noise figure of the IF amplifier). The $NF_{\text{IF,amp}}$ is normally better than 5 dB. Hence, for a moderate $NF_{\text{tot}}$ of 10 ~ 15 dB, as long as the $G_{\text{Mixer}}$ is better than $\sim$ -10 dB, the noise contribution from the mixer is dominant.

Aiming for monolithically integrated mixers at millimeter and sub-millimeter wave range, different semiconductor technologies are employed in this thesis. In Chapter 2, a 100 nm GaAs mHEMT technology, a 250 nm InP DHBT technology, and a 130 nm SiGe BiCMOS technology are presented and compared. In Chapter 3, dominant topologies of active mixers are described and corresponding designs, aiming for millimeter/sub-millimeter wave frequencies, are presented. Chapter 4 presents a 110-170 GHz frequency modulated continuous wave (FMCW) transceiver, in which the transistor operates as both an amplifier for transmitting and a fundamental mixer for receiving, intended for standoff imaging applications. Finally, the thesis is concluded in Chapter 5.
Chapter 2
Technologies

Semiconductors brought a revolutionary change to the world. The first semiconductor effect was recorded in 1833 by Michael Faraday, who observed that the electrical conduction increased with temperature in silver sulfide crystals, which was opposite to the other metals [38]. In 1874, Karl Ferdinand Braun discovered the semiconductor point-contact rectifier effect, and described the semiconductor diode for the first time [39]. In 1926, Julius Lilienfeld patented the concept of the field effect semiconductor device [40], which is called a field-effect transistor (FET) today. However, no functioning devices were constructed at that time. In 1940, Russel Ohl discovered the p-n junction in silicon [41]. Derived from Ohl’s discovery, William Shockley conceived an improved transistor, which is the junction transistor, in 1948 [42]. Due to the lack of sufficiently pure, uniform semiconductor materials, it took three more years until the first grown-junction transistor was fabricated by Gordon Teal in 1951 [43].

In 1958, Jack S. Kilby demonstrated the first all-semiconductor solid state circuit, on which both active and passive components were fabricated from semiconductor materials, and the separate elements were connected through gold wires [44]. Aiming for a more efficient way to make electronic circuits, Jean Hoerni invented the “planar” manufacturing process in 1959, thereby solving reliability problems and revolutionizing semiconductor manufacturing [45]. In the same year, Robert Noyce patented a monolithic integrated circuit concept that can be manufactured in high volume [46]. Based on Hoerni’s planar process and Noyce’s approach, Jay Last led the development of the first commercial planar integrated circuit in 1960 [47]. From then on, monolithic integrated circuits together with the semiconductor technologies began to be developed rapidly and research has drastically changed the world.

In the past half century, researchers have explored many semiconductor materials, in which silicon (Si) is the most widely used material because of its low raw material cost, high yield, and relatively high thermal conductivity. By alloying other materials with the silicon, several compound semiconductor materials emerged with different features. Silicon germanium (SiGe) is a relative new material, and it is now commonly used for high-speed heterojunction bipolar transistors. Silicon carbide (SiC) is found to be applied for light-emitting diodes (LEDs) and detectors. Investigations also show that the SiC can withstand very high temperatures and high voltages. In III-V technologies, gallium arsenide (GaAs) and indium phosphide (InP) are the two most popular materials for very
high speed devices. By far, both the GaAs-based metamorphic high electron mobility transistor (mHEMT) [13] and the InP-based high electron mobility transistors (HEMT)/heterojunction bipolar transistors (HBT) have reported state-of-the-art performance, with current gain cutoff frequency \( f_t \) and power gain cutoff frequency \( f_{\text{max}} \) approaching or exceeding 1 THz [48]-[50].

In this thesis, the presented work covers three semiconductor technologies, namely 100 nm GaAs mHEMT technology, 250 nm InP double-heterojunction bipolar transistor (DHBT) technology, and 130 nm SiGe BiCMOS technology.

### 2.1 100 nm GaAs mHEMT Technology

The HEMT based on InGaAs/InAlAs heterostructures is a well-proven device for high-frequency and low-noise applications [51]-[52]. The 100 nm GaAs mHEMT technology presented in this work is developed by the Fraunhofer Institute of Applied Solid-State Physics (FHG-IAF), Freiburg, Germany [53]. Fig. 2.1 shows a transmission electron microscopy (TEM) cross section of the metamorphic buffer with the active device on top. The high dislocation density confined to the metamorphic buffer is clearly visible, and the heterostructure is grown on a metamorphic buffer to adapt the lattice constant on GaAs wafers.

![Fig. 2.1. TEM cross section of a mHEMT. (from Fraunhofer Institute)](image)

In this process, passive elements are metal-insulator-metal (MIM) capacitors, thin film resistors (TFR), an electron beam evaporated Au-based interconnection layer and a 2.7 µm thick plated Au layer for air bridges and transmission lines. The GaAs substrate is thinned to a final thickness of 50 µm in order to suppress substrate modes for circuits operating in the G- and H-band. Fabricated transistors exhibit a maximum transconductance \( g_{\text{m,\text{max}}} \) of 140 mS/mm and a maximum drain current \( (I_{\text{D,\text{max}}} \) of 900 mA/mm. A 2x30 µm gate width 100 nm mHEMT demonstrates an \( f_t \) of 200 GHz and an \( f_{\text{max}} \) of 300 GHz.

### 2.2 250 nm InP DHBT Technology

InP HBTs are competitive for millimeter wave power amplification [50], because they
offer a high cutoff frequency with high voltage handling capacity due to the use of a wide bandgap InP collector. Furthermore, at frequencies approaching a significant fraction of the cutoff frequency, input shot noise no longer dominates over Johnson noise from the base resistance, and InP HBTs operated at 10-20% of their peak current density should have comparable noise figures to HEMTs of similar bandwidth [54].

Fig. 2.2 shows a representative cross-section of the back-end of the 250 nm InP DHBT MMIC-process, which is developed by Teledyne Technologies, Inc., Thousand Oaks, California, USA [55]. This process includes thin-film resistors (TFR), MIM capacitors, and 4-levels of interconnect (MET1-MET4). A benzocyclobutene (BCB) spin-on-dielectric (εr ~2.7) is used as the interlayer dielectric (ILD) with 1 µm ILD spacing between each metal layer. Electroplated Au-based interconnects are used for the metallization layers, where MET1-MET3 have a thickness of 1 µm and MET4 has a thickness of 3 µm. Fabricated transistors exhibit a typical dc current gain (β) of around 25 and a common-emitter breakdown voltage (BVCEO) of >4 V. A typical 4x0.25 µm² HBT demonstrates an $f_t$ of 375 GHz and an $f_{max}$ of >650 GHz, at $I_C$=9 mA and $V_{CE}$=1.8 V.

![Fig. 2.2. Cross-section of the 250 nm InP DHBT process. (from Teledyne Technologies)](image)

### 2.3 130 nm SiGe BiCMOS Technology

SiGe BiCMOS technology combines the strengths of two different transistor technologies, namely the bipolar transistor and the CMOS transistor, into a single integrated chip. The HBTs offer high speed and high gain, which are critical for high frequency analog components, whereas CMOS technology allows for low-power logic gates. This unique combination opens up the opportunity for Si-based RF system-on-a-chip solutions [56].

The 130 nm SiGe BiCMOS technology presented here is developed by Infineon Technologies [57]. The cross section of this SiGe BiCMOS process back-end is shown in Fig. 2.3. It includes npn transistors, metal-oxide-semiconductor (MOS) transistors, metal
film resistor, MIM capacitor, junction capacitor, pin diode, and 6-levels of interconnect (M1-M6). Cu-based interconnects are used for the metallization layers, with 4 thin lower layers (M1-M4) and 2 thick upper layers (M5-M6).

For RF designs, 3 types of npn transistors are available in this process. These are high speed transistors, medium speed transistors, and high voltage transistors. All types of transistors show a typical dc current gain ($\beta$) of around 1500. A single base high speed npn transistor with an emitter mask size of 0.22×2.8 $\mu$m$^2$ exhibits a common-emitter breakdown voltage ($BV_{CEO}$) of 1.4 V and demonstrates typical $f_t/f_{max}$ of 250/400 GHz. A medium speed npn transistor exhibits a $BV_{CEO}$ of 2.2 V and demonstrates a typical $f_t$ of 100 GHz. A high voltage npn transistor exhibits a $BV_{CEO}$ of 3 V and demonstrates a typical $f_t$ of 55 GHz.

Fig. 2.3. Cross-section of the 130 nm SiGe BiCMOS B11HFC process. (from Infineon Technologies)
Chapter 3

Mixer Topologies

In general, a mixer is a nonlinear electrical component that multiplies the two input signals \( f_1 \) and \( f_2 \) and generates a number of new frequencies \( f_{\text{out}} \):

\[
f_{\text{out}} = m f_1 + n f_2
\]

where \( m \) and \( n \) are integers or zero \( (0, \pm 1, \pm 2, \pm 3, \ldots) \).

For a down-converter mixer, normally the IF frequency \( f_{\text{IF}} = |f_1 - f_2| \), is the desired one, while for an up-converter mixer, \( f_{\text{RF}} = f_1 + f_2 \) is most often used.

A frequency mixer can be realized on any device with a non-linear current-voltage (I-V) characteristic. Depending on the device property, mixers are widely classified as passive mixers and active mixers. Passive mixers often use one or more diodes, e.g. point-contact diodes, PN-junction diodes, or Schottky-barrier diodes, as the non-linear device \([58]-[59]\). Since a passive mixer consumes no dc power, only conversion loss can be obtained. Nowadays, active mixers using transistors as the dominant devices may achieve conversion gain instead of conversion loss, and normally require lower local oscillator (LO) power levels than would be required for passive mixers \([60]\). In the millimeter wave and THz regimes, Schottky diodes based on waveguide technologies used to be the only solution for mixers \([61]-[63]\). As the semiconductor manufacturing technologies are continuously developing, active mixers based on transistors have already reached the THz range \([64]-[65]\).

Based on transistor technologies, a self-oscillating mixer (SOM), which avoids a bulky LO chain, may be a cost-effective solution especially at millimeter and sub-millimeter wave frequencies. The topology is studied in this thesis and a 24 GHz SOM is designed and evaluated. In FET technologies, resistive mixers have various advantages such as no dc consumption, no shot noise, high linearity, low 1/f noise \([60]\), and possibility to operate at or even above the transistor’s \( f_{\text{f} \text{max}} \) \([66]\). Therefore, in the 100 nm GaAs mHEMT technology with \( f_{\text{f} \text{max}} \) of 200/300 GHz, two resistive mixers are designed at \(~200 \) GHz. In bipolar junction transistor (BJT) technologies, both Gilbert mixers and transconductance mixers have been experimentally well-proved at frequencies below 100 GHz. In a 250 nm InP DHBT technology with \( f_{\text{f} \text{max}} \) of 375/650 GHz, both topologies are studied and designed at frequencies above 100 GHz. Pros and cons of each topologies are discussed at the end of this chapter.
3.1 Self-Oscillating Mixer (SOM)

3.1.1 Principle of SOM

The SOM operates as both a frequency mixer and an oscillator, in which the self-oscillation signal applies as the LO for the mixer. It can be a convenient solution at high frequencies where a typical bulky LO multiplication chain may be omitted [67]. Fig. 3.1 shows the schematic of one type of single-ended SOM. It is a combination of a gate mixer and a common source oscillator.

Fig. 3.1. Schematic of a single-ended SOM.

Since an oscillator is an autonomous component, to make the SOM oscillate at the desired frequency with acceptable power is of higher priority than optimizing the mixer performance. Therefore, the design priority is to have the source feedback and gate feedback optimized and make the SOM fulfill oscillation conditions at the desired frequency [68]. Then, all parts including the dc biases are tuned for optimized performance. In addition, the matching network at the gate should be designed such that the oscillation is not sensitive to the input RF signal.

3.1.2 Design and Evaluation of a 24 GHz Balanced SOM with Integrated Patch Array

The purpose of designing the 24 GHz SOM was to evaluate the circuit for later use as an up-scaled key-element for millimeter-wave standoff imaging applications. Considering the target frequency of 340 GHz, the SOM may be a convenient solution even though a deteriorated conversion gain and noise performance might be foreseen compared to a traditional mixer.

In order to gain more experimental knowledge on a SOM, the 24 GHz design is fabricated as a hybrid integrated circuit, which enables on-board trimming. Fig. 3.2 shows the schematic of the designed 24 GHz SOM. A balanced topology is chosen in order to reduce the required oscillation frequency by a factor of 2. This can be of benefit for the planned 340 GHz SOM, because the maximum oscillation frequency is limited by the $f_{\text{max}}$
of the transistor in use. In Fig. 3.2, a quarter wavelength short-circuited stub (at 24 GHz) is connected at the source to enable a dc ground path for the transistor. The resonant circuit which mainly determines the oscillating frequency incorporates the gate transmission line as an inductive element and the capacitors “C1”. Values of these components are tuned in simulations to achieve the fundamental oscillating frequency at 12 GHz. The RF port, which is inserted at the center point, does not affect the oscillation condition due to the virtual ground property at this node. Furthermore, the anti-phase condition offered by the topology will cancel the fundamental frequency (12 GHz) and all the odd harmonics at both RF and IF ports, while the even harmonics are in phase and will thus be added constructively.

The designed 24 GHz SOM is integrated with a 4×4 patch array antenna with uniform amplitude and phase feeding network. The SOM and the antenna are matched to 50 Ω and connected to each other. Fig. 3.3 shows the photo of the integrated 24 GHz down-converter. It is fabricated on standard Rogers 3003 substrate with $\varepsilon_r=3$, and occupies a board size of 75×45 mm².

The integrated SOM with the patch array is characterized as a receiver in a complete transmitter/receiver (Tx/Rx) link. A standard rectangular horn acts as the Tx antenna and is

![Fig. 3.2. Schematic of the balanced SOM.](image1)

![Fig. 3.3. Photo of the 24 GHz SOM with integrated 4×4 patch array antenna.](image2)
aligned on axis with the Rx patch array. A distance of 4 meters between the two antennas guarantees the far-field condition. In the link budget, the Tx antenna gain is from electromagnetic (EM) simulation while the patch array antenna gain is from the measurement results on the breakout antenna alone. Fig. 3.4 shows both the simulated and measured isotropic receiver gain, which incorporates the SOM’s conversion gain and the antenna’s isotropic gain. The integrated receiver (SOM+patch array) achieves a peak isotropic gain of 5.9 dB and a 3-dB-bandwidth of 800 MHz.

![Graph](image)

Fig. 3.4. Simulated and measured isotropic gain of the receiver.

### 3.2 Resistive FET Mixer

#### 3.2.1 Principle of Resistive FET Mixer

The resistive FET mixer was first proposed by Stephen A. Maas in 1987 [69]. The topology is shown in Fig. 3.5. The LO signal along with a dc bias are applied at the gate while the RF signal is applied to the drain. The IF frequency is then filtered from the drain.

Fig. 3.6 shows the typical I-V characteristics of a FET. In the linear region, the drain-to-source channel can be approximated by a variable resistor, and channel resistances can be denoted by the IV-slopes which depend on the gate voltage. Resistive FET mixers utilize exactly this property, so it can be modeled as a variable resistance which is controlled by the LO signal. For a typical resistive mixer, the gate is biased at the transistor’s threshold voltage ($V_t$) while no dc bias is applied to the drain [70]. In one LO cycle, the channel resistance increases to virtually infinity ($R_{off}$) when the gate voltage drops below $V_t$, and it decreases to a very low value ($R_{on}$) when the gate voltage reaches its maximum.
3.2.2 Design and Evaluation of Two 200 GHz Resistive Mixers with Integrated Double-Slot Antenna

The frequency band around 220 GHz, as one of the atmosphere windows, is potentially interesting for both high-speed wireless communication and high-resolution imaging applications. In the past decade, continuous development of semiconductor manufacturing technologies has opened up opportunities for monolithic integrated circuits at such high frequencies.

The 100-nm mHEMT technology, which has been described in section 2.1, shows typical \( f_l / f_{\text{max}} \) of 200/300 GHz. Therefore, circuits at around 220 GHz are theoretically realizable. Based on such a technology, a single-ended resistive mixer and a single-balanced resistive mixer with integrated double-slot antenna are designed at \( \sim 200 \) GHz. Fig. 3.7 shows the schematics of the two mixers. In both topologies, the LO is connected to the gate in order to vary the channel resistance, and a single-section coupled line filter is inserted at the RF port to suppress LO-to-RF leakage. In the single-balanced topology, the LO signals at the two gates show a 180° phase difference due to the half wavelength stub. Therefore, the LO leakage at the combined RF port can be cancelled.
In the given process with two metal layers (including the ground layer at the backside), the double-slot antenna is chosen to be integrated on-chip, because at millimeter-wave frequencies, its radiation can be coupled to a focusing ellipsoidal lens [71]-[72]. With the help of the focusing lens, a narrow beam with a directivity of ~24.5 dBi is obtained in simulation.

Fig. 3.8 shows the chip photos of both integrated receivers. Two slots are etched out on the backside metal layer (marked by the black dashed rectangles) while the microstrip feed network is located on the top metal layer for integration with resistive mixers. The RF ports of both mixers and the antenna ports are matched to 50 Ω to be able to connect directly. The two integrated receivers occupy chip areas of 1100×700 µm² and 900×950 µm², respectively.

An attempt was initially made to measure the two integrated receivers by using the Y-factor method, where a big piece of absorbing foam at room temperature (295 K) is seen by the receiver antenna as the hot load, and a box of absorbing foam at liquid nitrogen (77 K) serves as the cold load. A similar measurement setup is presented in [73]. Theoretically, both conversion gain and noise figure can be obtained from the Y-factor method. However, the measured Y-factors of the two designed receivers are too small to be read accurately.
As can be seen from Fig. 3.9, the Y-factor tends to be lower than 0.5 dB when the noise figure is higher than 7.5 dB.

In order to evaluate the two integrated receivers in a more reliable way, a complete Tx/Rx link at G-band (140-220 GHz) has been built. Fig. 3.10 shows a photo of the measurement setup. In a wafer-probe measurement, the pads on the chip can only be probed from the top direction, so the beam from the on-chip double-slot antenna radiates downwards. A 30 cm high metallic table is specially designed and fabricated for this measurement to offer the possibility to mount probe manipulators from three directions. The receiver to be tested is glued onto a Si lens, which is mounted at the center opening on top of the metallic table, and a G-band corrugated horn antenna together with an in-house manufactured ×6 frequency multiplier source module (output frequency band: 163-202 GHz) are located 200 mm beneath it. The Tx/Rx antennas should be aligned in axis with the same polarization.

With +5 dBm LO power applied, the measured receiver gain (\(G_{RX}\)) and conversion loss of the mixers (\(L_c\)) are shown in Fig. 3.11 and Fig. 3.12, respectively. Here the receiver

![Fig. 3.9](image_url)  
*Fig. 3.9. The Y-factor as a function of the noise figure when \(T_{hot} = 290 \text{ K}\) and \(T_{cold} = 77 \text{ K}\).*

![Fig. 3.10](image_url)  
*Fig. 3.10. Photo of the measurement setup.*
gain incorporates the antenna gain referred to an isotropic antenna and the conversion loss of the mixer. Therefore, in the RF frequency range of 185–202 GHz or the IF frequency range of 1~18 GHz, a typical $L_c$ of 8.0 dB and $G_{RX}$ of 15.4 dB are measured for the single-ended topology, while a typical $L_c$ of 12.2 dB and $G_{RX}$ of 11.2 dB are obtained from one of the two IF outputs for the single-balanced one.

In this work, the noise figures of the two integrated receivers are estimated by a proposed novel method, which is called the signal generator N-times power method. The working principle of the proposed method is presented in the Appendix. The measured noise figure of the two receivers is around 1 dB higher than the conversion loss of mixers alone.

![Conversion loss and estimated gain graphs](image)

**Fig. 3.11.** Conversion loss of the single-ended resistive mixer and estimated gain of the integrated receiver (a) fixed LO at 209 GHz (b) fixed IF at 1 GHz.

![Conversion loss and estimated gain graphs](image)

**Fig. 3.12.** Conversion loss of the single-balanced resistive mixer and estimated gain of the integrated receiver (a) fixed LO at 184 GHz (b) fixed IF at 1 GHz.
3.3 Gilbert Mixer

3.3.1 Principle of Gilbert Mixer

In bipolar transistor technologies, the Gilbert-cell mixer is popular for its excellent properties, such as relative high conversion gain, broad operating bandwidth, relative low LO driving power, and good port-to-port isolation [74]. Fig. 3.13 shows the topology of a basic bipolar Gilbert-cell mixer. It is double-balanced and has all the properties of a double-balanced mixer. The upper four LO transistors are driven by a strong LO signal and operate as switches which are turned alternately on and off over the LO cycle. The lower two RF transistors are biased at the forward active region and operate like a differential amplifier. Ideally, the emitters of the LO transistors are virtual ground for the LO, so there will be no LO voltage on the collectors of the RF transistors. Similarly, the collectors of the LO transistors are also virtual ground for the LO, so the LO-to-IF isolation is usually good (e.g. can be around 50~60 dB at frequencies below 1 GHz [74]).

![Fig. 3.13. Basic bipolar Gilbert-cell mixer.](image)

3.3.2 Topologies of Sub-Harmonic Gilbert Mixer

As the operating frequency increases into millimeter/sub-millimeter wave frequency ranges, generation of sufficient high LO power is a challenging task. Therefore, the sub-harmonic mixer (SHM) is especially interesting because the LO frequency is only half of the frequency needed for a fundamentally pumped type.
The most popular topologies for sub-harmonic Gilbert mixers are the stacked-LO configuration and the leveled-LO configuration. Fig. 3.14 (a) shows the simplified topology of the stacked-LO sub-harmonic Gilbert mixer. It is composed of two upper LO stages of a double-balanced switching cell and a lower RF stage of a differential pair. When the switching phases are offset by 90°, the two stages of double-balanced switching cell will double the LO frequency effectively [75]. Fig. 3.14 (b) shows the simplified topology of the leveled-LO sub-harmonic Gilbert mixer. It consists of four cross-connected transistor pairs at the upper LO level and one transistor pair at the lower RF level. The LO is applied in quadrature at around half of the RF frequency. By feeding the LO signals with a large enough amplitude, the upper transistors work as a mixer by commutating the RF current at twice the LO input frequency [76].

Both topologies have been investigated and compared in [77]. The stacked-LO configuration requires a smaller LO pumping power at the expense of a greater supply voltage and degraded noise performance. Since the upper LO level transistors are stacked in a cascode type, the $2f_\text{LO}$ to the RF port leakage is suppressed. Therefore, the stacked-LO structure is claimed to be the best topology to achieve the highest 2LO-to-RF isolation. In a leveled-LO sub-harmonic Gilbert mixer, the mixing operation is based on the transistor’s nonlinearity, so it can potentially operate at higher frequency but requires larger LO pumping power.

### 3.3.3 Design and Evaluation of a 340 GHz Receiver Front-End with Integrated 2×2 Patch Array

As is mentioned in Chapter 1, THz frequencies are especially interesting for standoff imaging applications due to their unique properties. However, a combined effect from absorptions, distortions, attenuation and the relative weakness of spectral features in the reflection makes the THz spectra difficult to use in practical applications [78]. At the expense of reduced spatial resolution or increased optical system size, the lower end of the
THz frequency range (e.g. frequency band at ~340 GHz) seems more promising for standoff imaging applications [78]-[79].

In Teledyne’s 250 nm InP DHBT process, which shows an $f_i$ of 375 GHz and an $f_{\text{max}}$ of >650 GHz, circuits and even integrated system (e.g. fully integrated transmitters and receivers) at ~340 GHz frequency band can be realized. Therefore, a 340 GHz integrated receiver, which consists of a sub-harmonic Gilbert mixer, an IF differential amplifier, and a 2×2 patch array, is designed and fabricated in this technology.

Fig. 3.15 shows the schematic of the integrated 340 GHz Gilbert mixer and differential IF buffer amplifier. The leveled-LO sub-harmonic Gilbert mixer topology is adopted due to its higher operating frequency, as is discussed in the previous section. The smallest available transistor (0.25×3 µm$^2$) is chosen for both the upper LO level and lower RF level. The quadrature-phase LO is generated by a simple combination of a Marchand balun [80] followed by two branch-line hybrids [81]. The differential IF buffer amplifier consists of three transistor stages, in which the second stage is the core for power amplification and the first and third stages improve the matching.

In order to achieve a compact integration, a differential patch antenna is designed to

---

Fig. 3.15. Schematic of the integrated 340 GHz subharmonic Gilbert and differential IF buffer amplifier.

Fig. 3.16. Block diagram of the integrated receiver.
feed out-of-phase RF signals into the mixer. Therefore, no additional RF balun is needed. Fig. 3.16 shows the block diagram of the 340 GHz integrated receiver, and the chip photo is shown in Fig. 3.17. The single-ended LO port, differential IF ports, and dc bias ports are designed with on-wafer pads. The whole chip occupies an area of 1680×1840 µm² and consumes 472 mW dc power out of which 55 mW is consumed by the mixer.

Similar to before, a complete Tx/Rx link is set up to characterize the designed receiver front-end. Fig. 3.18 shows the photo of the measurement setup. The receiver chip is glued onto a small piece of brass block and further mounted at the opening of a big piece of aluminum board, which has been attached on an optical table. Probe manipulators with a magnet underneath are mounted on the same optical table to enable the on-wafer probing. A WR-03 conical horn is connected with the built transmitter chain to illuminate the on-chip antenna with RF signals. The alignment of the two antennas is obtained by the fine-tuning x-y scanner which is mounted on the top plate.

In this work, $G_{RX}$ is defined as the receiver gain, which incorporates the conversion

![Fig. 3.17. Chip photo of the integrated receiver (Size: 1680×1840 µm²)](image1)

![Fig. 3.18. Photo of the measurement setup.](image2)
gain of the mixer, the gain from IF buffer amplifier and the antenna gain referred to an isotropic antenna, and $G_{c,circuit}$ is defined as the conversion gain of the down-converter circuit, where the on-chip antenna gain ($G_i$) is excluded from $G_{RX}$. Limited by the measurement setup, the RF signal can only sweep up to 338 GHz. Therefore, double sideband performance at 160 GHz LO and the lower sideband performance at 170 GHz LO, with a maximum available LO power of ~4 dBm on-chip applied, are characterized by measuring the output power from one of the IF ports. Fig. 3.19 shows the measured results. A peak $G_{RX}$ of ~12 dB and a peak $G_{c,circuit}$ of ~14 dB are obtained at 170 GHz LO and 338 GHz RF. The gain slope is mainly due to the limited bandwidth of the IF buffer amplifier.

The double-sideband noise figure (DSB-NF) of the receiver is calculated from the direct noise measurement method [82]. A typical noise figure of 17 dB is obtained.

Fig. 3.19. Measured conversion gain (from single IF output port) of the down-converter circuit and the conversion gain of the receiver at (a) $f_{LO}=160$ GHz, and (b) $f_{LO}=170$ GHz.

3.4 Transconductance Mixer

3.4.1 Principle of Transconductance Mixer

In a transconductance mixer, the transistor is biased to provide transconductance, and possibly amplification for the RF and LO signals applied to the input base or gate terminal of the transistor [83]. Fig. 3.20 shows a simplified schematic of a single-ended transconductance mixer. The transistor is biased around the turn-on voltage, similar to that of a class-B amplifier, with the transfer characteristic shown in Fig. 3.21. As the LO input drives the base, the transistor switches on along the load line during the positive voltage swings. Thus the transconductance waveform will have the same frequency as the LO. Therefore, $g_m(t)$ can be written as
As the small-signal RF voltage is applied to the base, the collector current will be

\[ i(t) = g_m(t) \cdot v_{RF}(t) = g_0 V_{RF} \cos(\omega_{LO}t) + \frac{g_1}{2} V_{RF} \left[ \cos(\omega_{RF} - \omega_{LO})t + \cos(\omega_{RF} + \omega_{LO})t \right] + \cdots \] (3.3)

Then the IF signal, which is represented by \( \frac{g_1}{2} V_{RF} \cos(\omega_{RF} - \omega_{LO})t \), can be selected by an output IF filter.

For optimal conversion gain, the base-emitter junction of a fundamentally pumped
transconductance mixer is biased around the turn-on voltage, where a 50% duty-cycle of the transconductance waveform is obtained. For an arbitrary harmonic mixer, the optimal duty-cycle of the transconductance waveform is 1/2n, where the integer number n is equal to the order of harmonic that is used for mixing. In reality, the duty-cycle of the transconductance waveform can be controlled by varying dc bias at the base-emitter junction. More details of this design rule can be found in paper [D].

3.4.2 Design and Evaluation of a 110-170 GHz Multi-Mode Transconductance Mixer

At the atmospheric window around 145 GHz, a relatively broad frequency band (141~148.5 GHz) has recently been allocated for fixed and mobile communication [84]. As several semiconductor manufacturing technologies have achieved over 500 GHz or even 1 THz $f_t/f_{max}$, it is feasible to design circuits in the ~145 GHz frequency band. In the Teledyne 250 nm InP DHBT technology, a typical $4\times0.25 \mu m^2$ HBT demonstrates an $f_t$ of 375 GHz and an $f_{max}$ of >650 GHz. From the receiver point of view, key components (LNAs and mixers) with relative high performance should be realizable in such a technology. In many wireless communication systems, dc power consumption is also important. For a traditional receiver architecture, the LO chain often consumes a large portion of the dc power. As the operation frequency increases into the millimeter wave range, the LO chain becomes more bulky. By using a harmonic ($\times2$, $\times3$, $\times4\ldots$) mixer, the LO-generation is simplified at the expense of mixer performance. In the given 250 nm InP DHBT technology, a 145 GHz well-performed LNA can be expected to compensate the mixer noise, and the conversion gain of the mixer can be easily increased by adding an IF amplifier. Therefore, a transconductance mixer, which can be pumped at multiple LO harmonic mixing modes, is designed and characterized for the next generation of high-speed communication.

The schematic is shown in Fig. 3.22. A single-balanced topology is used in order to suppress the second-order intermodulation (IM2). The two identical branches are fed with in-phase LO and differential RF signals. The two IF outputs are out-of-phase and can be combined by an off-chip balun. Looking into either one of the two identical branches, transistors Q1 and Q2 are biased in class-A condition and work together as a broadband active power combiner for RF and LO signals. The transistor Q3 is the transconductance mixer transistor. Its base-emitter junction is biased depending on the order of harmonic mixing mode. A large transistor ($0.25 \mu m\times10 \mu m\times2$ finger) is chosen for Q4 while it is biased under class-A condition, to make sure that the linearity of the overall mixer will not be deteriorated. The chip photo is shown in Fig. 3.23, and it occupies an area of 1100×750 $\mu m^2$.

Table 3.1 lists the base bias of the mixer transistor ($V_{b2}$ in Fig. 3.22) at different harmonic mixing modes. With the $\times1$, and $\times2$ mixing modes, instability was observed in the measurement. To stabilize the circuit, the base bias $V_{b2}$ at the mixing transistor is decreased compared to the ones in the simulation.
Table 3.1.  

<table>
<thead>
<tr>
<th></th>
<th>×1</th>
<th>×2</th>
<th>×3</th>
<th>×4</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{b2_sim}$ (V)</td>
<td>0.7</td>
<td>0.6</td>
<td>0.32</td>
<td>0.32</td>
</tr>
<tr>
<td>$V_{b2_meas}$ (V)</td>
<td>0.5</td>
<td>0.45</td>
<td>0.32</td>
<td>0.32</td>
</tr>
</tbody>
</table>

Fig. 3.22. Schematic of the single-balanced D-band mixer.

Fig. 3.23. Chip photo of the transconductance mixer. (Size: 1100×750 µm²)
At an IF frequency of 2 GHz, the conversion gain and noise figure are measured versus RF frequencies, as is shown in Fig. 3.24. For ×1 and ×2 mixing modes, the discrepancy between the simulation and measurement is due to the base bias reduction (as is shown in Table 3.1) and the collector current deviation through the Q4 in Fig. 3.22.

3.5 Discussion

In this chapter, four frequency converter topologies are described. Aiming for either high-speed communication or standoff imaging applications, all four topologies are designed and characterized.

Based on the presented works and literature study, the electrical performances of the four mixer topologies are compared in Table 3.2. In general, a self-oscillating mixer is cost effective in terms of compact size (considering the LO is applied by itself) and relative low dc power consumption [85]-[87]. However, since the dc bias is compromised between an optimized oscillator and an optimized mixer, the other electrical performances (e.g. conversion gain and noise figure) cannot compete with the other traditional mixer topologies.

Resistive mixers use the channel-resistance of FETs to achieve frequency conversion and typically show better linearity than an active mixer. Since the drain is not biased, a resistive mixer consumes virtually zero dc power. However, it normally requires a high LO power to work efficiently. For a single-ended resistive mixer, the LO-to-RF isolation is poor (e.g. 9.3 dB isolation was obtained from the single-ended mixer [88]). However, this can be solved by using a balanced topology in which the LO leakage can be suppressed.
intrinsically because the LO signals at the two gates are 180° out-of-phase. By comparing the presented resistive mixers, the LO-to-RF isolation from the single-balanced topology is improved by 30 dB compared to the single-ended one. However, since two transistors are working for frequency conversion in a single-balanced mixer, higher LO power would be needed.

Gilbert mixers have been very successful since they were invented, and are more suitable in BJT technologies than in FET technologies. Since the Gilbert mixer is doubly balanced, it has delightful properties such as isolation between all three ports, LO AM noise suppression, and rejection of all spurious responses with odd LO harmonics (for sub-harmonic mixer). Typically, Gilbert mixers can achieve a moderate to high conversion gain but relatively poor linearity. As the working frequency increases, a Gilbert cell can be modified, e.g. the stacked-LO configuration and the leveled-LO configuration, to operate as a sub-harmonically pumped mixer.

Transconductance mixers, which utilize the time varying transconductance of BJTs, feature a simple topology compared to a Gilbert mixer. It is feasible to be pumped in an arbitrary harmonic mixing mode without changing the topology. Since the noise of a mixer consists of the internal noise generated by the mixer device itself and the noise converted from all the harmonics’ ports, by increasing the order of the harmonic mixing mode, the local oscillator (LO) frequency can be decreased at the expense of the higher noise figure.

Table 3.2.
COMPARISON OF MIXER TOPOLOGIES

<table>
<thead>
<tr>
<th></th>
<th>SOM</th>
<th>Resistive mixer</th>
<th>Gilbert mixer</th>
<th>Transconductance mixer</th>
</tr>
</thead>
<tbody>
<tr>
<td>dc power consumption</td>
<td>Low</td>
<td>0</td>
<td>High</td>
<td>Moderate</td>
</tr>
<tr>
<td>Conversion gain</td>
<td>Low</td>
<td>Low</td>
<td>Moderate~High</td>
<td>Moderate~High</td>
</tr>
<tr>
<td>Noise figure</td>
<td>Poor</td>
<td>Moderate</td>
<td>Moderate</td>
<td>Moderate~Good</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>Poor</td>
<td>Good</td>
<td>Moderate~Good</td>
<td>Moderate~Good</td>
</tr>
<tr>
<td>Linearity</td>
<td>Poor</td>
<td>Good</td>
<td>Moderate</td>
<td>Moderate</td>
</tr>
<tr>
<td>LO power</td>
<td>0</td>
<td>High</td>
<td>Low~Moderate</td>
<td>Low~Moderate</td>
</tr>
<tr>
<td>Port isolation</td>
<td>Poor~Moderate</td>
<td>Poor (single-ended) Good (balanced)</td>
<td>Good</td>
<td>Poor (single-ended) Good (balanced)</td>
</tr>
<tr>
<td>Design complexity</td>
<td>Moderate</td>
<td>Low</td>
<td>High</td>
<td>Low~Moderate</td>
</tr>
</tbody>
</table>
Chapter 4

A 110-170 GHz Transceiver for FMCW Applications

The frequency modulated continuous wave (FMCW) radar is widely used in applications such as automotive anti-collision, maritime navigation, aircraft navigation, etc. In this chapter, the principle of a basic FMCW radar is introduced. Aiming at a standoff imaging array with a sub-cm range resolution, a 110-170 GHz transceiver is presented for FMCW applications.

4.1 Principle of FMCW Radar for Range Measurement

The FMCW radar is a special type of continuous wave (CW) radar [89]. Aiming for measuring range and velocity, the transmitted signal is modulated in frequency, and the modulation can be different, e.g., triangle wave, sawtooth wave, sine wave, and square wave. The most common method is to modulate the frequency of a continuous wave in a linear manner. As is shown in Fig. 4.1 (a), the transmitted signal is shown by the solid triangular waveform, with a modulation rate of \( f_m \) and a frequency sweeping bandwidth of \( B_{\text{sweep}} \). The dashed waveform represents the received echo signal from a stationary target. When the transmitted signal is taken as a reference, the time when the echo signal arrives back at the radar can be represented by:

\[
t_b = \frac{2R}{c} \tag{4.1}
\]

where
- \( R \) represents the range to the target;
- \( c \) is the speed of light.

When the received echo signal is mixed with the transmitted one, a beat frequency \( f_b \) is generated, as is shown in Fig. 4.1 (b). From the geometry of Fig. 4.1 (a), \( f_b \) can be expressed as:
4.2 Design of a 110-170 GHz Transceiver for FMCW Applications

In a conventional FMCW radar front-end, the receiver path and transmitter path are separated all the way through the antenna [90]-[95], or share one antenna by introducing either a circulator [96]-[97] or a hybrid [98]-[99]. For reasons of simplicity and low dc power consumption, an FMCW radar transceiver, which operates as both transmitter and receiver, was demonstrated in [100]. Then, in the microstrip technology, a single-ended transceiver, which uses only one transistor and several passive components, is published for ~10 GHz FMCW radar applications [101], and followed by a balanced version with improved AM noise suppression [102].

For standoff imaging applications, Jet Propulsion Laboratory (JPL) has developed three generations of FMCW imaging radars at frequencies above 500 GHz [93]-[95]. In order to separate the transmitted and received signal in their radars, a beam splitter is used, however, this introduces a round-trip loss of at least 6 dB. In order to overcome the 6 dB additional loss from the beam splitter and again simplify the Tx/Rx chains, an integrated FMCW radar transceiver module, which uses GaAs Schottky diode technology and has the transmitter and receiver as a single unit, is demonstrated at 200-240 GHz [103]. In reality, a single transceiver is not enough to provide the necessary frame rate for real-time standoff imaging, so an array of transceivers is needed. Therefore, making an array in monolithically integrated circuit technologies is more efficient in terms of space and cost.
compared to stacked single transceivers in waveguide technologies.

To allow future production in high volume, a balanced 110-170 GHz transceiver is designed, utilizing a SiGe BiCMOS technology. Fig. 4.2 shows the schematic of the transceiver. The transistors are biased under class-AB condition. Therefore, they operate as amplifiers for transmitting and simultaneously as fundamentally pumped down-converter mixers for receiving. When the circuit works as a receiver, the input signal serves as the LO and the returned signal back into the output port serves as the RF. The two branches are fed through a 90° hybrid and further combined by a second 90° hybrid. Thus the transmitted signals from the two branches are in-phase at the output. At the differential IF ports, a commercial transformer is connected to obtain a single-ended output, and its center tap is used to apply collector dc bias. The chip photo of the transceiver is shown in Fig. 4.3, with a size of 980×560 µm².

Fig. 4.2. Schematic of the balanced transceiver.

Fig. 4.3. Chip photo of the transceiver (chip size: 980×560 µm²).
4.3 Experimental Results

The designed transceiver is characterized by on-wafer probed measurements on circuit level, and in addition also demonstrated as a FMCW radar for distance measurement.

4.3.1 Circuit Measurement

The transceiver is characterized as an amplifier and as a down-converter mixer. After terminating the IF port by a 50 \( \Omega \) matched load, the two-port small signal S-parameter is measured, as shown in Fig. 4.4 (a). Since the transistors are not biased for an optimal amplifier, very little power gain is achieved from simulation while a \(~4\) dB lower value is obtained in the measurement. However, in our applications, the maximum output power is more crucial for a transmitter. It is observed from measurements that more than 0 dBm output power can be obtained when an input power of +3 dBm is applied. Under the same bias condition as a transmitter, the circuit is also measured as a receiving down-converting mixer. With an LO power of approximately 3 dBm, the measured conversion gain is shown in Fig. 4.4 (b). The IF frequency is limited to 300 MHz by the off-chip transformer. With an LO frequency of 130 GHz, a typical conversion gain of -9 dB is obtained. The noise performance of the mixer is evaluated by measuring the IF noise power. A noise figure of 19 dB is achieved with an LO frequency of 130 GHz.

Fig. 4.4. (a) The measured (solid line) and the simulated (dashed line) two-port small signal S-parameter for transmitter. (b) Simulated and measured conversion gain as a function of the IF frequency \((f_{LO}=130\) GHz). 

4.3.2 FMCW Radar Measurement

The transceiver is also demonstrated for distance measurement. The FMCW radar measurement setup is shown in Fig. 4.5.
To demonstrate the capability of measuring distance, a piece of wood is placed in front of the antenna, as is shown in Fig. 4.6 (a). Fig. 4.6 (b) shows the IF spectrum when placing the target at different distances from the radar transceiver, and the second x-axis shows the corresponding distance according to the IF frequency.

With the aim of demonstrating the range resolution, cardboard boxes with different thicknesses are chosen as the targets. Therefore, the two cardboard layers from one box should be recognized as two targets in the wave propagation direction. Fig. 4.7 shows the IF spectra with different layer distances. It can be seen that the two targets (cardboard layers) can be well distinguished between each other when the distance is more than 10
With a range difference of 3 cm, two peaks can still be recognized from the IF spectra, as is shown in Fig. 4.7 (c), but are very close to each other. So the range resolution of such a radar setup is better than 3 cm.

A penetration test is also carried out on different materials while a piece of metal is placed on the backside as a reference, as is shown in Fig. 4.8. A plastic board, a piece of wet cardboard and a piece of wood have been alternatively placed as the first target in front of the Tx/Rx antenna. Fig. 4.9 shows the measured IF spectra of the three cases. It can be seen that the ~140 GHz signal penetrates through a 0.5 cm thick plastic board with barely any loss, while a 0.3 cm thick piece of wet cardboard and a 2 cm thick piece of wood show around 20 dB loss and 40 dB loss in a return path, respectively.
Chapter 5

Conclusions

In this thesis, millimeter and sub-millimeter wave frequency converters are studied as possible candidates for the next generation of high-speed communication and standoff imaging applications. State-of-the-art semiconductor manufacturing technologies, which include a 100 nm GaAs mHEMT technology, a 250 nm InP DHBT technology, and a 130 nm SiGe BiCMOS technology, are employed for circuit designs. In chapter 3, the self-oscillating mixer, the resistive mixer, the Gilbert mixer, and the transconductance mixer are described. Circuits based on those mixer topologies are designed and characterized at, or aiming at, the ~145 GHz frequency range, ~220 GHz frequency range, or ~340 GHz frequency range. From the measurement results, these mixers are suitable candidates in given technologies to be further integrated with other components.

In chapter 4, a 110~170 GHz novel transceiver is designed and manufactured for standoff imaging applications. It is successfully demonstrated in a FMCW radar setup for distance measurement. This circuit is planned to be packaged into a waveguide module and employed in an imaging scanning system. Furthermore, the design is planned to be scaled to 220 GHz and 340 GHz.
Appendix

Noise Figure Measurements

The noise figure is an important factor from a system perspective. It measures the amount of noise added by a component, and is defined by the ratio of the input signal-to-noise ratio (SNR) to the output SNR, or more often by the ratio of the total available noise power at the output to the output available noise power due to thermal noise originating from the input resistor at standard room temperature [104]. The noise can be quantified by either the equivalent noise temperature (T_e) or the noise factor (F), and they can be interconverted by:

\[ T_e = T_0 (F - 1) \]  

(A.1)

In communication fields, the noise figure (NF) in dB, which is 10\log_{10} F, is often preferred.

A.1 Traditional Noise Figure Measurement Methods

Traditional noise figure measurement methods include the direct noise measurement method, the Y-factor method and the signal generator twice-power method [82]. Representing the device under test (DUT) in Fig. A.1, where

- \( G \) is the power gain in linear scale.
- \( T_e \) is the equivalent noise temperature, which is to be measured.
- \( B \) is the equivalent noise bandwidth.

![DUT Diagram](image)

Fig. A.1. Block diagram of a DUT represented by its power gain (G), equivalent noise temperature (T_e), and equivalent noise bandwidth (B).
Table A. 1.
TRADITIONAL NOISE FIGURE MEASUREMENT METHODS

<table>
<thead>
<tr>
<th>Method</th>
<th>Noise temperature</th>
<th>Noise factor (linear scale)</th>
<th>Parameters should be known</th>
<th>Limitations at mm/sub-mm wave</th>
</tr>
</thead>
<tbody>
<tr>
<td>Direct noise power method</td>
<td>$T_e = \frac{P_N}{kB} - T_0$</td>
<td>$F_{DUT} = \frac{P_N}{kT_0B}$</td>
<td>$^*P_N, G, B$</td>
<td>Active DUT with moderate to high NF</td>
</tr>
<tr>
<td>Y-factor method</td>
<td>$T_e = \frac{T_{hot} - YT_{cold}}{Y - 1}$</td>
<td>$F_{DUT} = \frac{T_{hot} - YT_{cold}}{(Y - 1)T_0} + 1$</td>
<td>$^#T_{hot}, ^5T_{cold}, ^*Y$</td>
<td>Low to moderate (&lt;10 dB) NF</td>
</tr>
<tr>
<td>Twice-power method</td>
<td>$T_e = \frac{P_{gen}}{kB} - T_0$</td>
<td>$F_{DUT} = \frac{P_{gen}}{kT_0B}$</td>
<td>$^\odot P_{gen}, B$</td>
<td>Active DUT with high NF</td>
</tr>
</tbody>
</table>

$k = 1.38 \times 10^{-23}$ J/K is the Boltzmann constant.
$T_0 = 295$ K is the standard room temperature in Kelvin.
$^* P_N$ is the measured output noise power.
$^# T_{hot} = 295$ K (standard room temperature) is the hot temperature in Kelvin.
$^5 T_{cold} = 77$ K (temperature of liquid nitrogen) is the cold temperature in Kelvin.
$^* Y$ is the ratio of the measured output noise power when the input is terminated by a matched load at $T_{hot}$ and $T_{cold}$.
$^\odot P_{gen}$ is the power of the input continuous wave signal when the total measured output power is twice as the output noise power only.

Table A. 1 lists the properties of the traditional methods. As can be seen from the limitations at the millimeter/sub-millimeter wave range, none of the traditional methods would work nicely for a relative high noise figure component, which has no gain and nearly passive, e.g. resistive mixers. Therefore, based on the signal generator twice-power method, the signal generator N-times power method is proposed.

A.2 Signal Generator N-Times Power Method

Fig. A.2 shows the working principle of the signal generator N-times power method. The output noise power is first measured when the input port is terminated by a matched load at the standard room temperature, and represented by $P_1$:

$$P_1 = k(T_0 + T_e)BG$$  \(\text{(A.2)}\)
Then the input is fed with a continuous wave signal, which is within the bandwidth of the DUT. With a certain input power of $P_{\text{gen}}$, the output power can be measured and represented by

$$P_2 = k(T_0 + T_e)BG + P_{\text{gen}}G$$ (A.3)

The $N$ factor is defined as

$$N = \frac{P_2}{P_1}$$ (A.4)

Substituting eq. (A.2) and eq. (A.3) into eq. (A.4), the equivalent noise temperature can be expressed by

$$T_e = \frac{P_{\text{gen}}}{kB(N - 1)} - T_0$$ (A.5)

And the noise factor is:

$$F_{DUT} = \frac{P_{\text{gen}}}{kT_0B(N - 1)}$$ (A.6)

So far, the dynamic range of a power meter is very much limited at frequencies above 100 GHz, e.g. ~1 µW from an Erickson power meter [105]. Therefore, the proposed signal generator N-times power method is especially beneficial, because the input $P_{\text{gen}}$ can be an arbitrary amount of power.
Summary of Appended Papers

Paper A

24 GHz Balanced Self-Oscillating Mixer with Integrated Patch Antenna Array

This paper presents the design and characterization of a 24-GHz self-oscillating mixer integrated with a 16 element quadratic microstrip patch array. It has been demonstrated as a receiver front-end without any additional local oscillator supply. I contributed with the design, simulation and measurement of the SOM circuit part while the patch array antenna was designed by Y. B. Karandikar, radar measurement together with Y. B. Karandikar, and writing of the paper.

Paper B

Monolithically Integrated 200-GHz Double-Slot Antenna and Resistive Mixers in a GaAs-mHEMT MMIC Process

This paper presents the design and characterization of a single-ended and a balanced 200-GHz integrated resistive mixer with double-slot antenna in a 100 nm GaAs-mHEMT technology. A novel method is also proposed and proved to evaluate a moderate to high noise figure device in millimeter/sub-millimeter frequency band. The mixers were originally designed by Sten E. Gunnarsson and Bahar M. Motlagh, and the antenna was originally designed by Bahar M. Motlagh under supervision from Sergey Cherednichenko. I contributed with circuit re-simulation, characterization together with Y. B. Karandikar, idea and experimental validation of the novel noise figure measurement method with Y. B. Karandikar, and writing of the paper.

Paper C

340 GHz Integrated Receiver in 250 nm InP DHBT Technology

This paper presents a 340 GHz integrated receiver, which consists of a sub-harmonically pumped Gilbert mixer, a differential IF buffer amplifier, and a 2×2 differential patch array antenna, in a 250 nm InP DHBT technology. This work demonstrated the first integrated receiver above 300 GHz in such technology. The antenna was designed by Y. B. Karandikar. I contributed with the design and simulation of the Gilbert mixer and IF amplifier, measurements together with Y. B. Karandikar, and writing of the paper.
Paper D

A 110-170-GHz Multi-Mode Transconductance Mixer in 250-nm InP DHBT Technology

This paper presents a 110-170 GHz multi-mode transconductance mixer in a 250 nm InP DHBT technology. It is successfully demonstrated as a ×1, ×2, ×3, and ×4 harmonic mixer. In order to understand how the mixer should be biased at different harmonic mixing modes, an arbitrary harmonically pumped transconductance mixer is described. The circuit was originally designed by Mingquan Bao. I contributed with the circuit re-simulation, characterisation, theoretical mechanism analysis, and writing of the paper.

Paper E

A 110-170 GHz Transceiver in 130 nm SiGe BiCMOS Technology for FMCW Applications

This paper presents a balanced 110-170 GHz transceiver in a 130 nm SiGe BiCMOS technology for FMCW applications. The designed transceiver operates as an amplifier for transmitting and simultaneously as a down-converter for receiving. The transceiver is successfully demonstrated as an FMCW radar for distance measurement. I contributed with the design and simulation of the circuits, measurements together with T. Bryllert, and writing of the paper.
Acknowledgement

The journey towards my PhD has been full of challenges, happiness, and occasional confusions. All those experiences shaped who I am today, and I would like to express my gratitude to the people who have helped me during my PhD study.

I would like to express my deepest gratitude to my supervisor Prof. Herbert Zirath. Looking back over the past six years, I feel so lucky to be one of his PhD students. As a supervisor, he offered me the opportunity to explore the world of monolithic microwave integrated circuit design freely, and supported me with continuous inspiration, encouragement, and guidance. As an employer, he expressed the kindest understanding especially when I was pregnant and on parental leave. Also, I would like to thank my co-supervisor Sten E. Gunnarsson for his valuable suggestions and discussions whenever I had new ideas or got confused in my research. He helped me to make detailed study plans towards my PhD, and always supported me with prompt proofreading.

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In addition, Sivers IMA is acknowledged for the support and PCB manufacturing of the SOM circuit. The Fraunhofer Institute for Applied Solide-State Physics (IAF), Teledyne Technologies, and Infineon Technologies are acknowledged for MMIC chips manufacturing.

Lastly, I would like to acknowledge my parents for always believing in me and caring about me, my beloved husband Dapeng for greatest support with all his love, and my sweet daughter for bringing us a more colourful life.

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Bibliography


Paper A

24 GHz Balanced Self-Oscillating Mixer with Integrated Patch Antenna Array

Y. Yan, Y. B. Karandikar, S. E. Gunnarsson, and H. Zirath

Abstract—Design and performance of a balanced self-oscillating mixer (SOM) co-designed and integrated with a 16 element quadratic microstrip patch array is presented in this paper. The oscillation frequency of the SOM is 24 GHz and the conversion gain is better than -15 dB. The patch antenna array has a gain better than 16 dB. The integrated receiver has a 3dB-bandwidth of 800 MHz and a peak receiver gain of 5.9 dB.

Keywords- Self-Oscillating Mixer, Microstrip Patch Array

I. INTRODUCTION

The allocated industrial, scientific and medical (ISM) band around 24 GHz is one of attractive bands for the short range radar applications varying from high-tech automotive collision avoidance and healthcare sensors to low-tech door openers. In order to be more commercially competitive in all applications, high performance, low cost and compact size are always of large interest. A traditional receiver front-end is typically composed of antenna, mixer, and a local oscillator (LO). As the operating frequency increases, high output power LO multiplication chain tends to become bulky but is necessary in order to drive the mixer efficiently.

The first FET SOM was reported in [1] where the function of mixer and oscillator are realized by the same transistor without any external LO feed. Since the oscillating frequency is limited by device's $f_{\text{max}}$, sub-harmonic SOM [2] and balanced SOM [3] where the input RF signal will mix with higher order LO harmonics are good solutions to extend the frequency range of operation.

For a cost-effective overall solution, it is beneficial if both the mixer and antenna are integrated in the same planar technology. Planar dipoles are not considered in this work due to the matching problem in the chosen technology with thin substrate. Even though planar slots are feasible, they require opening in the ground planes when fed by microstrip lines. Hence, for easy integration with microstrip, a patch array is selected as suitable candidate.

In this paper, a balanced SOM integrated with a patch antenna is designed for 24 GHz application. The overall design was integrated on standard Rogers3003 with $\varepsilon_r=3$, [4].

The surface mount active devices are standard VMMK-1225 HEMTs offered by Avago Technologies, [5]. The proposed topology performs well as a receiver and can be further modified for FMCW application.

II. BALANCED SOM DESIGN

The SOM can be designed as a simple combination of a single-ended mixer and a common source oscillator, as shown in Fig. 1. Because of the source and gate feedback, the transistor oscillates at a frequency determined by the oscillation condition. The RF input signal from the gate is mixed with the oscillating frequency, and an IF output signal is extracted by a low-pass filter from the drain.

The balanced SOM contains two identical SOMs shown in Fig. 1, which are connected by a transmission line at the gate, as shown in Fig. 2. According to the analysis in [3], such fully symmetric topology forces the middle point of the gate transmission line as virtual ground. In this case, once the two transistors start oscillating, signals generated by these two branches will be 180-degree out-of-phase.

![Fig. 1. Combine single-ended mixer and common source oscillator into a SOM.](image-url)
Fig. 2. Schematic of balanced SOM.

Fig. 2. shows the schematic of the balanced SOM in this work. Both the gate transmission line and the shunt capacitance ‘C1’ serve as the gate feedback. The oscillating frequency can be tuned by varying the length of the transmission line or by varying the capacitance ‘C1’. Negative resistance at the gate is introduced by the source feedback capacitor ‘C2’. The fundamental oscillating frequency of 12 GHz is achieved by tuning the value of C1, C2 and the length of the gate transmission line in ADS simulation. A quarter wavelength short-circuited stub (at 24 GHz) is connected at the source to complete DC ground path of the transistor. The synthesized low-pass filter needs inductances in the order of nH. The high-Q inductors are realized with bond wires instead of surface-mount inductors with low-Q factor. The RF port when inserted at the centre point does not affect the oscillation condition due to the virtual ground property.

The anti-phase conditions offered by the topology will cancel the fundamental frequency and all the odd harmonics at both RF and IF ports, while the even harmonics are in phase.

The stand-alone SOM is manufactured and measured. The LO applied by the 2nd harmonic of the self-oscillation frequency is around 24 GHz. Then the measured conversion gain of the balanced SOM is shown in Fig. 3(a). A peak conversion gain of -13.3 dB @ 24.7 GHz is achieved with an optimum bias point of Vd=2.6 V and Vg=0.4 V. Sweeping RF frequencies from 24.6 GHz to 25.5 GHz, better than 15 dB conversion loss is achieved. The deep drop at 24.2 GHz is caused by resonance of drain bias network at 200 MHz IF, and it can be shifted down towards lower IF frequency by adding a serial connected inductor. As can be seen from Fig. 3(b), the input 1 dB compression point is around 0 dBm.

III. ANTENNA DESIGN

The patch antennas being resonant, offers limited bandwidth and it strongly depends upon the thickness and dielectric constant of the substrate. For wide bandwidths, low εr and thick substrates are suggested [6]. The wideband patch arrays even though having excellent crosspol characteristics requires multiple PCB layers to achieve aperture coupling [7]. Also bandwidth of the patch can be enhanced by using inset feed or making openings in the ground plane of the patch [8]. But for current application, to achieve low cost solution, only single metal layer is used for the design. With such a constraint, series fed microstrip patches integrated with MMIC receiver in mm wave band are demonstrated in [9],[10]. Integration of such an array with sub-harmonic mixer is demonstrated in [11].

Even though, series fed patch array is simpler in layout, the phase shift offered by the patch and the series line becomes frequency dependent, which results in beam scanning. Hence, for this work, broadside beam with 20dBi directivity using uniform amplitude and phase feeding network is selected.

A. Analytical Far-field function of Patch Array

Microstrip patch antennas inherently have broad beamwidths. So for higher directivity, uniformly excited patch array is unavoidable. The far-field function of single patch by using transmission line model is discussed in [12],[13]. By choosing the origin of coordinate system to center of the patch the far-field function is written as,

\[ G_p(\theta, \phi) = \frac{j \cdot 4F_p h}{\pi} \left\{ \frac{\sin \left( k \frac{w}{2} \sin \theta \cos \phi \right)}{\sin \theta \cos \phi} \right\} \]

\[ = \left[ \cos \left( k \frac{l}{2} \sin \theta \sin \phi \right) \sin \phi \right] \left[ \sin \phi + \cos \phi \cos \theta \sin \phi \right] ; \theta \leq \frac{\pi}{2} \]

\[ = k \frac{w}{2} \sin \theta \cos \phi \to 0 \]

\[ G_p(\theta, \phi) = 0 \quad \cdots \cdots \cdots \theta > \frac{\pi}{2} \]

where

- \( l \) = length of the patch;
- \( w \) = width of the patch.

Thus, when RF is applied, it splits in phase to both gates and mixed with 2nd harmonic and further gets added at the IF port.
k=propagation constant;
\( h \) =height of the substrate.

The far-field function of whole array is then achieved by element-by-element sum technique. To get equal beamwidths in E- and H- planes quadratic array with equal spacing in x-y direction is chosen. The requirement of 20dBi directivity gets satisfied by choosing 4 x 4 elements with spacing of \( \sim 0.75 \lambda \). The complete analytical far-field function of array is then written as,

\[
G_A(\theta, \phi) = \sum_{m=1}^{N} \sum_{n=1}^{N} G_P(\theta, \phi) \frac{\Delta}{N}\sin \theta \left( m - \frac{N+1}{2} \right) \cos \phi + \left( n - \frac{N+1}{2} \right) \sin \phi
\]

where

- \( \Delta \) = element spacing in x-y direction (9000\( \mu \)m);
- \( N \) = max. number of elements (\( N=4 \)).

**B. Simulated & Measured Performance of Patch Array**

For practical array, feeding network made up of microstrip lines and finite ground plane size is needed. Once the array geometry is selected, the initial patch dimensions are calculated using [13]. The microstrip feed network for 4 x 4 elements is designed using [14]. Finally, the whole geometry was simulated and optimized in [15]. The comparison between analytical patch array with infinite ground plane and simulated patch array with feeding network and finite ground plane size of 42 x 40 mm\(^2\) is shown in Fig. 4.

**Fig. 5.** (a) Simulated gain, (b) simulated and measured S11.

**Fig. 6.** Simulated and measured (a) E-plane and (b) H-plane @ 25 GHz.

**IV. RECEIVER CHARACTERISTICS**

The 24 GHz balanced SOM integrated with 16 element quadratic microstrip patch array was fabricated and mounted as shown in Fig.7.

**Fig. 7.** Fabricated 24 GHz SOM with integrated 16-element patch antenna, board size 75x45mm.

For the characterization of the SOM with integrated antenna, a measurement setup according to Fig. 8 was
arranged. The horn antenna and receiver SOM are aligned for horizontal polarization at a range of 4 m, which guarantee the far field condition.

![Measurement setup and link calculations.](Image)

**Fig. 8.** Measurement setup and link calculations.

The IF power can be calculated by Eq. (1).

$$P_{IF} = P_t + G_t - L_{RF}^{cable} - L_{FS} + G_r + G_{SOM} - L_{IF}^{cable}$$  \(1\)

where the power values are measured in dBm, and the gain/loss are given in dB:

- \(P_t\) = power from generator;
- \(G_t\) = gain of horn antenna;
- \(L_{RF}^{cable}\) = loss of RF cable;
- \(L_{FS} = 20\log \left(\frac{4\pi d}{c}\right)\) (free-space path loss);
- \(G_r\) = gain of patch array;
- \(G_{SOM}\) = conversion gain of SOM;
- \(L_{IF}^{cable}\) = loss of IF.

The simulated and measured IF power is shown in Fig. 9(a). The gain of the integrated receiver, which incorporates the antenna gain and the conversion loss of the SOM \((G_{receiver} = G_r + G_{SOM}\) in dB), can be extracted from the measurement, and the result is shown in Fig. 9(b). The peak gain of the receiver achieves 5.9 dB at 25.3 GHz RF. A 3dB-bandwidth of 800 MHz is obtained with a power consumption of 52 mW.

![Simulated and measured IF power.](Image)

**Fig. 9.** (a) Measured & simulated IF power, (b) Measured receiver gain

The simulated and measured system performance agrees well. The bandwidth for VSWR<2.0 is about 1GHz and can be improved with appropriate choice of substrate. Also the simulated and measured system performance agrees well. The integrated receiver achieves a peak gain of 5.9 dB and a 3dB-bandwidth of 800 MHz.

**V. CONCLUSION**

A balanced self-oscillating mixer integrated with 16 element quadratic microstrip patch array is designed, fabricated and measured for 24 GHz receiver application. Inherent symmetry of balanced SOM guarantees the anti-phase performance and amplitude balance, which further suppress the fundamental oscillation efficiently. RF signals mix with the 2nd harmonic of the oscillating frequency and a better than -15 dB conversion gain is achieved with 900 MHz bandwidth. The measured patch array performance is in agreement with simulations. The bandwidth for VSWR<2.0 is about 1GHz and can be improved with appropriate choice of substrate. Also the simulated and measured system performance agrees well. The integrated receiver achieves a peak gain of 5.9 dB and a 3dB-bandwidth of 800 MHz.

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**REFERENCES**


Monolithically Integrated 200-GHz Double-Slot Antenna and Resistive Mixers in a GaAs-mHEMT MMIC Process

Y. Yan, Y. B. Karandikar, S. E. Gunnarsson, B. Motlagh, S. Cherednichenko, I. Kallfass, A. Leuther, and H. Zirath

Monolithically Integrated 200-GHz Double-Slot Antenna and Resistive Mixers in a GaAs-mHEMT MMIC Process

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Abstract—This paper presents the design and characterization of two resistive mixers integrated with a double-slot antenna in a 100-nm GaAs mHEMT technology. With RF frequency varying from 185 to 202 GHz, a typical conversion loss ($L_c$) of 6.0 dB is measured for the single-ended mixer and a typical $L_c$ of 12.2 dB is obtained from one of the two IF outputs for the single-balanced mixer. Each mixer is integrated with a double-slot antenna and mounted on an Si lens. Incorporating the antenna gain and the conversion loss of the mixer, a typical receiver gain of 15.4 dB is achieved for the integrated antenna with single-ended mixer, and a typical receiver gain of 11.2 dB is obtained for the integrated antenna with single-balanced mixer by measuring one of the two IF outputs.

In this paper, a novel method is also proposed and proved to evaluate a moderate to high noise figure (NF) device in millimeter/sub-millimeter frequency band. The result shows that the single-ended mixer in this paper has an NF around 1.0 dB higher compared to its $L_c$, and the single-balanced one has an NF about 1.6 dB higher than its $L_c$ at room-temperature operation.

Index Terms—Conversion loss, double-slot antenna, GaAs, $G$-band, metamorphic HEMT (mHEMT), monolithic microwave integrated circuit (MMIC), noise figure (NF), $N$-times, resistive mixer, system gain.

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the metamorphic approach are the price and quality of the GaAs wafers. The material is less brittle than InP, and wafers with high crystal quality are available up to 150-mm wafer diameter. In addition, metamorphic buffers with lattice constants larger than InP enable even InAs channels [7]. The disadvantage of the mHEMT is the additional growth effort.

The mHEMT layers are grown on 4-in semi-insulating GaAs wafers by molecular beam epitaxy (MBE). For the metamorphic buffer, a linear $\text{In}_x\text{Al}_{1-x}\text{Ga}_{0.52}\text{As}$ ($x \approx 0 \rightarrow 0.52$) transition is used. Electron beam evaporated GeAu layers are used for the ohmic contacts, which are alloyed at $300 \, ^\circ\text{C}$ on a nitrogen purged hot plate. The 100-nm T-gate is defined by 100-kV electron beam lithography. The devices are passivated with a 250-nm-thick chemical vapor deposition (CVD) deposited SiN layer used as a dielectric layer for the metal–insulator–metal (MIM) capacitors. Further passive elements are NiCr thin-film resistors, an electron beam evaporated Au based interconnection layer, and a 2.7-$\mu$m-thick plated Au layer in air-bridge technology.

For MMICs operating in the $G$-band and beyond, a backside process was developed to suppress substrate modes within the circuits. After front side processing, the 4-in GaAs wafers are glued to sapphire substrates in a vacuum chamber. The GaAs substrates are thinned to a final thickness of 50 $\mu$m. Through-substrate vias are etched in a chloride based ICP etching process using resist as etching mask. The via diameter at the etch stop layer on the front side is 30 $\mu$m. An additional lithography layer defines the dicing streets on the Au plated wafer backside. Subsequently the 50-$\mu$m-thick GaAs wafer is separated from the sapphire substrate by dissolving the glue in an organic solvent. The wafers are rinsed, dried, and subsequently carefully transferred to glue tape for final measurements and dicing.

Typical electrical dc and RF parameters of a $2 \times 30 \, \mu$m gate width 100-nm mHEMT are shown in Table I.

### Table I

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_c$</td>
<td>0.07 $\Omega$</td>
</tr>
<tr>
<td>$R_d$</td>
<td>0.25 $\Omega$</td>
</tr>
<tr>
<td>$\eta_{\text{max}}$</td>
<td>1400 $\text{mS/mm}$</td>
</tr>
<tr>
<td>$I_{\text{D, max}}$</td>
<td>900 $\text{mA/mm}$</td>
</tr>
<tr>
<td>$f_s$</td>
<td>200 GHz</td>
</tr>
<tr>
<td>$f_{\text{max}}$</td>
<td>300 GHz</td>
</tr>
</tbody>
</table>

The metamorphic approach is often limited by the layer topology of HEMT process. Since the MMIC cost in manufacturing is proportional to its size, small gain antennas are usually feasible. Different types of antenna structures such as single-section coupled line filter, and the LO is applied through a single stub matching network to the gate of the FET. The IF signal is extracted by an IF filter from the drain. As a resistive mixer, the drain remains unbiased, and the gate voltage, applied through a large resistor, biases the transistor close to pinch-off for enhanced $I_c$ and distortion characteristic. A breakout of the single-ended resistive mixer, without the double-slot antenna, was presented in [9].

A drawback of the single-ended topology is that the LO-to-RF isolation is poor. According to [9], only 9.3-dB isolation was achieved by the single-ended mixer. To suppress this unwanted LO leakage, a balanced mixer topology could be used [10]. The second mixer presented in this paper is a 200-GHz single-balanced resistive mixer. The schematic of this mixer is shown in Fig. 2. A half-wavelength transmission line is used as an 180$^\circ$ phase shifter to apply differential LO signals at the gates of the FETs. Sufficiently low loss of this line ensures amplitude balance between the two branches. The residual out-of-phase LO signals will be combined in-phase and cancelled at the drain. Two 180$^\circ$ out-of-phase IF signals are extracted from the two drains and can be combined in an external balun.

### B. Antenna Design

The choice of MMIC-based antenna is often limited by the layer topology of HEMT process. Since the MMIC cost in manufacturing is proportional to its size, small gain antennas are usually feasible. Different types of antenna structures such as
dipoles, folded dipoles, microstrip fed patch, and slots are possible with the layers found in a typical HEMT process. Review on these types of antennas is given in [4].

Slot antennas are preferred in our case in comparison to patch or dipole since microstrip patches on thin substrates have poor ohmic efficiency, while dipoles on thin substrate exhibit low real part of input impedance (a few ohms), which makes them difficult to match.

Coplanar waveguide (CPW) fed double slot antennas are often used at millimeter-wavelengths since its radiation can be coupled to a focusing ellipsoidal lens, as presented in [11] and [12]. Two slot antennas separated by \( \lambda_{d}/2 \) make radiation pattern equal in the \( E \)- and \( H \)-plane. With CPW type of feeding, the slots radiate through the substrate and then further into the lens. If the substrate dielectric constant is matched with the lens, most of the radiation is focused by the lens and the problem of surface wave modes is overcome. It is also possible to use a folded slot antenna fed by CPW lines in this topology, as in [13] and [14].

GaAs, having a dielectric constant of 12.9, is not well matched to that of Si having \( \varepsilon_r = 11.7 \). Hence, the CPW fed double slot antenna should be modified to be fed with microstrips. Considering the layer topology of the process, slots can be etched out in backside metal layer with microstrip feeding them at top metal layer. The slots directly radiate in the Si lens beneath it. The feeding structure and topology is shown in the inset of Fig. 3.

The separation between the slots is a half-wavelength in silicon. The impedance properties of such microstrip fed slot are studied in [15]–[17], and improved matching of the folded slot using a via-hole is discussed in [18]. In this case, since the slot is at the interface of Si and GaAs, its resonant length is approximately chosen as \( \lambda_{d}/2 \) and the length, as well as radial stub, is optimized numerically for antenna input impedance of 50 \( \Omega \).

In this work, the length of the slots and the separations are optimized as 180 and 190 \( \mu \)m, respectively. The microstrip lines are terminated with a radial stub and the output from two slots is combined with a microstrip tee.

Fig. 3. Double slot antenna with microstrip feed network on Si lens.

The Si-lens used in this work has a diameter of 10 mm with ellipsoidal surface defined by semi-major and minor axes of 5.228 and 5 mm, respectively. High-resistivity Si is chosen as a material for fabrication along with the antireflection coating (ARC) of 210-\( \mu \)m thickness made from Stycast 1264 (\( \varepsilon_r = 2.9 \)). Stycast is chosen because its dielectric constant is the closest to the optimum value required, which is 3.42. While mounting the chip on the lens, care is taken that the antenna center is aligned to the lens optical axis to maximize the directivity in broadside direction. The overall geometry of chip+ lens is shown in Fig. 3.

The complete geometry presented in Fig. 3 has a large size, and full wave simulation on the whole geometry is time consuming. Hence, for faster simulation, the slots can be made to radiate in infinite Si medium without modeling the lens. Ideally, the slots should radiate in air for upper hemisphere and in infinite Si in lower hemisphere. The simulation tool used in this work, CST MWS [19], allows the complete volume to be filled with the same material, which means that we cannot model the volume as a combination of a semi-infinite Si medium and a semi-infinite air medium. This limitation is overcome by putting finite vacuum box with two Chebyshev quarter-wave matching layers [20] on the microstrip network side, i.e., upper hemisphere, while the rest of the volume is filled with Si. This is illustrated in Fig. 4. By making use of these matching layers, the slot impedance can be optimized much faster as compared to simulating with a whole lens. The double slot antenna input reflection coefficient at microstrip port, optimized for \( Z_{\text{ref}} = 50 \Omega \), using this method is shown in Fig. 5 along with the input reflection coefficient obtained after simulating the entire structure with ellipsoidal lens. The difference between two input reflection coefficients is due to the fact that the ARC made by Stycast is not the ideal one. This results in the small ripples in \( S_{11} \), as seen in Fig. 5.

The simulated antenna (together with Si Lens+ARC) radiation patterns at 200 GHz are shown in Fig. 6 (top). The sidelobe level is \( \sim -19 \) dB down. This result is similar to that of [12, Fig. 4] with an extension length of 2600 \( \mu \)m for extended hemispherical lens. The variation of the \( E \)-plane pattern for different frequency points is shown in Fig. 6 (bottom). Altogether, this antenna design achieves directivities of \( \sim 24.5 \) dBi and matching of \( -10 \) dB over 190–205 GHz.

IV. INTEGRATION OF ANTENNA AND MIXER

The RF ports of both the single-ended mixer and single-balanced mixer are matched to 50 \( \Omega \) for breakout measurements. The double-slot antenna is also matched to the same impedance.
Fig. 5. Simulated antenna input reflection coefficient.

Fig. 6. (top) Simulated normalized co- and cross-pol directivity at $f = 200$ GHz, $\phi = 45^\circ$ plane. (bottom) Simulated $E$-plane patterns for various frequencies.

and is directly coupled to the RF port of the mixer. Chip photographs are shown in Fig. 7. The double slots located at the back of the GaAs substrate beneath the coupler’s arms are marked by the black dashed rectangles. The chip dimensions are $1100 \times 700 \mu m^2$ and $900 \times 950 \mu m^2$, respectively.

V. Measurements

Fig. 8 shows the measurement setup. The transmitter is an in-house manufactured $\times 6$ frequency multiplier source module (output frequency band: 163–202 GHz) with a $G$-band corrugated horn antenna. The transmitter is aligned around 200 mm underneath the Si lens. The local oscillator (LO) signal is applied by a Virginia Diodes Inc. (VDI) $\times 18$ source module together with a signal generator, and further pumped into the mixer’s LO port through a $G$-band on-wafer ground–signal–ground (GSG) probe. The IF output signal is then amplified by an LNA (with 29-dB gain and 4-dB NF) and finally measured by a spectrum analyzer or power meter.

The gain ($G_{RX}$) of the integrated receiver, which incorporates the antenna gain referred to an isotropic antenna and the conversion loss of the mixer, can be represented by

$$G_{RX} = P_{out} - G_{LNA} + L_{probe} + L_{cable} + FSL - G_t - P_t$$

where the power values are measured in dBm, and the gain/loss are given in decibels.

- $P_{out}$ is the measured IF power.
- $G_{LNA}$ represents the gain of the IF LNA.
- $L_{probe}$ and $L_{cable}$ are the losses of the IF probe and the IF cable, respectively.
- Free-space loss (FSL) can be calculated by $FSL = 20 \cdot \log\left(\frac{4\pi d}{\lambda}\right)$ dB and $d$ is the distance between the transmitter and receiver.


$G_t$ is the gain of the corrugated horn and is obtained by electromagnetic (EM) simulation.

$P_s$ is the RF power from the $\times 6$ module. It was kept at $-20$ dBm for all the RF frequencies.

Considering the double-slot antenna and the resistive mixers are impedance matched, the mixer’s conversion loss $L_c$ can be deduced by

$$L_c = G_r - G_{RX}$$

where the gain ($G_r$) of the antenna with lens is derived from EM simulation.

### A. Measured Results of the Receiver With Single-Ended Resistive Mixer

The gate voltage of the device is tuned prior the measurements to determine the optimum bias that gives the minimum $L_c$. This tuning is repeated at different LO and RF frequencies and 0 V is chosen as the optimum gate voltage.

Fig. 9 shows the measured $L_c$ versus applied LO power, which is limited by the power from the VDI $\times 18$ source module. With a maximum applied $+5$-dBm LO power (probe loss has been accounted for), the single-ended mixer is not yet saturated.

Fig. 10 shows the $G_{RX}$ of the system and estimated $L_c$ of the mixer with fixed LO at 209 GHz and a LO power of $+5$ dBm. Within the measured bandwidth, the $G_{RX}$ is higher than 13.5 dB while the typical $L_c$ is 8.0 dB. The measured IF bandwidth is limited by the bandwidth of the $\times 6$ source module, which can only generate signals up to 202 GHz. However, nothing suggests that the IF bandwidth is limited to the shown 6–24 GHz in the measurement setup, the signal radiated from the transmitting horn not only illuminates the double-slot antenna with Si lens. The rest of the signal power is also reflected by any materials on its way. Some significant fluctuations (e.g., 3.5 dB jumps from 21 to 22 GHz) that are caused by multipath effect can be seen from the curves. The results have been improved significantly by placing absorbing material in a wide area around the transmitting antenna.

The $G_{RX}$ of the receiver and the $L_c$ of the mixer are also measured at fixed IF of 1 GHz by tuning the LO and RF frequencies at the same time, as shown in Fig. 11. At each LO frequency, the highest output power (3–5 dBm after probe loss correction) from the LO module is applied to the mixer. A typical system gain of 15.4 dB is achieved, and the typical $L_c$ is 8.0 dB.

### B. Measured Results of the Receiver With Single-Balanced Resistive Mixer

The single-balanced mixer has two differential IF outputs that are not combined on-chip. During the measurements, only one of the IF output signal is measured while the other one is terminated with a 50-Ω load. As the input LO power is split into two equal parts to feed the balanced topology, lower LO power to each branch will see a higher $L_c$ of the individual mixer cells compared to the single-ended mixer.

The same measurements have been performed on the receiver with single-balanced mixer as for the single-ended design. −0.2 V is chosen to be the optimal gate voltage.

In the measurement, we found that the outputs from the two IF ports are not equal, but possesses a 4-dB difference. When resimulating the design, this unequal performance from the two IF ports can be observed. As can be seen from the simulated conversion loss as a function of LO power in Fig. 12, $L_c$ derived from the “IF+” port, referred to Fig. 7(b), is better than that from “IF−” port unless the transistors are saturated by sufficient LO power. Further simulation indicates that this effect

---

**Fig. 9.** Conversion loss versus LO power for the single-ended mixer ($f_{LO} = 20$ GHz, $f_{RF} = 201$ GHz).

**Fig. 10.** Conversion loss of the single-ended resistive mixer and measured gain of the integrated receiver with single-ended mixer ($f_{LO} = 209$ GHz).

**Fig. 11.** Conversion loss of the single-ended resistive mixer and measured gain of the integrated receiver with single-ended mixer ($f_{RF} = f_{LO} - f_{RF} = 1$ GHz).
originates from the on-chip LO balun, which is shorter than a desired length of $\lambda_{LO}/2$, and results in an unequally pumped LO power at the gates of the two transistors. The performance of this mixer could thus be improved by a properly designed LO balun. The following results will present the performance obtained from the “IF+” port.

Keeping the maximum LO power (3–5 dBm over frequency after probe loss correction) from the LO source, the $G_{RX}$ of the receiver and the $L_c$ of the single-balanced mixer are measured with fixed LO ($\approx 184$ GHz) and fixed IF ($\approx 1$ GHz), respectively, as shown in Figs. 13 and 14. The receiver achieves a typical gain ($G_{RX}$) of $11.2$ dB and the resistive single-balanced mixer achieves a typical $L_c$ of $12.2$ dB.

C. NF Estimation

For the measurement of NF, we propose a novel method, called the signal generator $N$-times power method, which is suitable for evaluating moderate to high NF devices operating beyond 100 GHz. According to this method, the noise factor can be calculated as

$$F_{sys} = \frac{P_{gen}}{k \cdot T_0 \cdot B \cdot (N - 1)}$$

(3)

where

- $F_{sys}$ is the noise factor to be determined;
- $k$ is the Boltzmann constant;
- $T_0$ is the room temperature in Kelvin;
- $B$ is the noise bandwidth in hertz;
- $N$ is the ratio between two output powers;
- $P_{gen}$ is the input power in watt.

More details of the signal generator $N$-times power method is clarified in the Appendix.

The NF measurement setup is similar to the setup shown in Fig. 8, but a low-pass filter is added in the IF chain, as shown in Fig. 15. The NF of the receiver cascaded with the IF chain is evaluated by the signal generator $N$-times power method. For the measurement without continuous wave (CW) signal input, the matched load is replaced by absorbers at room temperature facing the receiver antenna. Certain power is then received from the transmitting antenna and $P_{gen}$ should be the calculated RF power right at the RF port of mixer. Once the NF of the cascaded
In order to make the measurement easier and compatible with the previous measurements, the IF is fixed at 1 GHz and RF and LO frequencies are swept. Fig. 16 shows the calculated NF of the single-ended mixer and the single-balanced mixer. Note that the NF curves have the same trend as the conversion loss, including certain multipath effect. This is reasonable, because for both NF and conversion loss measurement, we choose the same frequencies and use the same measurement setup, thus, the multipath effect will be the same. Comparing the NF with the shown in Figs. 11 and 14, respectively, the single-ended mixer has an NF around 1.0 dB higher than its 

<table>
<thead>
<tr>
<th>$f_{RF}$ (GHz)</th>
<th>*$G_C$ (dB)</th>
<th>NF (dB)</th>
<th>DC Consumption (mW)</th>
<th>Size (mm$^2$)</th>
<th>Antenna Topology</th>
<th>Technology</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>140</td>
<td>-43</td>
<td>N/A</td>
<td>120</td>
<td>0.58×0.7</td>
<td>Tapered Slot</td>
<td>65 nm CMOS</td>
<td>[25]</td>
</tr>
<tr>
<td>170</td>
<td>-30</td>
<td>21</td>
<td>800</td>
<td>1.52×0.84</td>
<td>Tapered Dipole (with metal fill)</td>
<td>120 nm SiGe BiCMOS HBT</td>
<td>[26]</td>
</tr>
<tr>
<td>200</td>
<td>15.4</td>
<td>9</td>
<td>0</td>
<td>1.1×0.7</td>
<td>Double-Slot</td>
<td>100 nm GaAs mHEMT</td>
<td>This Work</td>
</tr>
<tr>
<td>200</td>
<td>11.2</td>
<td>13.8</td>
<td>0</td>
<td>0.9×0.95</td>
<td>Double-Slot</td>
<td>100 nm GaAs mHEMT</td>
<td>This Work</td>
</tr>
<tr>
<td>220</td>
<td>2 (without antenna)</td>
<td>8.4</td>
<td>40</td>
<td>3.0×1.0</td>
<td>Square Slot</td>
<td>100 nm GaAs mHEMT</td>
<td>[2]</td>
</tr>
<tr>
<td>220</td>
<td>3.5 (without antenna)</td>
<td>7.4</td>
<td>110</td>
<td>2.75×1.75</td>
<td>Square Slot</td>
<td>100 nm GaAs mHEMT</td>
<td>[24]</td>
</tr>
<tr>
<td>650</td>
<td>-13</td>
<td>42</td>
<td>433</td>
<td>1.2×0.6</td>
<td>Folded Dipole</td>
<td>130 nm SiGe:C BiCMOS HBT</td>
<td>[3]</td>
</tr>
<tr>
<td>823</td>
<td>-22</td>
<td>47</td>
<td>1200</td>
<td>2.3×0.57</td>
<td>2×2 patch array</td>
<td>250 nm SiGe BiCMOS HBT</td>
<td>[27]</td>
</tr>
</tbody>
</table>

* $G_C$ is the receiver gain including the gain of receiver chain and the antenna gain referred to the isotropic antenna.

In order to make the measurement easier and compatible with the previous measurements, the IF is fixed at 1 GHz and RF and LO frequencies are swept. Fig. 16 shows the calculated NF of the single-ended mixer and the single-balanced mixer. Note that the NF curves have the same trend as the conversion loss, including certain multipath effect. This is reasonable, because for both NF and conversion loss measurement, we choose the same frequencies and use the same measurement setup, thus, the multipath effect will be the same. Comparing the NF with the shown in Figs. 11 and 14, respectively, the single-ended mixer has an NF around 1.0 dB higher than its $L_C$, and the single-balanced mixer shows an NF of 1.6 dB higher than its $L_C$.

### VI. COMPARISON TO OTHER REPORTED MONOLITHIC RECEIVER WITH ON-CHIP ANTENNA

The performance of the two receivers described in this paper is compared to the state-of-art monolithic integrated receiver with an on-chip antenna operating above 100 GHz. As can be seen from Table II, the integrated receiver in GaAs HEMT technologies performs better than those in silicon technologies in terms of conversion gain and NF. Two integrated single-chip receivers at similar frequencies and using the same MMIC technology are reported in [2] and [21]. These chips achieve better NF performance compared to the MMICs presented in this work. However, both of them integrate a three-stage LNA between the antenna and the mixer, which improve the system NF at the cost of a larger, and thus, more expensive solution in terms of manufacturing and DC power consumption. Therefore, the work presented in this paper with an antenna integrated with a resistive mixer is preferred where simplicity and low power consumption are critical issues.

### VII. CONCLUSION

In this paper, design and characterization of two resistive mixers integrated with a double-slot antenna on an Si lens have been presented. With +5-dBm LO power, a typical gain of 15.4 dB is achieved for the receiver with a single-ended mixer, and typically 8.0-dB conversion loss is obtained for the single-ended mixer. For the single-balanced topology, a typical gain of 11.2 dB is achieved for the receiver with one of the two IF outputs being measured, and a typical conversion loss of 12.2 dB is measured from one of the two IF outputs for the single-balanced mixer. 3–4-dB deviation between the simulated and measured results might be because that the large-signal model of the transistor is not accurate enough.

In order to evaluate the NF of the resistive mixers, a novel method is proposed and evaluated in this paper. This method is suitable for moderate-to-high NF circuits operating beyond 100 GHz, where commercial noise sources are difficult to find and the Y-factor is small with loads at 77/295 K. Using the signal generator $N$-times power method, the calculated results show that the NF of the single-ended mixer is around 1.0 dB higher than its conversion loss, and the NF of the single-balanced mixer is about 1.6 dB higher than its conversion loss.

### APPENDIX

#### SIGNAL GENERATOR $N$-TIMES POWER METHOD

The NF is an important factor when evaluating the performance of a communication system. The Y-factor method is commonly used by commercial noise figure analyzers (NFAs) [25], where abundant noise power coming from a noise source serves as the hot load and a matched load at room temperature (295 K) serves as the cold load. As frequency increases beyond 100 GHz, a matched load under room temperature and liquid nitrogen (77 K) are usually chosen as the hot load and cold load, respectively [2]. For a high NF system, the Y-factor will be very small, and thus difficult to measure accurately. On the contrary, the signal generator twice-power method [26] is useful for devices with high NF. The output power is firstly measured when the input is terminated with a matched load at room temperature. A CW signal generator is then connected and its power ($P_{gen}$) is adjusted to produce a 3-dB increase at the output. An accurate measurement of $P_{gen}$ is the most critical and error prone part of this method. As the CW input frequency increasing above 100 GHz, the $P_{gen}$, which results in only 3-dB increases at the output, could be difficult to measure.
accurately depending on the dynamic range of the power meter. Therefore, a more accurate measurement will be achieved if a higher \( P_{\text{gen}} \) can be applied. Based on the signal generator twice-power method, we propose the signal generator \( N \)-times power method.

Referring to Fig. 17, \( T_0 = 295 \) K is room temperature, assuming the device-under-test (DUT) has a bandwidth of \( B \) Hz and a linear gain of \( G \). We assume the DUT has an equivalent noise temperature of \( T_{\text{sys}} \) (which is unknown). The input is first terminated by a load at the room temperature \( T_0 \), and the output power is measured to be \( P_1 \). According to noise power definition [27],

\[
P_1 = k \cdot (T_0 + T_{\text{sys}}) \cdot B \cdot G
\]

where \( k = 1.38 \times 10^{-23} \) is the Boltzmann constant.

Next, a CW signal generator is connected to the input port, where the CW signal should be within the bandwidth of the DUT. With an input power of \( P_{\text{gen}} \), an output power of \( P_2 \) is obtained, where \( P_2 \) is the mix of noise power and amplified CW signal. It can be written as

\[
P_2 = k \cdot (T_0 + T_{\text{sys}}) \cdot B \cdot G + P_{\text{gen}} \cdot G.
\]

By dividing (5) by (4), we will achieve

\[
T_{\text{sys}} = \frac{P_{\text{gen}}}{k \cdot B \cdot (N - 1)} - T_0
\]

where \( N = P_2/P_1 \) is the ratio of the measured power in the two cases.

The noise factor now becomes

\[
F_{\text{sys}} = 1 + \frac{T_{\text{sys}}}{T_0} = \frac{P_{\text{gen}}}{k \cdot T_0 \cdot B \cdot (N - 1)}.
\]

According to (7), the gain is not needed to determine \( F_{\text{sys}} \), but the noise bandwidth, \( B \), must be known. Practically speaking, bandwidth can be confined by a bandpass filter (BPF) connected before the power meter. The value of \( B \) should be a calculated equivalent noise bandwidth with rectangular and “flat-top” frequency response spectral. Fig. 18 shows one way to determine the equivalent noise bandwidth. The input of the IF chain is terminated with a 50-Ω load at room temperature. The output power, \( P_N \), is measured by the power meter and can be expressed as

\[
P_N = k \cdot (T_0 + T_{\text{tot}}) \cdot B \cdot G_{\text{tot}}
\]

where the IF gain \( G_{\text{tot}} \) and the noise temperature \( T_{\text{tot}} \) are obtained from a separate calibration with the NFA. The equivalent noise bandwidth is then

\[
B = \frac{P_N}{k \cdot (T_0 + T_{\text{tot}}) \cdot G_{\text{tot}}}.
\]

Three simple networks have been characterized by the proposed method and by a commercial NFA (Agilent N8975A) as an experimental validation. As is shown in Fig. 19, network (a) has been used to apply low NF (<5 dB) and (b) with moderate NF (5–10 dB) and high NF (>10 dB) for network (c). NF at 14.25 GHz., which is the center frequency of the BPF, is evaluated by the signal generator \( N \)-times power method at different ratio \( N \). As can be seen from Fig. 20, results obtained by the signal generator \( N \)-times power method coincide very well with the ones measured by the commercial NFA.
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REFERENCES


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Paper C

340 GHz Integrated Receiver in 250 nm InP DHBT Technology

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340 GHz Integrated Receiver in 250 nm InP DHBT Technology

Yu Yan, Yogesh B. Karandikar, Student Member, IEEE, Sten E. Gunnarsson, Member, IEEE, Miguel Urteaga, Member, IEEE, Richard Pierson, and Herbert Zirath, Fellow, IEEE

Abstract—A 340 GHz integrated receiver based on a 250 nm InP DHBT technology is presented in this paper. It consists of a 2×2 differential patch array antenna, a sub-harmonically pumped Gilbert mixer and an IF buffer amplifier. Performance of the integrated receiver is evaluated by setting up a RF link in the frequency band of 302–338 GHz. At 338 GHz RF and 170 GHz LO, the peak conversion gain of 11.8 and 14.0 dB is achieved with and without antenna, respectively. A double-sideband noise figure of 17 dB at room temperature is obtained from direct noise figure measurement.

Index Terms—340 GHz, terahertz (THz), sub-millimeter wave, receiver, Gilbert cell mixer, down-converter, sub-harmonic mixer, differential amplifier, differential patch antenna, InP double-heterojunction transistor (DHBT), terahertz monolithic integrated circuits (TMICs).

I. INTRODUCTION

SPECTROSCOPIC detection has long been developed and applied in fields such as physics, chemistry, biology, medicine, and materials science. The growing terror threats led to a considerable amount of research for the detection of concealed weapons and hidden explosives. Traditional imaging techniques utilizing acoustic waves, microwave, infrared, or X-ray are not suitable for applications where the requirements include high spatial resolution, fast operation, and safety concern for persons being screened [1]. Terahertz (THz) spectra (0.3–3 THz) have the unique properties of both penetration and non-ionizing radiation. Besides, the spectral content of reflected/transmitted signals offers the capability of identifying certain hidden substances from their characteristic spectra [2]. This further boosts the research activities on THz imaging technologies. However, a combined effect from absorptions, distortions, attenuation and the relative weakness of spectral features in the reflection make the THz spectroscopy difficult to use in practical applications. At the expense of lower specificity, the lower end of the THz frequency range seems more promising for security application [1].

In a real imaging system, a receiver, which should at least include an antenna and a down converter, is an essential part for either a transmission-mode or a reflection-mode system. In the THz regimes, two terminal devices such as Schottky diodes incorporated with waveguide technology used to be the only accessible solution for the frequency converter [3]–[5]. Then, the continuously development of semiconductor manufacturing technologies open up opportunities for monolithic integrated circuits into the THz range [6]–[9]. In the last few years, indium phosphide (InP)-based high electron mobility transistors (HEMTs) and heterojunction bipolar transistors (HBTs) have reported the highest transistor bandwidth, with current gain cutoff frequency ($f_t$) and power gain cutoff frequency ($f_{max}$) approaching or exceeding 1 THz [10]–[12]. These further encourage the terahertz monolithic integrated circuits (TMICs) design where multiple functions could be incorporated on a single chip [13].

The first FET-based down-conversion mixer working up to 300 GHz was reported in a 50 nm metamorphic HEMT (mHEMT) technology [14], and the same topology has been further used in the integrated receivers [15], [16]. Silicon technology is well known for its low-cost but III-V technology outperforms Si-based one in terms of noise. A silicon-germanium (SiGe)-based 650 GHz receiver front-end was reported in [6]. Suffered from the limited $f_t$ and $f_{max}$, fourth-harmonic mixer was used with the cost of lower conversion gain ($G_c$) and increased noise figure (NF). Recently, a series of single-balanced mixers sharing the same topology in InP HBT technology are reported up to 0.57 THz mainly to facilitate their oscillator measurement [17].

In this paper, a 340 GHz integrated receiver in InP double-heterojunction transistor (DHBT) technology has been designed and characterized. It incorporates a 2×2 differential patch array antenna, a sub-harmonically pumped mixer (SHM) and a differential IF buffer amplifier. Even though a 324 GHz amplifier has been demonstrated in the same technology [18], considering the bandwidth and frequency shift compared to simulations, the RF LNA is omitted in the initial integrated receiver design. The paper is organized as follows: First, the 250 nm InP DHBT technology is introduced in Section II. Subsequently, in Section III to Section VI, the design of the SHM, IF amplifier, the patch antenna and the integrated receiver are described, respectively. Then the measurement setup together with the measured results is presented in Section VII, and the comparison to
the state-of-the-art works in these frequency bands is shown in Section VIII.

II. TECHNOLOGY

InP DHBTs offer high transistor bandwidth with high voltage handling due to the use of a wide bandgap InP collector. In this work, an InP DHBT technology with a nominal emitter junction width of 250 nm was utilized. Details of the HBT process can be found in [7]. Key features of the technology include the use of electron beam lithography and electroplating to form the emitter contact and the use of dielectric sidewall spacers to form a self-aligned base-emitter junction. Fig. 1 shows a representative cross-section of the given HBT IC process. It includes thin-film resistors (50 Ω/sq), metal-insulator-metal (MIM) capacitors, and 4-levels of interconnect (MET1-MET4). A benzo-cyclobutene (BCB) spin-on-dielectric is used as the interlayer dielectric (ILD) with 1 μm ILD spacing between each metal layer. The BCB has a low dielectric constant of εr ~ 2.7. Electroplated Au-based interconnects are used for the metallization layers, with 1 μm thick layers used for MET1-MET3 and a 3 μm thick MET4.

Fabricated transistors exhibit a typical DC current gain (β) of around 25 and a common-emitter breakdown voltage (BVCEO) of >4 V. Transistor S-parameter characterization is performed on wafer from 1–50 GHz. RF figures-of-merit are extracted from single-pole fits to the measurements of transistor current gain (h21) and unilateral power gain (U) for fT and fMAX, respectively. A typical 4 × 0.25 μm² HBT demonstrates a current gain cutoff frequency (fT) of 375 GHz and a maximum frequency of oscillation (fMAX) of 650 GHz, at IC = 9 mA and VCE = 1.8 V. Models based on the Agilent HBT model [19] have been developed to accurately describe the unique characteristics of III-V bipolar devices. The model includes all relevant transistor parasitic elements and should scale well to frequencies approaching the transistor cut-off frequencies.

III. 340 GHZ SUB-HARMONIC GILBERT-MIXER DESIGN

Monolithically integrated mixers operating above 100 GHz has been well proved in HEMT technology. Topologies vary from diode mixers, resistive mixers, and dual gate mixers to drain mixers [20]–[23]. In HBT technology, Gilbert-cell mixer is popular for its excellent performance [24]. As the frequency increasing into millimeter/sub-millimeter wave frequency ranges, sufficient high LO power is a challenging issue. Therefore, sub-harmonically pumped mixer (SHM) is especially interesting because the LO frequency is only half of the frequency needed for fundamentally pumped type.

A. Sub-Harmonically Pumped Mixer Core

In this work, the sub-harmonically pumped Gilbert mixer with leveled-LO configuration is adopted due to its higher operating frequency compared to the stacked-LO configuration [25]. Fig. 2 shows a simplified schematic of the sub-harmonic mixer. The working bandwidth of the mixer core mainly depends on the transistor’s speed. In this work, the smallest available transistor (0.25 × 3 μm²) is chosen for Q1–Q10 to achieve as high as 340 GHz operating frequency.

As can be seen from Fig. 2, the circuit consists of four cross-connected transistor pairs at upper-level and one transistor pair at lower-level. The current passing through the two levels is applied and controlled by a current mirror [26] at the bottom of the circuit. The lower-level transistor pair (Q1 and Q2) performs as a transconductance amplifier for the differential RF signals while the upper-level transistor pairs (Q3–Q10) operate as switches. By pumping with sufficient LO power with quadrature phases, the upper level transistors will be turned “on” and “off” alternately over one LO cycle. Due to the symmetrical structure, the emitters of Q3–Q10 are virtual ground for the LO signal such that no LO voltage will exist on the collectors of Q1 and Q2. As a result, an intrinsic LO-to-RF isolation can be obtained over a broad bandwidth. In addition, the outputs from the upper-level transistors are cross-connected to cancel the dominant spurious noise.
frequencies, such as $f_{LO}$ (fundamental LO), $f_{RF}, f_{RF} \pm f_{LO}$ and $f_{RF} \pm 3f_{LO}$. Then, the desired IF outputs $f_{RF} - 2f_{LO}$ are combined in-phase.

### B. Quadrature-Phase LO Generator

In this work, the differential RF will be fed from a differential patch antenna directly and this will be discussed in Section VI. The quadrature-phase LO should be generated from a single-ended input and this is often realized by a polyphase filter [27]. However, the simulated result of a 170 GHz single-stage polyphase filter indicates an insertion loss of more than 5 dB from each port. Considering the difficulty of getting power at such high frequency, a simple combination of a Marchand balun [28] followed by two branch-line hybrid [29] is utilized as is shown in Fig. 3. Enhanced coupling in the Marchand balun is achieved by overlapping the coupled lines on two different metal layers (MET3 and MET4). Fig. 4 shows the simulated results of the quadrature-phase LO generator. It achieves better than 2 dB insertion loss (apart from the ideal 6 dB of power division) from each port at the frequencies ranging from 157 GHz to 188 GHz, while the amplitude imbalance and phase imbalance are better than 0.5 dB and 5 deg, respectively.

### C. Integration

For the mixer core in Fig. 2, both amplitude and phase balance plays a critical role in its performance. At 170 GHz, the phase shift is very sensitive to the length of the transmission line (e.g., at 170 GHz, 20 $\mu$m of transmission line gives 6$^\circ$ phase shift in this process). In order to guarantee the quadrature-phase LO, upper-level transistors are arranged carefully and the length of feeding TLs are calculated to be as equal as possible. Simultaneously, each input of the upper-level transistors in Fig. 2 is matched to the quadrature-phase generator by a single open stub. For the given process, four metal layers enable a more flexible design. MET2 is designated as ground in this work while MET1, MET3, and MET4 can be manipulated for TLs. In the

### IV. Differential IF Buffer Amplifier Design

In a real receiver system, a good RF LNA is always preferred to improve the system noise figure as well as applying certain gain. However, it is challenging to design a good LNA at frequencies as high as 340 GHz. Hence, the RF LNA is omitted in this work, and a differential buffer amplifier is designed for the IF amplification [26], as is shown in Fig. 5. The transistor pair Q3 and Q4 is the core for power amplification, and both transistors are biased under the class-A condition. The emitter follower consists of Q5 or Q6 with a 50 $\Omega$ resistor (R1) at its base helps the input match, and the one formed by Q5 or Q6 improves the output match. In the simulation, a maximum gain

of around 25 dB is achieved at 2 GHz and it decreases to 16 dB at 20 GHz. For simplicity, no additional matching or feedback techniques were used for bandwidth optimization in this initial design.

V. DIFFERENTIAL 2×2 PATCH ARRAY ANTENNA DESIGN

As discussed in Section III, the sub-harmonically pumped Gilbert mixer used in this design has differential RF input. Hence, for a compact design if an antenna also has differential output, the integration of mixer with antenna would be easier, and it would eliminate the need of the RF balun. Also considering the MMIC layer topology, as shown in Fig. 1, only planar antennas are feasible utilizing MET3 or MET4. Thus for simplicity, a planar patch antenna with microstrip based feed network is considered [30], and MET2 is chosen as the ground to be consistent with the rest of the circuit design.

The efficiency of patch antennas is proportional to the dielectric thickness, hence for maximum dielectric thickness of BCB layer, MET4 is used for patch array along with its microstrip feed network. The microstrip based patch antenna usually utilizes the corporate feeding network and has unbalanced output, as shown in Fig. 6(a). For an array of such patches, to maximize the directivity, all the elements must be fed in phase. In this work, a 2×2 patch array with a modified feeding network is designed, as shown in Fig. 6(b), to obtain a differential signal at the output for broadside beam direction. To get out-of-phase signals at two output ports, one arm of the array (consisting 2×1 patches) is rotated by 180°. In this way, current on the microstrip
line stays out-of-phase for all frequencies but the array pattern keeps its maximum in the broadside direction.

Both the analytical beam pattern and the CST MWS\(^2\) simulated pattern are shown in Fig. 7 for comparison. The directivity along with radiation efficiency \(\eta_{\text{rad}}\) is shown in Fig. 8. Due to limited dielectric thickness (3 \(\mu\)m), the \(\eta_{\text{rad}}\) of this antenna is poor, but it can be strongly improved with a thicker substrate. For improved matching, double balanced stubs are used as shown in Fig. 6, and the simulation result indicates a \(-10\) dB input reflection coefficient from 336 GHz to 358 GHz referred to a port impedance of 70 \(\Omega\).

VI. INTEGRATED RECEIVER

Fig. 9 shows the block diagram of the 340 GHz integrated receiver. Single-ended LO port and differential IF ports are designed with on-wafer pads. The RF port of the mixer is fed by the differential 2\(\times\)2 patch array antenna followed by a matching network which transforms the line impedance from 70 to 50 \(\Omega\). Fig. 10 shows the chip photo of the integrated receiver. A coplanar waveguide structure is used for both LO and IF pads which enable the on-wafer probing measurement. The whole chip occupies an area of 1680\(\times\)1840 \(\mu\)m\(^2\) and consumes 472 mW DC power out of which 55 mW is consumed by the mixer.

VII. CHARACTERIZATION

A. Measurement Setup

In order to measure the integrated receiver with antenna on chip, a complete transmitter/receiver (T/R) link is setup, as shown in Fig. 11. Fig. 12 shows the photo of the measurement setup. The receiver chip is located at the bottom with the patch array antenna facing upwards. The LO signal is pumped in by using a D-band on-wafer ground-signal-ground (GSG) probe. The LO chain consists of a cascade connected signal generator, W-band source module, W-band power amplifier (PA) and a WR-5.1 frequency doubler. The multiplier chain covers the frequency range from 150 to 220 GHz. However, due to the standing wave between PA and the last doubler, the available output power varies significantly as a function of frequency. Hence, fixed LO frequencies at 160 and 170 GHz are chosen to offer several dBm measured power. The transmitter chain is built up in a similar way up to 340 GHz. A WR-03 conical
horn is connected to illuminate the on-chip antenna with RF signals. The output power of the transmitter varies significantly due to standing waves between the modules. But, considering that the performance of a mixer does not depend on the RF power as long as it is not saturated, such power variation could be calibrated, and a RF sweep measurement is possible.

The alignment of the two antennas is also a critical issue. In this measurement setup, the receiver chip is glued on the bottom plate. The transmitter part except for the signal generator is mounted on an x-y scanner and then fixed on the top plate, as shown in Fig. 11. The top plate can move along x-axis in a large range and the fine-tuning x-y scanner eventually aligns the transmitter horn by detecting the maximum IF power.

B. Conversion Gain Characterization

The conversion gain of the receiver \( G_{RX} \) incorporates the conversion gain of mixer, the gain from IF buffer amplifier and the antenna gain referred to an isotropic antenna. Since the breakout patch array antenna is not available for measurement, the patch array antenna gain \( G_p \) is based on the simulation results in Fig. 8, and can be calculated by \( D_0 + \eta_{rad} \) in dB. In a link budget, similar to [31], the \( G_{RX} \) is derived from one of the two IF output ports while the other one is terminated with a 50 \( \Omega \) load. It can be expressed as

\[
G_{RX} = P_{IF} - G_{LNA} + L_{cable} + L_{probe} + FSL - G_t - P_t \tag{1}
\]

where

- \( P_{IF} \) measured IF power in dBm;
- \( G_{LNA} \) gain of the IF LNA in dB;
- \( L_{cable} \) IF cable loss in dB;
- \( L_{probe} \) IF probe loss in dB;
- \( FSL \) Free-Space Loss = \( 20 \cdot \log((4\pi d)/\lambda) \) in dB, where \( d \) is the distance between the two antenna;
- \( G_t \) gain of the conical horn in dB;
- \( P_t \) transmitted power before the conical horn in dB.

By excluding the on-chip antenna gain \( G_p \) from \( G_{RX} \), the conversion gain of the down-converter circuit alone \( G_{circuit} \) is also an interesting parameter and it can be calculated by

\[
G_{circuit} = G_{RX} - G_p \tag{2}
\]

Fig. 13 shows the \( G_{circuit} \) as a function of the on-chip LO power (probe loss has been removed). The maximum available LO power is limited to 4 dBm. Below the maximum available LO power, the measured result agrees well with the simulated curve. Therefore, the LO saturation power in this work is around 10 dBm from the simulated result.

Limited by the measurement setup, the RF signal can only sweep up to 340 GHz. Therefore, double sideband performance at 160 GHz LO and the lower sideband performance at 170 GHz LO, with a maximum available LO power of \( \sim 4 \) dBm on-chip applied, are measured, as shown in Figs. 14 and 15, respectively. A peak \( G_{RX} \) of 11.8 dB and a peak \( G_{circuit} \) of 14.0 dB is measured at 338 GHz RF and 170 GHz LO. As is discussed in Section IV, the gain slope mainly due to the IF buffer amplifier.

At 160 GHz LO, the combined IF is also measured by using an external balun. However, as can be seen from Fig. 16,
TABLE I
COMPARISON TO RELATED WORKS

<table>
<thead>
<tr>
<th>f&lt;sub&gt;LO&lt;/sub&gt;</th>
<th>LO harmonic</th>
<th>G&lt;sub&gt;c,LO&lt;/sub&gt; (dB)</th>
<th>G&lt;sub&gt;c&lt;/sub&gt; (dB)</th>
<th>NF (dB)</th>
<th>Amplifier</th>
<th>Antenna Topology</th>
<th>DC (nW)</th>
<th>Technology</th>
<th>Ref</th>
</tr>
</thead>
<tbody>
<tr>
<td>170</td>
<td>1</td>
<td>-30</td>
<td>-6</td>
<td>21</td>
<td>RF LNA</td>
<td>Tapered Dipole (with metal fill)</td>
<td>800</td>
<td>120 nm SiGe BiCMOS HBT</td>
<td>[33]</td>
</tr>
<tr>
<td>200</td>
<td>1</td>
<td>15.4</td>
<td>-8</td>
<td>9</td>
<td>-</td>
<td>Double-slot on Si lens</td>
<td>0</td>
<td>100 nm GaAs mHEMT</td>
<td>[31]</td>
</tr>
<tr>
<td>200</td>
<td>1</td>
<td>11.2</td>
<td>-12.2</td>
<td>13.8</td>
<td>-</td>
<td>Double-slot on Si lens</td>
<td>0</td>
<td>100 nm GaAs mHEMT</td>
<td>[31]</td>
</tr>
<tr>
<td>220</td>
<td>2</td>
<td>-</td>
<td>2</td>
<td>8.4</td>
<td>RF LNA</td>
<td>Square Slot on Si lens</td>
<td>40</td>
<td>100 nm GaAs mHEMT</td>
<td>[34]</td>
</tr>
<tr>
<td>220</td>
<td>4 (Doubler + SHM)</td>
<td>-</td>
<td>3.5</td>
<td>7.4</td>
<td>RF LNA</td>
<td>Square Slot on Si lens</td>
<td>110</td>
<td>100 nm GaAs mHEMT</td>
<td>[35]</td>
</tr>
<tr>
<td>338</td>
<td>2</td>
<td>11.8</td>
<td>14</td>
<td>17</td>
<td>IF buffer</td>
<td>2×2 patch array</td>
<td>472</td>
<td>250 nm InP DHBT</td>
<td>This work</td>
</tr>
<tr>
<td>650</td>
<td>4</td>
<td>-13</td>
<td>-</td>
<td>42</td>
<td>IF buffer</td>
<td>Folded Dipole</td>
<td>433</td>
<td>130 nm SiGeC BiCMOS HBT</td>
<td>[6]</td>
</tr>
<tr>
<td>823</td>
<td>5</td>
<td>-22</td>
<td>-</td>
<td>47</td>
<td>IF buffer</td>
<td>2×2 patch array</td>
<td>1200</td>
<td>250 nm SiGe BiCMOS HBT</td>
<td>[8]</td>
</tr>
</tbody>
</table>

G<sub>c,LO</sub> is the gain of the receiver circuit together with the antenna gain referred to an isotropic antenna.

C. Double-Sideband Noise Figure (DSB-NF) Characterization

In this work, double-sideband noise figure (DSB NF) of the receiver is calculated from the direct noise power measurement [32]. Fig. 17 shows the noise measurement setup. The receiver chip is biased under the same condition as a working receiver. The 170 GHz LO signal is applied but without RF signal fed in. The output noise power at a certain IF frequency is measured by the spectral analyzer and it can be expressed by

\[ P_{N,LO} = k(T_0 + T_{N,LO})BG_{tot} \]  

where

\[ k = 1.38 \times 10^{-23} \text{ J/K} \] is the Boltzmann constant;

\[ T_0 = 290 \] K is the standard room temperature;

\[ T_{N,LO} \] noise temperature of the receiver circuit (excluding the patch array antenna) together with the IF chain;

\[ B \] equivalent noise bandwidth;

\[ G_{tot} \] gain of the receiver circuit (\( G_{c, circuit} \)) together with the IF chain;

As the measured \( G_{c, circuit} \) agrees well with the simulated results from Fig. 14, the simulated \( G_{c, circuit} \) is utilized to calculate \( G_{tot} \) in (3). In this measurement, an equivalent noise bandwidth of 100 kHz is confined by the resolution bandwidth of the spectral analyzer. In addition, the patch array antenna is a pure passive structure, so the noise temperature at the antenna port (or the input of the mixer) should be \( T_0 \). By using the Friis formula, the noise figure of the integrated receiver circuit (\( NF_{receiver} \)) can be calculated from \( T_{N,LO} \). Fig. 18 shows the estimated \( NF_{receiver} \) referred to the input of the mixer. An average DSB NF of around 17 dB is achieved.
VIII. COMPARISON TO RELATED WORK

Table I compares the performance of the presented receiver to other related work. As can be seen from the table, III-V based HEMT technology is still dominant at sub-millimeter wave range due to its simplicity and more matured processes. Si-based HBT technology is working towards THz, but improved noise performance could be a long lasting challenge. In InP-based HBT technology, the presented work achieves very good conversion gain and noise figure considering the RF frequency. To further improve the NF, the integration with RF LNA and LO multiplier chain is being developed for the next generation.

IX. CONCLUSION

In this paper, a 340 GHz monolithically integrated receiver based on a 250 nm InP DHBT technology is presented. It incorporates a 2×2 differential patch array antenna, a sub-harmonically pumped Gilbert mixer and a differential IF buffer amplifier. The performance of the integrated receiver is evaluated by setting up a RF link. Conversion gain over the RF frequencies from 302 to 338 GHz is characterized and it agrees well with the simulation. The integrated receiver achieves a peak gain of $G_{RX}$ of 11.8 dB at 338 GHz RF and 170 GHz LO while the circuit gain ($G_{circuit}$) alone is 14.0 dB. By using the direct NF measurement method, a DSB NF of around 17 dB is obtained for the receiver circuit.

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REFERENCES

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Paper D

A 110-170-GHz Multi-Mode Transconductance Mixer in 250-nm InP DHBT Technology

Y. Yan, M. Bao, S. E. Gunnarsson, V. Vassilev, and H. Zirath

A 110–170-GHz Multi-Mode Transconductance Mixer in 250-nm InP DHBT Technology

Yu Yan, Student Member, IEEE, Mingquan Bao, Sten E. Gunnarsson, Member, IEEE, Vessen Vassilev, and Herbert Zirath, Fellow, IEEE

Abstract—A novel full D-band (110–170 GHz) multi-mode transconductance down-converter mixer is realized in a 250-nm indium–phosphide double heterojunction bipolar transistor technology. A single-balanced topology is chosen and an active power combiner for the RF and the local oscillator (LO) signals’ combination is used. The designed mixer is feasible to work at \( x \times 1, x \times 2, x \times 3, x \times 4 \) subharmonically LO-pumped mixing modes with relatively low LO powers of \( 0, -1, 5, \) and \( 6 \) dBm, respectively. The measured conversion gain achieves typical values of \(-3, -1, -5, \) and \(-4 \) dB over the full D-band while the best noise figures of \( 12, 13.5, 18.5, \) and \( 19 \) dB are obtained, respectively. Through the multi-mode operation in terms of subharmonic LO-pump-frequency, the designer can make a tradeoff between LO frequency, LO power, and noise figure.

Index Terms—Conversion gain, D-band, double heterojunction bipolar transistor (DHBT), millimeter wave, monolithic microwave integrated circuit (MMIC), multi-mode, noise figure, 110–170 GHz, sub-harmonic mixer, transconductance mixer, 250 nm.

I. INTRODUCTION

The frequencies below 100 GHz have been well explored over the last century. In recent years, a drastic increase in the demand for data rate pushes the frequencies of interest above 100 GHz, where a wider bandwidth can be utilized and higher data rate would be achieved consequently.

A down-converter mixer is a key component in a receiver front-end. A subharmonically pumped mixer is an attractive solution in millimeter- and submillimeter-wave receivers due to the fact that one or more frequency multipliers can be omitted in the local oscillator (LO) frequency multiplier chain, thereby saving chip area and reducing power consumption. Subharmonically pumped resistive mixers, based on high electron-mobility transistors (HEMTs), have been studied and reported extensively including single device [1], [2], dual devices [2]–[6], and quad devices [7], up to 220 GHz. Subharmonic millimeter-wave antenna integrated HEMT mixers are reported in [8] and [9].

A CMOS-based dual device subharmonically pumped mixer is reported in [10]. In bipolar transistor technologies, the Gilbert mixer is commonly used in a fundamentally pumped mode or second harmonically pumped mode [11]–[14]. For mixers that are designed to operate approaching or exceeding the cutoff frequency of given transistors, a higher order (greater than 2) of the subharmonically pumped transconductance mixer is a good solution [15]–[17].

The noise figure is an important factor from a system perspective. Since the noise of a mixer consists of the internal noise generated by the mixer device itself and the noise converted from all the harmonics’ ports, by increasing the order of the harmonic mixing mode, the LO frequency can be decreased with the tradeoff of higher noise figure. Therefore, a multi-mode mixer, which supports different orders of sub-harmonic operation, allows higher flexibility in a system design. For instance, if low noise is the most important requirement, the fundamental or \( x \times 2 \) harmonic mixing mode should be used, and if small chip size and low dc power consumption of the overall front-end is more important, higher harmonic mixing modes is a good choice.

In this paper, a full D-band transconductance mixer is designed in a 250-nm indium–phosphide (InP) double heterojunction bipolar transistor (DHBT) technology. The mixer is characterized at the \( x \times 1, x \times 2, x \times 3, \) and \( x \times 4 \) subharmonically pumped mixing modes. In Section II, the mechanism of a sub-harmonically pumped transconductance mixer is described in order to understand how the mixer should be biased at different harmonic mixing modes. Sections III and IV present the mixer design and characterization, respectively. Finally, a conclusion and comparison are given in Sections V.

II. PRINCIPLE OF SUB-HARMONIC TRANSCONDUCTANCE MIXER

The principle of a fundamentally pumped transconductance mixer has been well described in [18] and [19]. Aiming for the maximum conversion gain, the base–emitter junction is biased around the turn-on voltage (\( V_T \)) and a 50% duty-cycle of the transconductance waveform is obtained. In this section, an extended analysis is carried out based on a simplified small-signal model, aiming to get some physical understanding on the optimal transconductance waveform and base bias at different harmonic mixing modes.
Fig. 1 shows the simplified schematic of a single-ended transconductance mixer. $V_b$ and $V_c$ denote the dc bias voltages at the base and the collector, respectively. The RF and LO signals are applied at the base of the transistor through a power combiner, while the IF output is extracted from the collector.

Fig. 2 shows the simplified small-signal equivalent circuit of a bipolar transconductance mixer. Normally, $r_\pi$ is large and can be neglected compared to the reactance of $C_\pi$. Assume the input is conjugate matched, and both input and output are properly terminated such that all unwanted frequency components are short-circuited. Thus,

$$\text{Re}\{Z_S\} = r_b.$$  

(1)

Therefore, the intrinsic base–emitter voltage $v_1$ from LO and RF supplies can be expressed as

$$v_{1,\text{LO}} = \frac{I_{\text{LO}}(t)}{\omega_{\text{LO}} C_\pi} = \frac{V_{\text{LO}} \cos(\omega_{\text{LO}} t)}{2 \omega_{\text{LO}} C_\pi r_b},$$

(2)

$$v_{1,\text{RF}} = \frac{I_{\text{RF}}(t)}{\omega_{\text{RF}} C_\pi} = \frac{V_{\text{RF}} \cos(\omega_{\text{RF}} t)}{2 \omega_{\text{RF}} C_\pi r_b}.$$  

(3)

Assume the transistor can be ideally switched where its transconductance ($g_m$) is shown in Fig. 3(a). Applying a large LO signal swing, a switched waveform is generated, as is shown in Fig. 3(b). It has a duty-cycle of $\alpha$. By expanding the $g_m$ waveform into Fourier series, it can be expressed as

$$g_m = g_0 + \sum_{n=1}^{\infty} g_n \cos(n \omega_{\text{LO}} t)$$

(4)

where

$$g_c = g_{\text{max}} \cdot \alpha$$

(5)

$$g_n = \frac{2g_{\text{max}}}{n\pi} \sin(n\pi \alpha).$$

(6)

The coefficient $g_n$ represents the equivalent transconductance at the $n$th harmonic of the applied LO frequency.

Normally, the RF is a small signal so the current at the collector is

$$i_c = g_m \times v_{1,\text{RF}}$$

$$= g_0 \cdot \frac{V_{\text{RF}} \cos(\omega_{\text{RF}} t)}{2 \omega_{\text{RF}} C_\pi r_b} \sum_{n=1}^{\infty} g_n \cos(n \omega_{\text{LO}} t) \frac{V_{\text{RF}} \cos(\omega_{\text{RF}} t)}{2 \omega_{\text{RF}} C_\pi r_b}$$

$$- g_0 \cdot \frac{V_{\text{RF}} \cos(\omega_{\text{RF}} t)}{2 \omega_{\text{RF}} C_\pi r_b} \sum_{n=1}^{\infty} g_n \cos(n \omega_{\text{LO}} - \omega_{\text{RF}}) t$$

$$+ \frac{V_{\text{RF}}}{4 \omega_{\text{RF}} C_\pi r_b} \sum_{n=1}^{\infty} g_n \cos(n \omega_{\text{LO}} + \omega_{\text{RF}}) t.$$

(7)
Thus, the magnitude of the IF current for the $\times n$-harmonic mixer is

$$i_{IF} = \frac{V_{IF}}{4\omega_{RF}C_r r_b} \cdot g_n.$$  \hspace{1cm} (8)

Substitute (6) into (8),

$$i_{IF} = \frac{V_{IF}}{2n\pi\omega_{RF}C_r r_b} \cdot g_{max} \cdot \sin(n\pi\alpha).$$  \hspace{1cm} (9)

The IF output power will be

$$P_{IF} = \frac{1}{2}I_{IF}^2R_L = \frac{(V_{IF} \cdot g_{max})^2}{8(n\pi\omega_{RF}C_r r_b)^2} \cdot \sin^2(n\pi\alpha) \cdot R_L.$$  \hspace{1cm} (10)

The available RF power from the source is

$$P_{RF} = \frac{V_{RF}^2}{8r_b}.$$ \hspace{1cm} (11)

The conversion gain of a $\times n$-harmonic mixer can hence be determined by

$$G_c = \frac{P_{IF}}{P_{RF}} = \left[ \frac{g_{max} \cdot \sin(n\pi\alpha)}{n\pi\omega_{RF}C_r} \right]^2 \cdot \frac{R_L}{r_b}.$$  \hspace{1cm} (12)

The optimal duty-cycle of the $g_m$ waveform that maximizes the conversion gain can also be obtained when

$$\sin(n\pi\alpha) = 1.$$  \hspace{1cm} (13)

Fig. 4 (top) shows the numerically calculated conversion gain, which is normalized to the peak conversion gain at the fundamental mixing mode, as a function of the duty-cycle ($\alpha$) according to (12), where $g_{max}$, $C_r$, $R_L$, and $r_b$ are assumed to be constant. The verification is carried out in Agilent Technologies’ Advanced Design System (ADS) simulation referred to a single-ended transconductance mixer in Fig. 1. A transistor model from the given Teledyne 250-nm InP DHBT technology is used. In order to obtain an ideally switched $g_m$ waveform, the LO is applied by an ideal pulse wave source. Thus, the duty-cycle of the $g_m$ waveform can be controlled directly by the duty-cycle of the LO pulse wave. The simulation result is shown in Fig. 4 (bottom), where the conversion gain is also normalized to the peak conversion gain at fundamental mixing mode. It agrees well with the analytical curves in Fig. 4 (top) regarding the peak conversion gain in relative scale and the correspondent duty-cycle at different harmonic mixing modes. For a subharmonically pumped mixing mode in Fig. 4, we can see that the number of the conversion gain peaks is equal to the order of the harmonic mixing mode. Since the first peak corresponds to the shortest conducting time of a transistor, lowest shot noise will be generated. Therefore, the first gain peak is more interested for each harmonic mixing mode, and the correspondent duty-cycle can be found from the first root of (13),

$$n\pi\alpha = \frac{\pi}{2}.$$  \hspace{1cm} (14)

Thus,

$$\alpha = \frac{1}{2n}.$$  \hspace{1cm} (15)

In reality, the LO is typically a sinusoidal wave. Hence, the duty-cycle of the $g_m$ waveform can be controlled by properly choosing the dc bias $V_b$. As can be seen from Fig. 3(b), as $V_b$ is decreased, the duty-cycle of the $g_m$ waveform is reduced. Therefore, the higher order of the harmonic mixing mode, the lower base bias should be chosen. In addition, the transconductance of a transistor is not ideally switched but with a certain slope. Thus, the LO power typically needs to be increased to drive the transistor efficiently and speed up the switching when the base bias is lower. Generally speaking, if the transconductance mixer is designed for a higher order of harmonic mixing mode, the optimal base bias should be lower and the driving LO power should be higher.

### III. MIXER DESIGN

In this work, a transconductance down-converter mixer is designed for 110–170-GHz RF and is intended to be characterized in $\times 1$, $\times 2$, $\times 3$, and $\times 4$ LO mixing modes. The mixer is fabricated in a 250-nm InP DHBT technology, which includes four metal layers. A 4 $\mu$m $\times$ 0.25 $\mu$m HBT, from the given process, demonstrates a current gain cutoff frequency ($f_{CE}$) of 375 GHz and a maximum frequency of oscillation ($f_{max}$) greater than 650 GHz. Details of the technology can be found in [20].

Aiming for low IF frequency applications, a single-balanced topology is used to suppress the second-order intermodulation (IM2). The schematic is shown in Fig. 5. Two identical branches are fed with in-phase LO and differential RF signals. The two IF outputs are out-of-phase and can be combined by an off-
chip balun to obtain a single-ended output. Therefore, both the second-order intermodulation and the LO leakage from the two branches are in phase, and will be cancelled in the output balun. From the simulation, the second-order intermodulation intercept point (IIP2) is improved by more than 20 dB compared to the single-ended topology, and the LO-to-IF isolation is improved by more than 25 dB. Looking into either one of the two identical branches, transistors $Q_1$ and $Q_2$ are biased in class-A condition and work together as a broadband active power combiner for RF and LO signals. This is more compact and convenient than a traditional Wilkinson power combiner, especially in the presented design where the LO frequency varies over $f_{LO}$ to $f_{LO}$. As the LO frequency decreased, (e.g., ×3 and ×4 harmonic mixer), a few decibels of LO gain is obtained from simulations, which will be of benefit to reduce the LO power. Furthermore, the active combiner has a good LO-to-RF isolation due to the internal isolation of $Q_1$ from the collector to the base. The transistor $Q_3$ is the transconductance mixer transistor. Its base–emitter junction is biased depending on the order of the harmonic mixing mode. The generated IF signals from $Q_3$ is directly coupled into the last amplifier stage without a dc decoupling capacitor in order to allow low IF. A large transistor (0.25 μm × 10 μm × 2 finger) is chosen for $Q_4$ while it is biased under class-A condition to make sure that the linearity of the overall mixer will not be deteriorated.

In order to make this mixer feasible to work at different LO harmonic mixing modes, the balun is applied at the RF port. Compared to most common designs where the balun is applied at the LO port, this results in differential IF outputs no matter which order of LO harmonic mixing mode is chosen. Any loss introduced by the balun will, however, degrade the mixer’s conversion gain and noise figure. In this work, a Marchand balun [21] is utilized. In order to obtain low insertion loss and wide bandwidth, the Marchand balun exploits two adjacent metal layers so that a strong coupling coefficient can be realized. As is shown in Fig. 6, the space ($S$) between the two metal layers is 1 μm, which is determined by the process. Along the width direction, the two coupled lines shifted a distance of $W_S$. This offers a freedom to tune the coupling coefficient. The balun is simulated and optimized in Agilent Technologies’ ADS Momentum. The simulation results show that the amplitude unbalance is less than 0.5 dB and the phase unbalance is within ±5° in the full D-band.

The designed multi-mode transconductance mixer is simulated and optimized in Agilent Technologies’ ADS. The chip photograph is shown in Fig. 7 and it occupies an area of 1100 × 750 μm².

IV. MEASUREMENT

A. Measurement Setup

On-wafer measurement was used to characterize the designed mixer. The measurement setup is shown in Fig. 8. For the fundamental LO (×1) mixer measurement, both the RF and LO are in the D-band. A cascaded power amplifier (PA) and two frequency doublers are utilized for the RF source. The LO source consist of a Virginia Diodes (VDI) D-band source module, which has higher output power. For the ×2, ×3, and ×4 harmonic mixer measurements, the RF is applied by the VDI D-band source module. The V-band (50–75 GHz) or the W-band (75–110 GHz) source module applies the LO signal for the ×2 harmonic mixer, while the 67-GHz signal generator applies the LO power for the ×3, and ×4 harmonic mixer directly. At the RF port, a D-band tunable attenuator is inserted to enable RF power sweep. At the IF ports, large capacitors

![Fig. 5. Schematic of the single-balanced D-band mixer.](image-url)
in two off-chip bias tees are used as the dc block. An off-chip balun is used to combine the two differential IF signals.

To characterize the conversion gain ($G_c$), the output IF power ($P_{IF}$) is measured by a spectrum analyzer. The noise figure is characterized from the direct noise power measurement [22], as described in [14]. The mixer under test should be biased under the same condition as the conversion gain measurement. The LO signal is applied, but the RF power is turned off. The output noise power from the combined IF port is amplified by a low-noise amplifier (LNA) and further measured by the spectrum analyzer. According to the noise power definition,

$$P_N = k(T_0 + T_N)BG (W)$$

where

- $P_N$ is the measured output noise power in watts;
- $k = 1.38 \times 10^{-23}$ J/K is the Boltzmann constant;
- $T_0 = 290$ K is the standard room temperature;
- $T_N$ is the noise temperature of the overall device-under-test (including the noise from the mixer, the IF probe, the IF cable, and the LNA) in Kelvins.

$B$ is the equivalent noise bandwidth in Hz, and is equal to 1.128 times the resolution bandwidth (RBW) of the spectrum analyzer [23];

$G$ is the gain of the overall device-under-test (including the mixer’s conversion gain, the IF probe loss, the IF cable loss, and the LNA’s gain).

The noise temperature $T_N$ can be calculated since all other parameters are known (e.g., $k$, $T_0$, and $B$) or already obtained from measurements (e.g., $P_N$ and $G$). The noise temperature of the mixer can now be calculated from the Friis formula.

### Table I

<table>
<thead>
<tr>
<th>Mixing Mode</th>
<th>$V_{lb_sim}$ (V)</th>
<th>$V_{lb_meas}$ (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0.7</td>
<td>0.5</td>
</tr>
<tr>
<td>2</td>
<td>0.6</td>
<td>0.45</td>
</tr>
<tr>
<td>3</td>
<td>0.32</td>
<td>0.32</td>
</tr>
<tr>
<td>4</td>
<td>0.32</td>
<td>0.32</td>
</tr>
</tbody>
</table>

### B. Measurement Results

In Table I, the base bias of the mixer transistor ($V_{lb}$ in Fig. 5) is given at different harmonic mixing modes. As the mixing order increases, the base bias decreases, as is predicted in Section II. For the $\times 1$, and $\times 2$ mixing modes, instability was observed in the measurement. To stabilize the circuit, the base bias $V_{lb}$ at the mixing transistor is decreased compared to the ones in the simulation.
Fig. 10. Simulated and measured conversion gain and noise figure as a function of RF frequency at 1, 2, 3, and 4 LO mixing modes, with the LO power of around 0, 1, 5, and 6 dBm, respectively. (GHz.)

At an RF input of 140 GHz and an IF output of 2 GHz, the conversion gain is measured as a function of LO power at different mixing modes. Fig. 9 shows both the simulated and measured results. Due to the active power combiner, even low to moderate LO power can pump this mixer sufficiently. The discrepancy between the simulation and measurement is due to the base bias reduction (at 1 and 2 mixing modes, as is shown in Table I) and the collector current deviation through the last transistor stage ($Q_4$ in Fig. 5). For the $x_2, x_3$, and $x_4$ mixing modes, when the LO power increases, the collector current of $Q_4$ decreases at a similar trend in both simulation and measurement. For the $x_1$ mixing mode, when the LO power increases from −7 to 1 dBm, the collector current of $Q_4$ decreases 10% in the measurement while no variation was observed from the simulation. Hence, the power gain from $Q_4$ starts to saturate at lower LO power compared to the simulation.

At an IF frequency of 2 GHz, the conversion gain and noise figure are measured versus RF frequencies. In the $x_1$ mixer measurement, the LO power available at frequencies below 120 GHz and above 160 GHz is too low to drive the mixer efficiently. Therefore, the measurements cover an RF frequency of 120–160 GHz for the $x_1$ mixer, while a full D-band sweep is performed at $x_2, x_3$, and $x_4$ mixing modes. Fig. 10 shows both the simulated and measured results. With the LO power of around 0 dBm (for $x_1$ mixing), −1 dBm (for $x_2$ mixing), 5 dBm (for $x_3$ mixing), and 6 dBm (for $x_4$ mixing), the
measured results achieve a typical conversion gain of $-3$, $-1$, $-5$, and $-4$ dB and the best noise figure of $12$, $13.5$, $18.5$, and $19$ dB at $\times1$, $\times2$, $\times3$, and $\times4$ LO mixing modes, respectively.

Fig. 11 shows the simulated and measured IF output power as a function of the RF input power. Limited by the measurement setup, the available RF power on chip is less than $0$ dBm and no RF power saturation is observed.

In a subharmonic mixer, the desired mixing harmonic of the LO is critical to be suppressed at the RF port. Therefore, the LO-to-RF isolation is characterized by measuring the $\pi \times$ LO-to-RF leakage, as is shown in Fig. 12.

Table II lists the performance of the presented mixer and some related references. Compared to the other designs at frequencies above $100$ GHz, the presented design is unique for its multi-mode flexibility and operates at relatively low LO powers in the full D-band.

V. CONCLUSION

In this paper, the principle of an arbitrary LO harmonic pumped transconductance mixer has been studied and the optimal duty-cycle of the transconductance waveform has been obtained for the best conversion gain. A novel multi-mode D-band subharmonically pumped transconductance mixer has been designed and fabricated, utilizing a 250-nm InP DHBT technology. The mixer has been characterized at $\times1$, $\times2$, $\times3$, and $\times4$ LO mixing modes, and the measured results achieve a typical conversion gain of $-3$, $-1$, $-5$, and $-4$ dB and a minimum noise figure of $12$, $13.5$, $18.5$, and $19$ dB, respectively.

ACKNOWLEDGMENT

The authors would like to acknowledge and thank the wafer processing team at Teledyne Technologies Inc., Thousand Oaks, CA, USA, for chip manufacture.

REFERENCES


<table>
<thead>
<tr>
<th>$f_{in}$ (GHz)</th>
<th>LO harmonic</th>
<th>LO power (dBm)</th>
<th>$G_c$ (dB)</th>
<th>Noise Figure (dB)</th>
<th>Amplifier</th>
<th>dc (mW)</th>
<th>Technology</th>
</tr>
</thead>
<tbody>
<tr>
<td>122</td>
<td>2</td>
<td>9</td>
<td>-5</td>
<td>21</td>
<td>IF buffer</td>
<td>89.1</td>
<td>SiGe: C BICMOS [24]</td>
</tr>
<tr>
<td>140</td>
<td>1</td>
<td>1</td>
<td>-4</td>
<td>22</td>
<td>IF Ampl.</td>
<td>34.2</td>
<td>65 nm CMOS [25]</td>
</tr>
<tr>
<td>157-164</td>
<td>1</td>
<td>-29</td>
<td>22.5</td>
<td>RF LNA+Baseband Amp.</td>
<td>-</td>
<td>65 nm CMOS [26]</td>
<td></td>
</tr>
<tr>
<td>150-162</td>
<td>2</td>
<td>3</td>
<td>35</td>
<td>9</td>
<td>RF LNA+IF buffer</td>
<td>490</td>
<td>0.25 µm SiGe HBT [27]</td>
</tr>
<tr>
<td>110-170</td>
<td>1</td>
<td>0</td>
<td>-3</td>
<td>12</td>
<td>IF buffer</td>
<td>260</td>
<td>250 nm InP DHBT</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>-1</td>
<td>-1</td>
<td>13.5</td>
<td>IF buffer</td>
<td>262</td>
<td>This work</td>
</tr>
<tr>
<td></td>
<td>3</td>
<td>5</td>
<td>-5</td>
<td>18.5</td>
<td>IF buffer</td>
<td>285</td>
<td></td>
</tr>
<tr>
<td></td>
<td>4</td>
<td>6</td>
<td>-4</td>
<td>19</td>
<td>IF buffer</td>
<td>290</td>
<td></td>
</tr>
<tr>
<td>220</td>
<td>2</td>
<td>-</td>
<td>3.5</td>
<td>7.4</td>
<td>RF LNA</td>
<td>110</td>
<td>100 nm GaAs mHEMT [2]</td>
</tr>
<tr>
<td>220</td>
<td>1</td>
<td>5</td>
<td>-8</td>
<td>9</td>
<td>None</td>
<td>0</td>
<td>100 nm GaAs mHEMT [28]</td>
</tr>
<tr>
<td>245</td>
<td>4</td>
<td>8</td>
<td>-7</td>
<td>39</td>
<td>IF buffer</td>
<td>29.4</td>
<td>0.13 µm SiGe HBT [29]</td>
</tr>
</tbody>
</table>
His research interests include RF integrated circuit (RFIC) designs such as and conferences. He holds 24 U.S., European, Japan, and China patents.


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Paper E

A 110-170 GHz Transceiver in 130 nm SiGe BiCMOS Technology for FMCW Applications

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A 110-170 GHz Transceiver in 130 nm SiGe BiCMOS Technology for FMCW Applications

Yu Yan, Student Member, Tomas Bryllert, Member, IEEE, Sten E. Gunnarsson, Member, IEEE, and Herbert Zirath, Fellow, IEEE

Abstract—A 110-170 GHz transceiver is designed and fabricated at a 130 nm SiGe BiCMOS technology. The transceiver operates as an amplifier for transmitting and simultaneously as a fundamental mixer for receiving. In a measured frequency range of 120-160 GHz, a typical output power of 0 dBm is obtained with an input power of +3 dBm. As a fundamental mixer, a conversion gain of -9 dB is obtained at 130 GHz LO, and a noise figure of 19 dB is achieved. The transceiver is successfully demonstrated as a FMCW radar for distance measurement. With a chirp rate of 1.6×10^10 Hz/s and a bandwidth of 14.4 GHz, a range resolution of better than 3 cm is demonstrated, and transmission test is shown on different objects.

Index Terms—Transceiver, radar, FMCW, amplifier, mixer, power, conversion gain, noise figure, 130 nm, SiGe, BiCMOS, HBT, chirp rate, range resolution, transmission.

I. INTRODUCTION

In most commercial imaging techniques for security applications, the sensor need to be close to the target. However, to survive from a person borne improvised explosive device (IED) even without shrapnel, at least 5 meters separation distance is required [1]. Therefore, standoff imaging, which is capable to detect concealed weapons, explosives, or hidden contraband, tends to be increasingly important for security applications.

Using radar technologies, the 100 GHz to 1 THz region is interesting for standoff detection of concealed objects [2]. The cross-range resolution is proportional to wavelength of the operating frequency, and the range resolution is inversely proportional to the frequency bandwidth, which is also related to the operating frequency [3]. In general, higher operating frequency gives better range resolution and cross-range resolution. Furthermore, as the frequency increases above 500 GHz, the aperture sizes become more manageable. However, the attenuation of the atmosphere and clothing will be affected significantly as the frequency increasing. At 100-600 GHz frequency range, transmission has been experimentally shown on a variety of clothing [4]. Taking the overcoat as an example, the measured transmission decreases from the peak value of more than 0.8 down to around 0.5 as the frequency increases from 192 GHz to 576 GHz. To compensate the attenuation, active systems can be a choice. By employing the frequency-modulated continuous wave (FMCW) radar technique, Jet Propulsion Laboratory (JPL) has developed a 580-GHz imaging radar [5], followed by a 675 GHz version [6], and the latest updated 675 GHz one [7]. In the coherent transceiver front-ends of the three versions, the transmitters are constructed by multiplier chains and power amplifiers, while the receivers are formed by mixers driven by multipliers. Schottky diodes are used in all the multipliers and mixers based on the waveguide technology. In addition, to achieve high-isolation duplexing, a high-resistivity silicon etalon beam splitter is used, however, at the expense of losing half of the beam power for both transmitter and receiver. For the best case, this duplexing method would introduce a round-trip loss of 6 dB. In order to simplify the bulky transmitter/receiver chains and overcome the power loss from duplexing method, an integrated FMCW radar transceiver module, which operates as a frequency doubler for transmitting and simultaneously as a sub-harmonic mixer for receiving, is designed at 200-240 GHz, and readily extended to frequencies up to 1 THz [3]. The waveguide technology is employed by the transceiver module, in which the transceiver circuits are fabricated on 3-μm thick GaAs membranes which consist GaAs Schottky diodes.

According to [3] and [7], a single transceiver is not enough to provide the necessary frame rate for real-time standoff imaging. The most practical solution is to use an array of transceivers. To stack single transceivers into an array, monolithically integrated circuit technologies would be more efficient, in terms of space and cost, compared to the one in waveguide technology [8]. At frequencies above 500 GHz, key components of a transceiver may be more challenging to realize in transistor based technologies than Schottky diode technologies. However, as is pointed in [2], transmission loss in atmosphere and clothing tend to drive designs to lower frequencies (e.g. below 500 GHz). Then, the transistor based active circuits would possibly have gain to achieve adequate...
In this paper, a transceiver, which operates as an amplifier for transmitting and simultaneously as a fundamental mixer for receiving, is designed at 110-170 GHz and can be stacked linearly on-chip to form a compact transceiver array. The circuit is fabricated in Infineon’s 130 nm SiGe BiCMOS technology (B11HFC), which has a typical \( f_{\text{fmax}} \) of 250/435 GHz. The given technology consists of 6 metal layers for interconnection and offers the opportunity of high integration level.

II. TRANSCEIVER CIRCUIT DESIGN

The original idea of sharing a single circuit by both transmitter and receiver was first demonstrated in [9]. The presented FMCW radar transceiver, which consists of two diodes and a few passive components on a printed circuit board, operates as a frequency multiplier for transmitting, and simultaneously as a sub-harmonically pumped “I/Q” mixer for receiving. Then, by choosing a field effect transistor (FET) as the only nonlinear device, a transceiver circuit is designed and demonstrated simultaneously as an amplifier and a resistive mixer at around 10 GHz [10]. Using it as the prototype, a balanced FMCW transceiver is presented with improved AM noise performance [11]. Again, in [3], the measured IF noise power is largely suppressed from the balanced transceiver module compared to the unbalanced one.

Since the IF noise performance is extremely important for standoff imaging applications, a balanced configuration is chosen in this work. The schematic of the designed transceiver is shown in Fig. 1. The circuit is designed to operate as an amplifier for transmitting and simultaneously as a fundamental mixer for receiving. The input signal not only applies as the input for the amplifier but also serves as the local oscillator (LO) signal for mixer. Then, the transmitted signal will be echoed back into the output port and applies as RF for the mixer. In the presented transceiver circuit, active devices consist only two high speed npn transistors (emitter size: 0.13×10 \( \mu m^2 \)) from given technology, and they are biased under class-AB condition for a compromised performance as an amplifier and a mixer. The two identical single-ended common emitter stages are combined by a 90° branch line hybrid at the input and another 90° branch line hybrid at the output. Therefore, the output signals from the two common emitter stages will be combined in-phase from the transmitter’s view, and the generated IF signals will be 180° out-of-phase from the receiver’s view. On the integrated transceiver chip, the IF signals share the same path as the collector dc bias lines. In addition, IF signals generated from a short range FMCW radar normally at a frequency range of kHz or MHz. Therefore, large capacitors and inductors (e.g. bias tee) would be needed to isolate the dc bias from the IF port. However, the capacitor and inductor, which intend to couple out and block few kHz IF frequencies, would occupy unacceptable large chip areas in given technology, so they are omitted on-chip and will be addressed off-chip.

The circuit is designed and optimized in Cadence Virtuoso and some essential passive components (e.g. the 90° branch line hybrid and matching networks) are EM simulated in Sonnet. Fig. 2 shows the chip photo of the fabricated transceiver circuit. The 90° branch line hybrids are meandered to save space, and the base dc bias of the two transistors are combined on-chip into a single dc pad. The transceiver chip occupies a chip area of 980×560 \( \mu m^2 \).

In this work, a commercial off-chip transformer (ADT4-6T from Mini-Circuits) is used to convert the differential IF outputs to a single-ended output, and its center tap is used to apply collector dc bias. Fig. 3 shows the photo of the balanced transceiver circuit together with the off-chip transformer. The transformer is surface mounted on a designed printed circuit board (PCB), which is further mounted on a brass block by silver epoxy. The secondary terminals of the transformer are
connected to the two on-chip Vcc/IF pads through bond wires. Since the chip has no back metallization for grounding, a small gold plate is conductively glued on the brass block and sits between the circuit chip and the PCB. When connecting the on-chip ground pads and the gold plate through bond wires, common ground between the chip and the PCB is obtained.

III. CIRCUIT MEASUREMENT

On-chip measurement is applied to the fabricated transceiver circuit, where the input/output ports and dc bias are connected through probes. The circuit is characterized as an amplifier and a mixer.

To characterize it as an amplifier, the single-ended IF port is terminated by a 50 Ω load. Two-port small signal S-parameter measurement is applied at D-band (110-170 GHz). At the dc biases of Ib=34 µA and Vc=1.6 V, Fig. 4 shows both the measured and simulated small signal S-parameters. Reasonable agreement of S21 and S12 is achieved in the whole D-band. Measured S11 and S22 show that both input and output ports are well matched, even though the best matching frequency shifts 20 GHz downwards compared to the simulated results. From the measured S21, no power gain is obtained. However, from the transmitter’s point of view, the maximum output power is more crucial. Therefore, the output power is measured as a function of the input power, where the input is applied by the VDI D-band source module followed by a tunable attenuator and the output power is measured by
Ericson power meter. Fig. 5 shows both the measured and simulated results at 140 GHz. As can be seen from the measured results, more than 0 dBm output power is obtained with an input power of ~3 dBm, and the gain is still linear at this power level. At the frequency range of 120-160 GHz, the maximum output power is measured when the maximum available power from the VDI D-band source module is applied. It is shown in fig. 6, in which the measured maximum input power is also included as a reference.

When characterizing the circuit as a mixer, the input is applied by the VDI D-band source module with a maximum available power and serves as LO. The output is applied by a VDI D-band extender with a power level of around -20 dBm and serves as the RF. By measuring the output IF power, conversion gain of the mixer can be obtained. With a LO power of around 3 dBm, fig. 7 shows the measured conversion gain as a function of the LO frequencies at a fixed IF frequency of 10 MHz. Fig. 8 shows the measured conversion gain as a function of the IF frequencies at a fixed LO frequency of 130 GHz. The IF frequency is only swept up to 300 MHz, which is the upper limit of the transformer in use. Typical conversion gain of -10~-12 dB is obtained.

To evaluate the noise performance of the mixer, the IF noise power is first amplified by a low noise amplifier, which has a typical gain of G\text{LNA}=50 dB and a typical noise figure of NF\text{LNA}=2.5 dB, and further measured by spectral analyzer. With a resolution bandwidth of RBW=1 MHz from the spectral analyzer, fig. 9 shows the measured IF noise power at different conditions, in which 130 GHz LO signal is applied for the condition of transceiver on. A typical IF noise power of P\text{IF}=-53 dBm is obtained when the transceiver circuit is dc biased and LO pumped. From fig. 8, a typical conversion gain of G\text{mixer}=-9 dB can be read. Therefore, the noise figure of the mixer can be calculated from:

\[ P_{\text{IF}} = k(T_0 + T_{\text{tot}})B G_{\text{tot}} \]
\[ T_{\text{tot}} = \frac{T_{\text{mixer}}}{G_{\text{mixer}}} + \frac{T_{\text{LNA}}}{G_{\text{LNA}}} \]
\[ G_{\text{tot}} = G_{\text{mixer}} \times G_{\text{LNA}} \]

where
- K=1.38×10^{-13} J/K is the Boltzmann constant;
- T_0=295 K is the standard room temperature;
- B=RBW×1.128 is the equivalent noise bandwidth in Hz \[12\].

Given all the numbers, the calculated noise figure is 19 dB.

IV. FMCW RADAR MEASUREMENT

Using the designed transceiver front-end, a FMCW radar is setup and demonstrated for distance measurement. Fig. 10 shows the radar measurement setup. A chirped signal is generated by a direct digital synthesizer (DDS) and it linearly sweeps from 0.3 GHz to 1.2 GHz in 9 ms. After up-converting with a 7.8 GHz signal, two ×4 frequency multipliers are followed. This results in a 129.6-144 GHz signal with a chirp rate of 1.6×10^{12} Hz/s to be fed into the designed transceiver front-end. At the output of the transceiver, a D-band lens corrected antenna, which has a gain of 40 dBi, is connected to the output port of the transceiver. The output IF signal is amplified by an LNA (G_{\text{LNA}}=50 dB and NF_{\text{LNA}}=2.5 dB) and measured by an oscilloscope. The IF spectra is obtained from fast Fourier transform (FFT).

Using FMCW radar technology, the theoretical range resolution is given by:

\[ \Delta r_0 = \frac{c}{2BW} \]
where $c$ is the speed of light, and $BW$ is the chirp bandwidth. In our setup with a chirp bandwidth of 14.4 GHz, it gives a theoretical range resolution of $\sim 1.04$ cm. In practice, the range resolution will be degraded due to nonlinearity and windowing in the post processing [5]. In the measurement, the range resolution is demonstrated by placing two cardboard layers (which are actually the two layers from a cardboard box and the distance in between is tuned by replacing boxes with different thicknesses) alone with the beam travel direction. Fig. 11 demonstrates the range resolution in our setup when a $\sim 3$ cm thick cardboard box is used as the target. The two IF peaks can be recognized with a frequency separation ($\Delta f$) of 300 Hz, which results in a distance ($D$) of:

$$D = \frac{\Delta f \times c}{2 \times \text{chirp rate}} \approx 2.81 \ (\text{cm})$$

This agrees with the value of $\sim 3$ cm, which is measured by a ruler.

Transmission test is also applied on several materials. As is shown in fig. 12. A big piece of metal facing to the antenna is used as a reference. The object under test is then placed between the antenna and the metal reference. Fig. 13 shows the measured IF spectra with different objects. By comparing the power of the second IF peaks with the reference one, it can be seen that the signal at $\sim 140$ GHz penetrate through a 0.5 cm thick plastic board with barely any loss, while a 0.3 cm thick wet cardboard and a 2 cm thick wood shows around 20 dB loss and 40 dB loss, respectively, in a return path.

V. CONCLUSION

Aiming for standoff imaging applications, a 110–170 GHz transceiver is designed to operate as an amplifier for transmitting and simultaneously as a fundamental mixer for receiving. The circuit is fabricated in a 130 nm SiGe BiCMOS technology. The transceiver circuit is well matched in full D-band, and in the frequency range of 120–160 GHz, a typical output power of $\sim 0$ dBm is measured with an input power of $\sim 3$ dBm. When it works as a mixer, a conversion gain of $-9$ dB is obtained at 130 GHz LO frequency, and a measured noise figure of 19 dB is achieved. The designed transceiver is successfully demonstrated as a FMCW radar for distance measurement. With a chirp bandwidth of 14.4 GHz and a chirp rate of $1.6 \times 10^{12}$ Hz/s, a range resolution of better than 3 cm is demonstrated, and transmission loss from several objects are also measured. From the performance of the transceiver circuit alone, reasonable output power and conversion gain are obtained in a frequency bandwidth of more than 30 GHz. Therefore, a sub-cm range resolution should be achieved if the chirp signal could cover the whole bandwidth of the transceiver.

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REFERENCES


