Buffer Related Dispersive Effects in Microwave GaN HEMTs

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Abstract

In applications such as mobile communication and radar, microwave power generation at high frequency is of utmost importance. The GaN HEMT offers a unique set of properties that makes it suitable for high power amplification at high frequencies. However, their performance is limited by trap states, leading to reduced output power and time variant effects. Furthermore, for good high frequency performance a high efficiency it is essential to limit the access resistances in the transistor. The GaN HEMT technology has long lacked a good ohmic contact with good reproducibility.

In this thesis, three buffer designs are considered; C-doped GaN, AlGaN back barriers and a thin GaN structure. The three designs are evaluated in terms of trapping effects using the drain current transient technique. For the C-doped GaN buffer, trapping at dislocations covered with C-clusters is believed to be the main factor limiting output power. Dislocations are presumed to play a major role for the trapping behavior of AlGaN back barriers and the thin structure as well. The maximum output powers for C-doped GaN, AlGaN back barriers and the thin structure are 3.3, 2.7, and 3.9 W/mm at 30 GHz. The output power is found to be limited by trapping effects for all buffer designs.

Moreover, a Ta-based, recessed ohmic contact enables a contact resistance of down to 0.14 Ωmm. The results also indicate that a highly reproducible process might be possible for deeply recessed contacts. An optimized AlGaN/GaN interface shows high mobility >2000 cm²/Vs without the use of an AlN-exclusion layer. The improved interface also decreases trapping effects and the gate-source capacitance at large electric fields compared to an unoptimized interface.

**KEYWORDS:** GaN HEMT, buffer design, C-doping, trapping effects, recessed ohmic contacts, AlGaN/GaN interface quality.
List of appended papers

This thesis is based on the work contained in the following papers:


Other publications

The following papers have been published but are not included in the thesis. Their content partially overlap with the appended papers or are out of the scope of this thesis.


h. J. Bergsten, ”Advanced Heterostructure Designs and Recessed Ohmic Contacts for III-Nitride-Based HEMTs,” Thesis for the degree of Licentiate of Engineering, Department of Microtechnology and Nanoscience, Chalmers University of Technology, Gothenburg, Sweden, 2015.
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Chapter 1

Introduction

GaN high electron mobility transistors (HEMTs) are of great interest for microwave power generation at high frequency. At the early stages, the advancements of GaN HEMTs were mainly driven by radar applications in the defense industry. In these, high output power, efficiency, and robustness are of great importance. The last couple of years, radar systems based on GaN HEMT monolithic microwave integrated circuits (MMICs) have started entered the market. Currently, mm-wave scanners for security applications are also among possible applications for GaN HEMTs. Furthermore, as the demand for higher data rates in mobile communication is increasing, higher operating frequencies are required in order to increase bandwidths and escape the congested bands in the sub 6 GHz range. In the 5th generation of wireless systems (5G), operating frequencies up to 60 GHz are expected. Moreover, wireless links in the backhaul of the 5G network (requiring very high data rates) are expected to operate at frequencies up to 170 GHz. These demands are a good fit for the large bandwidths achievable through the GaN HEMT technology. Aside from these applications, GaN HEMTs are readily employed in high power switching applications. In these, the low on-resistance, high switching frequencies and high operating voltages offer exceptional performance [1]. Even though GaN HEMTs for power applications share many of the issues of GaN HEMTs for microwave applications, power devices will not be considered in this thesis.

The excellent performance of the GaN HEMT is enabled by the large band gap of GaN (3.4 eV), its large electron velocity \(2 \cdot 10^7\) cm/s), together with the ability to form HEMT epi-structures with
high electron mobility (> 2000 cm$^2$/Vs) and large electron sheet density (> $1 \cdot 10^{13}$ cm$^{-2}$). The large band gap leads to robust devices that can operate at high voltages. The high electron mobility and large sheet density decreases the losses in the transistors and, together with the large electron velocity, enables excellent high frequency performance with $f_T$ and $f_{max}$ reaching over 400 GHz [2]. In total, the exceptional material qualities leads to high achievable output power ($P_{out} = 3$ W/mm) even at operating frequencies around 100 GHz [3]. Furthermore, due to the large operating voltages superior linearity and lower matching losses compared to competing technologies are expected [4]. The HEMT structure also facilitates great noise performance, making GaN HEMTs ideal for low noise amplifiers.

However, even though GaN HEMT technology has matured exceedingly over the past years, several problems still remain. For example, a highly repeatable ohmic contact with low contact resistance is not yet available. This leads to reduced yield, reduced efficiency and reduced high frequency performance. Furthermore, DC-AC dispersion is a major concern, leading to reduced output power and efficiency. In some applications, such as low noise amplifiers, linearity can also be heavily affected by dispersive effects. The dispersive effects are due to traps located mainly on the surface or in the bulk of the semiconductor. The effects of the surface traps can be almost completely mitigated using passivation layers and field plates while the bulk traps require extensive epi-structure optimization to be minimized. Since the HEMTs operate at high power levels, large demands are put on thermal management. The epi-structure is commonly grown on SiC substrates, enabling an effective removal of excess heat. However, layers of poor crystalline quality or ternary alloys (e.g. AlGaN or InAlN) in the epi-structure can severely increase the total thermal impedance between the transistor and the substrate [5, 6]. From a commercial standpoint the GaN HEMT technology lacks standardized processes, leading to reduced reliability, uniformity, and repeatability, which are associated with large associated costs.

The main part of the thesis is attributed to buffer design and its effect on dispersive effects and output power. The goal has been to summarize the three appended papers dealing with this topic, trying to give a combined interpretation of the results. In the case when the appended papers does not cover the topic that is discussed, previously unpublished results are used to facilitate the discussion. Other aspects
on GaN HEMT technology are also investigated with focus on areas where problems still remain. Furthermore, this thesis aims to give the reader a brief introduction to the basic ideas and problems of the GaN HEMT.

The thesis is organized as follows. A brief introduction to the GaN HEMT, its operation, and the epi-structure design is given in Chapter 2. In Chapter 3 crucial technological aspects of the GaN HEMT is discussed, including ohmic contacts and surface passivations. The main contribution of this thesis, regarding buffer design and characterization, is presented in Chapter 4. Finally, Chapter 5 presents conclusions that can be drawn from this thesis and a future outlook of the field. Parts of the research work in this thesis have already been published in the Licentiate thesis [h]. Therefore, text and figures from [h] may be fully or partially reproduced in this thesis.
The aim of this chapter is to give a brief introduction to the basic design and function of a GaN HEMT. This is used as a basis for discussion of different issues and design choices, parts of which are considered more extensively later in the thesis. Section 2.1 deals with the transistor layout and its operation. In section 2.2 a brief introduction to a standard GaN HEMT epi-structure on a SiC substrate, similar to what has mostly been used in this thesis, is presented.

2.1 The GaN HEMT and its operation

A schematic cross section of an AlGaN/GaN HEMT, with its essential parts indicated, can be seen in Fig. 2.1. The 2-dimensional electron gas (2DEG) in the AlGaN/GaN interface forms the channel of the transistor. The electrons in the 2DEG should have a high electron mobility ($\mu$) to decrease the resistance of the access regions. Furthermore, the electron sheet concentration ($n_s$) should be appropriately large for the intended application. Standard values for $\mu$ and $n_s$ in an AlGaN/GaN heterostructure are 2000 cm$^2$/Vs and $10^{13}$ cm$^{-2}$ respectively.

2DEG formation The mechanisms responsible for the formation of the 2DEG is well described in [7]. In short, the III-N materials are all polarized due to the strong ionicity of their covalent atomic bonds. In the standard Ga-polar case, the polarization fields are pointing down into the structure, as indicated in Fig. 2.2a. The polarization field strength is larger in AlGaN compared to GaN, giving a net positive
polarization charge at the AlGaN/GaN interface. This charge attracts electrons originating from the AlGaN surface, forming the 2DEG. The number of electrons in the 2DEG will be the same as the polarization charge which depends on the Al content and thickness of the AlGaN layer, where increasing Al-concentration and thickness leads to larger $n_s$. For an AlGaN barrier layer the Al-concentration usually range from 15 to 30%, and the thickness from 10 to 25 nm. The band structure of an $\text{Al}_{0.30}\text{Ga}_{0.70}\text{N}/\text{GaN}$ structure can be seen in Fig. 2.2b. Compared to the AlGaAs/GaAs structure an important difference is that no n-doping in the AlGaN barrier layer is required to generate the electrons in the 2DEG. However, since the 2DEG is formed of electrons from the surface it is exceedingly sensitive to changes in the surface potential.

**Ohmic and Schottky contacts** The ohmic drain and source contacts should supply a connection to the 2DEG with low contact resistance ($R_C$). Due to the large band gaps of the III-N:s, ohmic contact formation is hard to achieve. The topic of ohmic contacts have been a long standing issue in the GaN HEMT community and is explored in more detail in Chapter 3.

The purpose of the gate Schottky contact is to control the current flowing between the two ohmic contacts. This is done by utilizing the field effect where a change in $V_{GS}$ will result in band bending under the gate contact. For a sufficiently negative $V_{GS}$, a depletion of the 2DEG under the gate contact is achieved, as illustrated in Fig. 2.3. Ni is the most commonly used gate metal for GaN HEMTs and is also used in
this thesis. Other large work function metals can also be employed, such as Pt, Pd, Ir or Au [8]. The gate metal should also offer a low resistivity, to decrease the gate resistance, and good adhesion to the surface. The maximum output current is set by when the forward biased Schottky diode starts conducting. When it does, any change in applied gate voltage will modulate the gate leakage current instead of the band bending. A metal-insulator-semiconductor (MIS) structure can be used to limit gate leakage [9].

Figure 2.3: Schematic illustration of flat band condition.
Surface effects Since the electrons in the 2DEG originates from the barrier surface it is very sensitive to changes in the surface potential [10]. Electrons can interact with trap states at the surface, reducing the number of electrons in the 2DEG. During transistor operation, this can have a large negative impact on performance. In fact, trapped electrons on the surface acts like a virtual gate, depleting the 2DEG [11]. If the trapping occur around the gate a decrease in $I_{DS}$ will be measured, an effect known as current collapse, see Fig 2.4a. If the trapping occur in the drain access region, an increase in $R_{ON}$ will be measured, Fig 2.4b. The trapped electrons usually originate from the gate metal and can get trapped during e.g. off-state biasing conditions or for large drain voltages. To mitigate these effects a surface passivation is usually deposited with the aim to passivate trap states or effectively blocking electrons from getting trapped.

Surface passivation The most investigated passivation layer for GaN HEMTs is silicon nitride, Si$_N_x$ [12, 13, 14, 15]. In this case, nitrogen is believed to play a crucial part in filling nitrogen vacancies on the surface, reducing the number of interface traps [16]. Other commonly used passivations are SiO$_2$ and Al$_2$O$_3$ [17, 18]. Several studies have compared different passivation layer’s ability to reduce current collapse with various results [19, 20, 21]. Generally, Si$_N_x$ is found to give best performance. However, only comparing the passivation material is problematic since both pre- and post-treatments have shown to have large impact on trapping effects. For example, both N and O plasma based
pre-treatments have shown to increase the effectiveness of the passivation layer [22, 23]. The topic of surface passivations and surface effects on III-N heterostructures is complex and many effects are not yet fully understood. Consequently, it is a popular research topic with many publications each year. For a more in depth look in to surface effects and passivations on GaN and AlGaN see [24].

**Device layout** A scanning electron microscope (SEM) micrograph of a GaN HEMT fabricated in this work can be seen in Fig. 2.5. The source, drain and gate contacts are indicated in the figure. As seen, two gate contacts are present. This design is made up of two transistors in parallel, with a shared drain contact. This is a common method to reduce the total area of the transistor for a certain gate width. In this thesis most, most measurements have been performed on 2x50 µm devices. Typical transistor dimensions are as follows; \( L_{DS} = 2-3 \) µm, \( L_{GD} = 1-2 \) µm, \( L_{GS} = 1 \) µm, \( L_G = 50-200 \) nm.

**High frequency operation** Two standard figures of merit of a transistors ability to operate at high frequencies are \( f_T \) and \( f_{max} \). \( f_T \) (\( f_{max} \)) is defined as the maximum frequency at which the transistor can supply
small signal current (power) gain. $f_T$ is proportional to $v_e/L_G$, where $v_e$ is the electron velocity, whereas $f_{\text{max}}$ is given by;

$$f_{\text{max}} = \frac{1}{2} \frac{f_T}{\sqrt{2\pi \cdot f_T \cdot C_{gd}(R_g + R_s) \cdot \frac{R_g + R_s}{R_{ds}}}}.$$  \hspace{1cm} (2.1)

Here, $C_{gd}$ is the gate-drain capacitance, $R_g$ and $R_s$ are the gate and source access resistances, and $R_{ds}$ is the output resistance. The main method of increasing the high frequency performance is down-scaling of $L_G$. However, as $L_G$ is decreased, short channel effects start emerging, weakening the gate control. The short channel effects can be reduced by making the barrier layer thinner, decreasing the distance between the gate and the 2DEG. It has been reported that the aspect ratio between the gate length and AlGaN barrier thickness should be at least 15 in order to limit short channel effects [25]. However, as the barrier thickness is decreased $n_s$ will also decrease, creating a complex optimization problem. Other than gate length scaling, decreasing the resistance in the access regions and the ohmic contacts are also vitally important for high frequency performance.

**Electric fields in the structure** One of the advantages of GaN HEMTs are the large breakdown voltages. During operation, large drain biases are regularly applied, leading to large electric fields. In Fig. 2.6 the electric potential distribution in a GaN HEMT held in off-state with a large drain bias are visualized. As seen, the change in electric potential (electric field) is largest at the gate edge on the drain side but also extends deeper into the GaN layer. Therefore, the large fields can have a considerable impact on the electron occupation of trap states in these areas. Gate or source connected field plates can help reduce the electric field strength and in so the number of occupied traps [26, 27]. In this work, a gate integrated field plate, as indicated in Fig. 2.1, is commonly used.

### 2.2 The GaN HEMT epi-structure

This section will give a brief overview of a standard GaN HEMT epi-structure, commonly used for RF power amplifier applications, see Fig. 2.7. The purpose of each layer will be shortly explained and alternative material selections will be outlined. Currently, more exotic epi-structures are frequently reported. These will be covered more
Figure 2.6: Electric potential distribution in a GaN HEMT biased in an off-state with a drain voltage of 50 V. Sentaurus simulations courtesy of Hans Hjelmgren.
extensively later in the thesis. Several different techniques are available to grow the epi-structure, the most commonly used are metal organic chemical vapor deposition (MOCVD) and molecular beam epitaxy (MBE). In this work, the main material suppliers (and collaborators) has been Linköping University and SweGaN AB, both of which use the same hot-wall MOCVD system [28]. However, materials have also been supplied by Cree Inc., IQE, and III-V lab, using the more common cold-wall MOCVD technique. As indicated by the name, in the hot-wall system the temperature of the growth target is controlled by heating the walls of the growth chamber, whereas only the target is heated in the cold-wall system. The lower temperature gradients in the hot-wall case generally results in better wafer uniformity but the technique is less suited for large scale fabrication compared to cold-wall systems. Since all the materials in this work have been grown using MOCVD, this will be the main growth method considered in this thesis.

Substrate A good substrate material should have a lattice constant close to the material that is to be grown on it. Under operation the HEMTs will generate a lot of heat so a large thermal conductivity of the substrate is desired. Furthermore, for high frequency applications the substrate should preferably be highly resistive in order to minimize parasitical capacitance. For commercial applications the substrate price is also of large concern. Table 2.1 summarizes the most common substrate alternatives for GaN-based epi-structures and their performance with respect to the parameters discussed above.
Table 2.1: Available substrates for III-N growth.

| Material | Lattice mismatch with GaN (|%|) | Thermal conductivity (W/mm K) | Price |
|----------|--------------------------------|-------------------------------|-------|
| 4H-SiC   | 3.4                            | 490                           | Moderate |
| Si       | 17                             | 150                           | Low    |
| GaN      | 0                              | 260                           | High   |
| AlN      | 2.5                            | 285                           | High   |
| Diamond  | 12                             | 600-2000                      | High   |

The high thermal conductivity and low lattice mismatch of SiC has made it the most common substrate for RF power amplifier applications. Meanwhile, the low price of Si substrates has made it the standard substrate for high power applications. GaN and AlN are both very attractive substrates but are only beginning to become commercially available in very small sizes. On these, very high quality GaN can be grown with low dislocation densities. Diamond is interesting due to its extremely high thermal conductivity. However, the large lattice mismatch and large difference in thermal expansion coefficient makes growth difficult. In this work SiC substrates have mainly been used.

**Nucleation layer** The function of the nucleation layer is mainly to facilitate two-dimensional growth of the subsequent GaN buffer, but also to mitigate the lattice mismatch between GaN and the substrate. Due to the lattice mismatch the crystal quality is inherently low for the nucleation layer, making it a poor thermal conductor. Since much of the benefits of using substrates with large thermal conductivity is negated by putting a thermal barrier in between the substrate and the devices, effort has been put in to optimizing the quality of the nucleation layer [5]. For SiC substrates AlN is most commonly used as nucleation layer. The larger lattice mismatch between GaN and Si sets larger requirements on the nucleation layer. Therefore, it is not uncommon to use strained AlN/GaN superlattices [29]. An advantage with GaN substrates is that no nucleation layer is required which will aid the overall heat transport through the structure.

**GaN buffer** The purpose of the GaN buffer layer is to decrease the number of defects in the channel region and enable a flat surface for
the barrier layer to be grown upon. Usually, the GaN buffer needs to be grown to a thickness of more than 1µm before these conditions are met. The buffer also needs to supply a good bottom confinement in order to limit short channel effects. This can be achieved in a number of ways, unfortunately all of them are associated with increased trapping in the buffer region. Minimizing trapping effects while maintaining good confinement is therefore a common research topic for GaN HEMTs. This is also a large part of the thesis work and is further investigated in Chapter 4.

**Barrier** As explained above, using an AlGaN barrier as example, the 2DEG is formed due to the polarization charge in the barrier/GaN interface. However, other barrier materials than AlGaN are commonly employed. In$_{0.17}$Al$_{0.83}$N has the advantage of being lattice matched to GaN. This gives less strain in the structure which is beneficial from a reliability perspective. Furthermore, the high Al-concentration of In$_{0.17}$Al$_{0.83}$N results in a large polarization field, meaning a large $n_s$ can be achieved for thinner barrier thicknesses. This is advantageous for high frequency applications since good gate control can be obtained even for short gate lengths. Even thinner barriers are possible when using pure AlN as barrier material. In this case, a barrier thickness of 3-4 nm is enough to generate a high $n_s$. Therefore, HEMTs with high values of $f_T$ and $f_{max}$ commonly utilize InAlN [30] or AlN [2] barriers.

**GaN cap** On top of the (usually Al rich) barrier layer it is common to include a thin (2-3 nm) GaN cap layer. This layer is intended to protect the surface of the barrier from oxidizing once it is removed from the growth chamber. The GaN cap layer reduces the maximum drain current as well as the gate leakage [31].
Standardized processes with high yield are of great importance for any semiconductor technology. Many emerging technologies struggle to compete with more mature technologies, such as Si or GaAs, due to higher associated costs. Over the last 20 years GaN HEMT technology has matured immensely. However, areas still remain where no standardized solutions exists. Most notably are the ohmic contacts which have been a long standing problem. The large band gap complicates the contact formation and although low resistive ohmic contacts are frequently reported, a standardized contact is not yet available. Another area of large interest is surface passivation. However, compared to ohmic contacts, surface passivation techniques are rather mature. A proper passivation layer in combination with field plates have shown to almost completely remove surface trapping [32]. A large part of the advances for GaN HEMTs can also be attributed to advances in material growth. Over the years, crystal quality have gradually increased and epi-structure designs that were previously only theoretically conceivable are now routinely grown. Nevertheless, dislocations and other growth defects can still have a limiting effect on device reliability and performance [33].

This chapter will give an overview of some important and challenging areas of GaN HEMT technology. First, the process flow for HEMT fabrication used in this thesis is presented in section 3.1. Second, ohmic contacts to GaN-based heterostructures are considered. A recess etched Ta-based contact is reported in paper [A] and the general state of ohmic contacts to GaN-based heterostructures is treated in section 3.2. Third,
achieving low device-to-device leakage has been investigated in section 3.3. Lastly, section 3.4 deals with material growth, specifically the quality of the GaN to AlGaN transition. Paper [B] reports on the effect of the AlGaN/GaN interface quality on electron penetration into the barrier layer. Buffer design is also of vital importance for the GaN HEMT large-signal and high frequency performance. This topic is considered in Chapter 4.

3.1 HEMT fabrication process

The process flow for HEMT devices used in this thesis is presented in Fig. 3.1. The processing steps are as follows:

1. A Si-rich SiN passivation layer (50-70 nm) is deposited using low pressure chemical vapor deposition (LP-CVD). This passivation has shown to give a good protection from surface trapping [34].

2. Mesa isolation is achieved using photolithography and an Oxford ICP-RIE dry etching system (used for all dry etching processes). The SiN is etched in a NF$_3$-based plasma, whereas the heterostructure is etched in a Cl/Ar-based plasma.

3. Recessed ohmic contacts are formed. This is a self-aligned process in which the same resist mask is used for both etching and metal lift-off. A low power Cl-based plasma is used for the recess etching, followed by surface cleaning in diluted HCl and HF. Metal deposition is performed in an e-beam evaporator system using a metal stack of Ta/Al/Ta. The contacts are annealed in a rapid thermal anneal system in N ambient at 550-600 °C. The ohmic contact process is explained in further detail in paper [A].

4. The gate footprint is defined using e-beam lithography and plasma etching. Most of the SiN is etched in an anisotropic etching process, based on CF$_4$/Ar. This allows the correct gate length to be maintained since the gate length is set by the etched trench in the SiN. The last part of the SiN is etched using the standard NF$_3$ plasma in order to remove any polymer residues created by the CF$_4$.

5. Another e-beam lithographic step is used to define the gate metal, which is deposited using e-beam evaporation. A Ni/Pt/Au metal stack is used, forming a gate with an integrated field plate.

6. Metal contact pads (Ti/Au/Ti) are formed using optical lithography and e-beam evaporation.
Figure 3.1: Illustration of the GaN HEMT process flow used in this thesis. Images not to scale.
3.2 Ohmic contacts

A reliable ohmic contact process with low contact resistance ($R_C$) is essential in all semiconductor technologies. For HEMTs, low $R_C$ is especially vital for the high frequency performance of extremely scaled devices [35]. Noise performance, efficiency, and reliability are also enhanced for devices with low $R_C$-contacts. Furthermore, for devices with short drain and source access regions, the line edge acuity of the contacts is of great importance in order to prevent short circuits with the gate metal.

Planar contacts The standard way to achieve ohmic contacts with low $R_C$ in GaN HEMT epi-structures is a Ti/Al/Ni/Au metal stack deposited directly on top of the barrier layer [36, 37, 38, 39, 40]. This planar contact method can give low $R_C$ ($\sim 0.15 \, \Omega \, \text{mm}$) but requires a high anneal temperature (800-900 °C) which may cause increased sheet resistance in the 2DEG [41]. Furthermore, poor line edge definition may be obtained due to the low melting point of Al ($\sim 660 \, ^\circ\text{C}$), causing reactions with the Au layer [42, 43]. Many explanations for the low $R_C$ obtained with Ti/Al-based contacts have been suggested. The formation of TiN through extraction of N from the semiconductor is the most common one. Here, N-vacancies in the barrier layer is thought to act as n-dopants which will effectively decrease the energy barrier seen by the electrons, increasing the tunneling probability and reducing the contact resistance [44, 45, 46, 47]. However, the violent reaction occurring when forming TiN have shown to lead to protrusions in to the semiconductor [48]. In paper [e] these protrusions have been connected to increased vertical and lateral leakage currents, limiting high voltage operation.

To get a sense of typical $R_C$ values for planar contacts, Table 3.1 compares literature values of contacts formed to various GaN heterostructures where the metal stack has been deposited on top of the barrier. Both Ti/Al/Ni/Au and other metallization schemes are included. As seen, typically an anneal temperature of over 800 °C is required, with the exception of an Mo-based contact annealed at 650 °C. Another observation that can be made is that for Ti/Al-based contacts a higher $R_C$ is generally obtained for AlGaN barriers with high Al-content. This is probably related to the larger energy barrier present in these cases.
<table>
<thead>
<tr>
<th>Ref.</th>
<th>Barrier</th>
<th>Metal stack</th>
<th>Anneal temp. (°C)</th>
<th>$R_C$ (Ωmm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>[36]</td>
<td>GaN/Al$<em>{0.28}$Ga$</em>{0.72}$N/AlN (2/27/1 nm)</td>
<td>Ti/Al/Ni/Au</td>
<td>820</td>
<td>0.45</td>
</tr>
<tr>
<td>[38]</td>
<td>Al$<em>{0.24}$Ga$</em>{0.76}$N (18 nm)</td>
<td>Ti/Al/Ni/Au</td>
<td>830</td>
<td>0.2</td>
</tr>
<tr>
<td>[40]</td>
<td>Al$<em>{0.30}$Ga$</em>{0.70}$N (24 nm)</td>
<td>Ti/Al/Mo/Au</td>
<td>750</td>
<td>0.35</td>
</tr>
<tr>
<td>[49]</td>
<td>Al$<em>{0.26}$Ga$</em>{0.74}$N/AlN (-/- nm)</td>
<td>Ta/Ti/Al/Mo/Au</td>
<td>825</td>
<td>0.4</td>
</tr>
<tr>
<td>[50]</td>
<td>GaN/Al$<em>{0.20}$Ga$</em>{0.80}$N/AlN (2/20/2 nm)</td>
<td>Ti/TiN</td>
<td>850</td>
<td>0.13</td>
</tr>
<tr>
<td>[50]</td>
<td>GaN/Al$<em>{0.35}$Ga$</em>{0.65}$N/AlN (2/20 nm)</td>
<td>Ti/TiN</td>
<td>850</td>
<td>0.6</td>
</tr>
<tr>
<td>[51]</td>
<td>In$<em>{0.17}$Al$</em>{0.83}$N/AlN (6/1 nm)</td>
<td>Mo/Al/Mo/Au</td>
<td>650</td>
<td>0.15</td>
</tr>
<tr>
<td>[52]</td>
<td>In$<em>{0.17}$Al$</em>{0.83}$N/AlN (7/1 nm)</td>
<td>Si/Ge/Ti/Al/Ni/Au</td>
<td>820</td>
<td>0.35</td>
</tr>
<tr>
<td>[53]</td>
<td>In$<em>{0.18}$Al$</em>{0.82}$N/AlN (10/1 nm)</td>
<td>Ti/Al/Ni/Au</td>
<td>900</td>
<td>0.15</td>
</tr>
<tr>
<td>[54]</td>
<td>In$<em>{0.18}$Al$</em>{0.82}$N/AlN (9/1 nm)</td>
<td>Ta/Si/Ti/Al/Ni/Au</td>
<td>825</td>
<td>0.36</td>
</tr>
</tbody>
</table>

Table 3.1: Literature values of $R_C$ for planar contacts on different heterostructures.
Regrown \( n^+ \)-GaN contacts

Extremely low values of \( R_C \) (\( \sim 0.1 \ \Omega mm \)) have been achieved using regrown \( n^+ \)-GaN contacts [2, 55]. These contacts are made by etching past the barrier, into the buffer layer, and then growing lattice matched, highly doped n-GaN in the recess. This allows for the formation of a direct contact between the 2DEG and the \( n^+ \)-GaN with low resistance. The \( n^+ \)-GaN is then easily contacted using standard metallization. This technique offers very low \( R_C \) but the processing is complex and costly which could make it unsuitable for large scale fabrication. Furthermore, a large 2DEG density is required to obtain extremely low values of \( R_C \) for regrown contacts [56]. Since a large \( n_s \) is not always an option other contact processes are sometimes more reasonable options. Due to their nature, regrown contacts are mostly used on extremely down-scaled devices for high frequency operation. As explained in section 2.2, in these cases an AlN or InAlN barrier is usually employed for which a large \( n_s \) is easily attained. Table 3.2 shows achieved contact resistances on different heterostructures using regrown contacts. As expected, for barriers sustaining a large \( n_s \), an extremely low \( R_C \) can be achieved. However, for structures with a more moderate \( n_s \) (\( \sim 1 \cdot 10^{13} \ \text{cm}^{-2} \)), \( R_C \) is comparable to metal-based contacts. This was also the case for the regrown contacts in paper [d].

<table>
<thead>
<tr>
<th>Ref.</th>
<th>Barrier</th>
<th>( R_C ) (( \Omega mm ))</th>
</tr>
</thead>
<tbody>
<tr>
<td>[57]</td>
<td>( \text{In}<em>{0.17}\text{Al}</em>{0.83}\text{N}/\text{AlN} ) (3/2 nm)</td>
<td>0.16</td>
</tr>
<tr>
<td>[55]</td>
<td>( \text{In}<em>{0.18}\text{Al}</em>{0.82}\text{N}/\text{AlN} ) (8/1 nm)</td>
<td>0.10</td>
</tr>
<tr>
<td>[58]</td>
<td>( \text{GaN}/\text{AlN} ) (3/4 nm)</td>
<td>0.10</td>
</tr>
<tr>
<td>[56]</td>
<td>( \text{GaN}/\text{Al}<em>{0.26}\text{Ga}</em>{0.74}\text{N} ) (3/18 nm)</td>
<td>0.31</td>
</tr>
<tr>
<td>[d]</td>
<td>( \text{GaN}/\text{Al}<em>{0.30}\text{Ga}</em>{0.70}\text{N} ) (2/11 nm)</td>
<td>0.24</td>
</tr>
</tbody>
</table>

Table 3.2: Literature values of \( R_C \) for regrown contacts on different heterostructures.
Figure 3.2: Illustration of three different cases of the formation of recessed ohmic contacts; (a) one where the barrier is still present, (b) one where the barrier is present but it is so thin that no 2DEG is formed under it and (c) one where the barrier has been entirely etched.

**Recess etched contacts** Recess etched metal based contacts can be seen as a compromise between planar metal contacts and regrown contacts. In this case, a recess etch is performed prior to metal deposition which has shown to decrease the required anneal temperature [59]. However, recess etching introduces additional parameters, such as recess depth and slope of the recess sidewall. Generally, the formation of recessed ohmic contacts can be divided into three different cases; one where the barrier is still present, one where the barrier is present but it is so thin that no 2DEG is formed under it, and one where the barrier has been entirely etched away, Fig. 3.2. In the first case the contact mechanisms should be similar to planar metal based contacts. However, in the two later cases current transport have to rely on a sidewall contact [60]. For these, the sidewall angle ($\alpha$) should be of great importance as it will determine the 2DEG-to-metal distance [56].

The effect of recess depth on $R_C$ has been studied a number of times
with various results. A minimum in $R_C$ has been found for recess depths around the 2DEG [51, 61, 62], when a large portion of the barrier was left [59, 63], and when the barrier was completely removed [60]. All in all, no clear conclusions regarding the optimum recess depth are easily drawn from the literature, perhaps because recess depth is not the only critical parameter. In paper [A] a parameter study was performed, varying the recess etch depth and anneal temperature using a Ta/Al/Ta metal stack with different thicknesses of the bottom Ta layer. This was done on an InAlN/AlN/GaN heterostructure with the lowest $R_C$ (0.14 $\Omega \text{mm}$) achieved for a recess etch which almost removed the whole barrier. Table 3.3 contains values of $R_C$ achieved using recessed contacts. Generally, the anneal temperatures are lower for recessed contacts compared to the planar contacts. Not only do the contacts presented in paper [A] have a comparably low anneal temperature, the $R_C$ is also close to state of the art, even compared to regrown contacts.

From a reproducibility perspective it is interesting to note that in paper [A] a low $R_C$ was achieved also for deeper etches, as seen in Fig. 3.3a. For recess depths close to the barrier thickness, a very stable etch-
Figure 3.3: A plot of (a) $R_C$ and (b) $R_{sh}$ versus etching depth using a bottom Ta thickness of 5 nm in paper [A]. The plot is constructed from the optimum anneal condition for each recess etch depth. The 2DEG position is indicated with a dotted line.

The recess etching process is required to get reproducible contacts. Furthermore, even for small changes in the barrier design re-optimization of the etching time is necessary. A method to increase the reproducibility of recessed contacts could be to make a deep recess, well past the barrier layer. Ideally, this would remove the etching depth as a critical parameter and changes in the barrier layer would not affect $R_C$. This concept was further investigated in a Master’s thesis [67]. In this work, the idea was to investigate the dependence of $R_C$ on recess sidewall slope ($\alpha$ in Fig. 3.2) for deeply etched contacts. This was achieved through a new plasma etching process and control of the resist profile. Using a simple model, it was calculated that a near vertical etch would be ideal, although no experimental data supporting this was found. Further studies in this area are ongoing.

Another interesting property of the deeply etched contacts in paper [A] was the decrease in $R_{sh}$ seen in Fig. 3.3b. A possible explanation is that the removal of the barrier under the contacts decreased a compressive strain in the heterostructure between the contacts. This would give a larger total polarization in this section which would increase $n_s$ in the 2DEG [7].

### 3.3 Device isolation

For MMIC applications electrically isolating devices from each other is of high importance. Generally, two different approaches to achieve de-
vice isolation on GaN heterostructures are available. By etching mesas to define the active regions the only device-to-device current path available is through the highly resistive buffer or surface states along the way. Alternatively, high energy ion implantation can be used to damage the crystal and in so increase the resistivity. Both mesa etching and ion implantation has shown low device-to-device leakage [60, 68, 69]. However, lower gate-leakage is expected for ion implantation since there is no risk of the gate metal directly contacting the 2DEG [70]. Furthermore, a flat surface may simplify further processing as the mesas might cause varying resist thicknesses or interference effects during lithography exposure. Nevertheless, mesa etching might be preferable since ion implantation may degrade at high temperatures [71, 72]. In this thesis, reasonable device-to-device isolation levels (> $10^6$ Ωmm at 100 V for a separation of 5 µm) are achieved using mesa etching. However, this value can be significantly larger depending on the buffer resistivity.

Decreased gate leakage using TMAH An experiment was designed with the intention of decreasing the gate leakage currents for the mesa etched devices. The chemical tetramethylammonium hydroxide (TMAH) has previously been used to decrease leakage currents in various GaN-based devices [73, 74, 75, 76]. Generally, TMAH works as an weak etchant on GaN, although it mostly etches areas with crystal defects. It has been shown to remove plasma etching damages and making etched sidewalls more vertical [77], as well as removing the native Ga-oxide and dangling bonds on the GaN surface [76]. Therefore, TMAH could decrease the gate leakage by producing a more vertical mesa sidewall, minimizing the gate metal-to-2DEG contact.

TMAH was applied on the dry etched surface after mesa etching (step 2 in Fig 3.1). The etching was performed for 10 min in a TMAH solution of 25%, kept at 80 °C. Two identical chips were used from the Fe-doped wafer in paper [E]. The first chip was processed using the standard HEMT process described in section 3.1 (denoted Standard), the other chip was processed in tandem but was also etched in TMAH after the mesa etch (denoted TMAH). The output characteristics remained unchanged by the TMAH treatment, Fig. 3.4a. However, a decrease in the gate leakage current by a factor of 5 was measured in the transfer characteristics, Fig. 3.4b. Most probably, this was due to a more vertical mesa sidewall, but could also be related to removal of current conducting surface states. In any case, TMAH treatment shows de-
increased gate leakage with no obvious side-effects. The approach should be easy to include in any mesa isolation process.

3.4 2DEG mobility enhancement

Electron mobility is intrinsically high in the 2DEG due to the separation of the electrons and the ionized donor atoms. At room temperature (RT) several scattering processes contribute to the total mobility, although optical and acoustic phonons usually have the largest impact [78]. The phonon scattering is highly temperature dependent and their importance can be decreased by lowering the temperature. Other important processes are scattering due to interface roughness, alloy disorder scattering, and scattering at dislocations [79], which are all temperature independent processes. The relative importance of each process can be studied by varying the temperature or \( n_s \) and fit the resulting mobility changes to theoretical models for the scattering mechanisms [78, 79].

**AlN exclusion layer** A common method to increase the mobility of the 2DEG in GaN heterostructures is to include a thin (1-2 nm) AlN exclusion layer at the bottom of the barrier stack, see Fig. 3.5a. The large band gap of AlN is believed to limit the number of electrons penetrating into the barrier layer. The mobility in the 2DEG is then increased since a large prevalence of alloy disorder scattering is present.
Figure 3.5: (a) Schematic illustration of barrier layer including an AlN-exclusion layer. (b) Simulated conduction band energies and electron densities for three AlGaN/GaN heterostructure with different AlGaN/GaN interfaces. The AlN layer is 1 nm thick and the diffuse interface changes Al-content from 0 % to 30 % over a distance of 3 nm.

in the barrier layer. Fig. 3.5b shows Poisson-Schrödinger simulations of AlGaN/GaN epi-structures with and without an AlN exclusion layer. As seen, the electron concentration extends further in to the barrier layer without the AlN exclusion layer. However, the inclusion of a high band gap AlN layer may inhibit the formation of ohmic contacts [80, 81, 82]. Furthermore, controlling the exact thickness of the thin AlN layer is problematic and even small variations in thickness can have large implications on e.g. $n_s$ and ohmic contact resistance (which is another reason for using deeply recessed ohmic contacts). Table 3.4 lists literature values of achieved electron mobility for AlGaN/GaN systems with and without AlN exclusion layers, to show typical values for both cases.

**Optimized AlGaN/GaN interface** Using an optimized growth process, a sharp transition from GaN to AlGaN has been achieved, increasing electron mobility without including an AlN exclusion layer [83]. This can enable lower $R_C$ while maintaining a low $R_{sh}$ in epi-structures without AlN exclusion layers. In paper [B] such a structure was compared to an unoptimized AlGaN/GaN structure. The band diagram of the unoptimized structure is visualized in Fig. 3.5a as a diffuse interface that changes Al-content from 0 % to 30 % over a distance of 3 nm. It was found that the increased electron mobility was due to a lower alloy
Table 3.4: Literature values of room temperature 2DEG mobility and carrier concentration together with barrier design. All epi-structures have been grown on SiC substrates.

<table>
<thead>
<tr>
<th>Ref.</th>
<th>Growth method</th>
<th>Barrier</th>
<th>AlN-excl.</th>
<th>Mobility (cm²/Vs)</th>
<th>$n_s \cdot 10^{-13}$ (cm⁻²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>[28]</td>
<td>MOCVD</td>
<td>$\text{Al}<em>{0.22}\text{Ga}</em>{0.78}\text{N}$ 23 nm</td>
<td>2 nm</td>
<td>2300</td>
<td>1.0</td>
</tr>
<tr>
<td></td>
<td>MOCVD</td>
<td>$\text{Al}<em>{0.22}\text{Ga}</em>{0.78}\text{N}$ 23 nm</td>
<td>-</td>
<td>1600</td>
<td>-</td>
</tr>
<tr>
<td>[85]</td>
<td>MOCVD</td>
<td>$\text{Al}<em>{0.25}\text{Ga}</em>{0.75}\text{N}$ 29 nm</td>
<td>- nm</td>
<td>2200</td>
<td>1.1</td>
</tr>
<tr>
<td></td>
<td>MOCVD</td>
<td>$\text{Al}<em>{0.25}\text{Ga}</em>{0.75}\text{N}$ 29 nm</td>
<td>-</td>
<td>1300</td>
<td>0.9</td>
</tr>
<tr>
<td>[86]</td>
<td>MBE</td>
<td>$\text{Al}<em>{0.24}\text{Ga}</em>{0.76}\text{N}$ 30 nm</td>
<td>2 nm</td>
<td>1700</td>
<td>1.8</td>
</tr>
<tr>
<td></td>
<td>MBE</td>
<td>$\text{Al}<em>{0.24}\text{Ga}</em>{0.76}\text{N}$ 30 nm</td>
<td>-</td>
<td>1300</td>
<td>1.2</td>
</tr>
<tr>
<td>[83]</td>
<td>MOCVD</td>
<td>$\text{Al}<em>{0.17}\text{Ga}</em>{0.83}\text{N}$ 28 nm</td>
<td>2 nm</td>
<td>2200</td>
<td>0.8</td>
</tr>
<tr>
<td></td>
<td>MOCVD</td>
<td>$\text{Al}<em>{0.17}\text{Ga}</em>{0.83}\text{N}$ 28 nm</td>
<td>-</td>
<td>1700</td>
<td>0.6</td>
</tr>
</tbody>
</table>

disorder scattering at the sharp interface. Furthermore, it is shown that in the unoptimized structure the electrons penetrate in to the barrier layer in a larger degree, leading to increased $C_{gs}$ (extracted using the model in [84]) and increased dispersion at large drain bias. It is possible that the increased mobility seen in samples with an AlN exclusion layer is not only due to the large band gap of AlN increasing confinement. It could also be related to an improved interface quality created by the large difference in growth settings between GaN and AlN growth. It is worth noting that the mobility achieved in the optimized structure in paper [B] was lower than expected. This was due to the growth process being optimized for a different substrate size than what was used in paper [B]. In an optimized growth process, the sharp interface can yield a mobility greater than 2200 cm²/Vs [83].
For their intended applications GaN HEMTs are required to be able to operate at high frequency and deliver a high output power. Furthermore, a high reliability is of large importance. The buffer design can have a large effect on these properties. For a leaky buffer the reliability is expected to decrease [87], and high operating frequencies cannot be achieved if the buffer does not confine the electrons, limiting short channel effects [88]. Lastly, dispersion due to traps in the buffer can severely limit the output power, and time-variant effects, such as charging and discharging phenomena, is a major concern for large-signal applications.

Unintentionally doped GaN in usually n-type due to the large incorporation impurities during growth. Therefore, compensation doping is required in order to increase the resistivity of the GaN buffer and fulfill the requirements listed above. In these structures a trade off between low leakage and low dispersion has to be made since the compensating dopants are a large source of trapping centers. Field plates can reduce the effect of buffer traps by reducing the peak electric field [27]. However, the trapping cannot be completely removed since the compensating atoms are required in order to reduce the buffer leakage. A possible alternative to compensation doped GaN buffers is the use of back barriers. In this case the bottom confinement is achieved by the means of an energy barrier. Ideally, this would remove the need for compensation doping and a device free of buffer dispersion could
be achieved. However, due to limitations in achievable material quality this is not the case in practice.

This chapter deals with the two main approaches of buffer design described above; compensation doped GaN and back barriers. First, a brief introduction to trap characterization through drain current transient measurements is given in section 4.1. In section 4.2 compensation doping of GaN buffers is discussed. Of particular interest are C-doped buffers and therefore a more detailed analysis of these is given, based on the results presented in the appended papers [C], [D], and [E]. Fe-doping is also considered since this is the current industry standard for microwave HEMTs. Section 4.3 describes the use of back barriers, their associated advantages and disadvantages. Also included is previously unpublished work on epi-structures utilizing back barriers. The results are used as a basis for discussion regarding design choices associated with back barriers. Following this, a new type of epi-structure, utilizing a thin buffer, is briefly discussed in section 4.4. This structure does not require compensation doping and is using the AlN-exclusion layer as a type of back barrier. Lastly, the different buffer designs are evaluated in terms of achievable output power in section 4.5.

4.1 Trap characterization

Trap characterization is an important tool for understanding and improving GaN HEMT devices. The characterization can have two goals; understanding what is causing the trapping or understanding the traps’ effects on device performance. Commonly, pulsed-IV is used for trap characterization in GaN HEMTs. In this method, both $V_{GS}$ and $V_{DS}$ are pulsed from a quiescent, trap filling bias point to an active bias point where the current is measured. This method can quantify the effects of trapping to a certain degree but gives less information of the actual trapping mechanisms. Other methods that are commonly used are deep-level transient spectroscopy (DLTS) and photoluminescence, both of which mostly focus on understanding what are causing the trapping effects. The drain current transient (DCT) technique, which is explained below, can capture both aspects but is in this case mostly used for understanding the underlying defects creating the traps.

Surface reactions with atmospheric moisture The surface passivation should not only prevent electron trapping on the surface, it should also preserve the surface when exposed to different atmospheres
Figure 4.1: Pulsed-IV measurements performed on the same device in (a) nitrogen atmosphere, and (b) air atmosphere. Four different quiescent bias points are used ($V_{GSQ}, V_{DSQ}$).

and protect from other contaminants. For example, atmospheric moisture might oxidize the surface with the aid of large electrical fields [89, 90]. In this thesis, similar effects have been observed for devices with SiN passivation. In Fig. 4.1 results from pulsed-IV measurements on the same device in different atmospheres are shown. In N$_2$ atmosphere the current decreases in an expected way with increasing quiescent drain bias. However, in air ambient almost total current collapse is measured for the two highest quiescent drain biases. In these cases it is believed that the large electric field enables moisture from the atmosphere to penetrate at the metal-SiN interface on the gate and drain edges. The moisture reacts with the surface of the barrier, changing the local electrical potential and in so the number of carriers in the 2DEG. This process seems to be reversible since the behavior in Fig. 4.1a is recovered after re-introducing a N$_2$ ambient. Therefore, the buffer trap characterizations have been performed in a N$_2$ ambient to prevent these effects from interfering with the measurements.

**DCT-analysis** The main trap characterization method used in this thesis is the drain current transient (DCT) technique. In this, the transistor is kept at a high stress bias point for a period of time, allowing traps to be filled. Following this, the bias is quickly switched to a low stress point, where the drain current is monitored for an extended time. When electrons are emitted from the traps, an increase in the drain current is observed. Depending on which high stress bias point is
chosen, traps in different regions of the transistor can be filled. Using a large drain bias with the gate pinched is believed to mostly fill traps in the buffer region [91]. An example of a DCT measurement with a single trap level can be seen in Fig. 4.2a. From the measurement data the trap time constant can be extracted by fitting the following equation;

\[
\frac{I_{DS}}{I_{DS,q}} = 1 - \sum_{i=1}^{N} \alpha_i \cdot \exp \left( - \frac{t}{\tau_i} \right)^{\beta_i}.
\]  

(4.1)

This model has been found to give the most accurate results for extraction of time constants [92]. Here, \(I_{DS}/I_{DS,q}\) is the drain current normalized by the quiescent drain current, \(\alpha_i\) is the amplitude of the trapping effect, \(\tau_i\) is the trapping/de-trapping time constant, \(\beta_i\) is the stretching term and \(N\) is the number of traps. The stretching term can give additional information regarding the defect responsible for the trap level. For a point defect \(\beta = 1\) and a standard exponential behavior is measured. However, for more complex emission processes \(\beta\) can be less than 1. For example, a small \(\beta\) has been related to the trapping/de-trapping kinetics being governed by hopping [93], or tunneling [94]. A small \(\beta\) has also been connected to the trapping centers forming a continuous distribution of energy levels rather than a discrete level [95].
**Arrhenius behavior**  To characterize traps it is useful to extract their activation energy \((E_A)\) and capture cross sections \((\sigma_n)\). For a trapped electron being emitted to the conduction band through a thermally activated process the emission rate is given by;

\[
e_n = \sigma_n v_{th} N_C \cdot \exp(-E_A/k_B T).  \tag{4.2}
\]

Here, \(v_{th}\) is the thermal velocity, \(N_C\) is the effective density of states in the conduction band, \(k_B\) is Boltzmann’s constant, and \(T\) is the absolute temperature. \(E_A\) and \(\sigma_n\) can be extracted by performing DCT measurements at different temperatures and extracting \(e_n\) to construct an Arrhenius plot, as seen in Fig. 4.2b. In the Arrhenius plot \(\ln(T^2/e_n)\) is plotted versus \(1/k_B T\). Using Eq. (4.2), \(\ln(T^2/e_n)\) can be re-written as;

\[
\ln \left( \frac{T^2 \exp(E_A/k_B T)}{(T^2 N_{C0}) \sigma_n v_{th}} \right) = E_A/k_B T - \ln(N_{C0} \sigma_n v_{th}),  \tag{4.3}
\]

where \(N_{C0}\) is the temperature independent part of \(N_C\). When plotted versus \(1/k_B T\) a line \((y = kx + m)\) with \(k = E_A\) and \(m = -\ln(N_{C0} \sigma_n v_{th})\) will be obtained. \(\sigma_n\) can then be calculated since \(N_{C0}\) and \(v_{th}\) are known for GaN. Specific defects can be identified using \(E_A\) and \(\sigma_n\) since these should be unique. A compilation of \(E_A\) and \(\sigma_n\) for several traps found in GaN and their assumed origin can be found in [92].

**Characterization of extended defects**  Point defects in semiconductors do not interact with each other, making each filled trap’s emission time well described by Eq. (4.2) using a single \(E_A\) and \(\sigma_n\). For extended defects the behaviour is more complex. Firstly, trapped electrons at an extended defect may change the local potential and in so change to effective capture cross section of the trap center [96]. Secondly, trap states along extended defects may have capture cross sections varying over several orders of magnitude [97]. These effects can be investigated through DCT measurements by varying the time spent in the trap filling bias condition (filling time variation). For longer filling times, traps with smaller \(\sigma_n\) may be trapped, leading to a large variation in the DCT signature for different filling times. In a sense, these measurements are similar to DLTS, although the DCT measurements is more versatile since both the gate and drain voltages can be changed in order to stress different areas of the device. The theory described above is the basis for the DCT analysis performed in paper [E]. For
further reading on the DCT technique [92] and [98] are highly recommended.

4.2 Compensation doped GaN

Due to the large band gap of GaN the intrinsic carrier concentration is very low (\(\sim 10^{-10} \text{ cm}^{-3}\)). However, as a result of the high growth temperatures, unwanted material from e.g. the growth chamber or substrate give large concentrations of impurities in the crystals. Two common impurities are Si and O, both of which are shallow donors in GaN [99]. Consequently, unintentionally doped (uid) GaN is often n-type. As explained in chapter 2.2 this is an issue for HEMT devices since the electrons in the 2DEG needs to be confined to minimize short channel effects and buffer leakage [88]. Hence, the excess electrons needs to be decreased in order to increase the resistivity of the buffer.

GaN buffers were initially rendered highly resistive by introducing a high density of defects in the buffer, but this also reduced the crystal quality in the 2DEG region, leading to decreased mobility [86, 100]. Currently, compensation doping using deep acceptors is the standard method to achieve high resistive buffers. In this method the compensation atoms can be minimized close to the barrier, maximizing \(n_s\) and \(\mu\) in the 2DEG. The two most commonly used acceptors are Fe and C, which will be described more in detail in the following paragraphs. Other dopants forming deep acceptors in GaN are for example magnesium [101] or beryllium [102], but these are rarely used in HEMT devices.

Fe-doped GaN buffers

Fe-doped buffers are the current industry standard for microwave GaN HEMTs due to their high resistivity and high associated output power. To grow Fe-doped GaN using MOCVD, the Fe atoms need to be introduced in the growth chamber using a precursor. From a growth perspective, an advantage of Fe-doping is the large process window, giving a stable, reproducible growth process [103]. A disadvantage is the growth related memory effect which makes rapid transitions from high to low Fe-concentrations difficult to achieve. This is due to Fe segregating on the GaN surface during growth. Once the Fe-precursor has been turned off the remaining Fe on the surface will be incorporated with an exponential tail in the subsequently grown GaN [104].
Fe-doped GaN commonly shows a Fermi level pinning of around 0.6 eV below the conduction band [105, 106]. However, this level is not believed to be related to Fe in itself, but rather that the presence of this level is enhanced by the Fe-incorporation [107]. The actual Fe-level is believed to be located deeper in the energy band [108]. The 0.6 eV level is regularly seen in devices with Fe-doped buffers, leading to increased on-resistance and reduced drain current. Furthermore, this level has a room temperature emission time in the millisecond range. Therefore, it can have a large performance impact in applications that are sensitive to transient effects [109].

Microwave HEMTs with Fe-doped buffers  Compared to unintentionally doped buffers, Fe-doping has been found to limit the achievable output power [110]. However, a low Fe-concentration has been found to decrease short-channel effects while maintaining a high output power [111]. The highest reported output power for GaN HEMTs have been achieved using an Fe-doped buffer (40 W/mm at 4 GHz under pulsed conditions) [26]. However, the exceptional result is mostly attributed to field plate optimization and no mention of reliability is made for these extreme operating conditions. An interesting approach to the growth related memory effects is presented in [112]. Here, a thin uid GaN channel is grown on a free standing Fe-doped GaN substrate, ensuring a rapid transition from high to low Fe-concentration. This results in 9.7 W/mm output power at 10 GHz, although in this case the excellent results should probably rather be attributed to the improved crystal quality and heat transport enabled by the GaN substrate rather than the Fe-doping profile.

Overall, Fe-doped GaN buffers are not as frequently investigated as C-doped buffers. This is probably due to Fe-doping suffering from fewer issues compared to C-doped buffers but also since C-doping is common in the commercially larger field of power electronics. As a result, the behavior of Fe-doped buffers in microwave applications can be predicted rather well whereas the underlying mechanisms are not as well understood. In this thesis, only one Fe-doped epi-structure has been reported (in paper [E]), grown by Cree Inc.. The purpose of this sample was to benchmark the HEMT process on an industry standard epi-structure. Generally, it offered a good trade off between dispersive effects and leakage. However, it also suffered from the characteristic 0.6 eV level which introduced knee-walkout effects and current collapse, and in so
reducing the achievable output power. Clearly, even though Fe-doped buffers generally give the best performance in microwave applications, problems still remain.

**C-doped GaN buffers**

Highly C-doped GaN generally offers a higher resistivity compared to Fe-doped GaN [113]. Therefore, C-doped buffers are most commonly used in power applications in which a highly resistive buffer is crucial in order to enhance the breakdown voltage [114]. In this thesis, C-doped buffers have been investigated for microwave applications, where a lower C-concentration is generally required due to the lower operating voltages. One of the advantages of C-doping is that it does not suffer from the same memory effects as explained for Fe incorporation. Instead, rapid changes from high to low C-concentration are readily achievable. For GaN films grown with MOCVD, the C-concentration may be controlled by managing the incorporation of residual C in the chamber. The residual C mainly originates from the Ga precursor (trimethyl gallium) and the incorporation rate is most commonly controlled by varying the growth pressure or temperature. Generally, at low pressure and at low temperature the C incorporation increases [115]. However, the same growth conditions can also lead to a degraded crystal quality, with increased presence of dislocations [116, 117]. This gives a trade off between high C-concentration and high crystalline quality. It is possible to avoid these issues by incorporating C using a C-carrying gas. For example, this was done in paper [a] using propane. In this case the growth settings can be optimized for high quality GaN and the C-concentration can be controlled by changing the flow rate of the C-precursor.

**Incorporation of C in the GaN crystal** Depending on growth conditions, C may be incorporated in a number of different places in the GaN crystal [118]. From physical simulations it has been found that when C is substituted with a Ga atom (C$_{Ga}$), a shallow donor in the conduction band is formed [119]. When C is substituted for an N atom (C$_{N}$), a deep acceptor state $\sim$0.9 eV above the valence band maximum is formed [120]. C may also be incorporated in an interstitial position. Although, among these configurations C$_{N}$ is the most energetically favourable for most growth conditions [120]. It is also the C$_{N}$ configuration that is believed to be responsible for the increased resistivity observed for C-doped GaN layers, where the deep
acceptor level works as a compensation dopant [108]. However, the exact mechanisms are still not fully understood.

The ideal conditions examined in physical simulations generally do not account for defects, which are always present in real samples. These defects can form separate energy levels [121], or even change the incorporation of C in the crystal. For example, dislocations commonly function as attractors of defects in semiconductor materials [122]. This means that other impurities are accumulated at the dislocation. The process is called gettering and can be used to "clean" semiconductors of unwanted dopants. Gettering of impurity atoms to dislocations has also been reported for GaN [33, 123]. In these cases the impurity atoms are decorating the dislocations, forming states and changing the charge of the dislocation cores [123]. As proposed in paper [E], to fully control the incorporation of C in the GaN crystal, residual C-doping is probably not a feasible option since many variables are changed when changing C-concentration. From this perspective extrinsic C-doping is more promising since the general growth conditions and the C-incorporation are easier to separate.

Highly C-doped GaN buffers For power applications, high C-concentrations (\( \sim 10^{19} \text{cm}^{-3} \)) are required in order to limit breakdown [114]. At these C-concentrations GaN has been shown to become p-type [124]. This can have large implications on dispersion in HEMT structures [125, 126]. The problem arises due to a pn-diode formed between the p-type GaN and the 2DEG channel region. For fast switching from large to small drain biases, electrons can get trapped in the p-type region, effectively forming a back-biased pn-diode. In this case, the trapped electrons have no obvious way of returning to the 2DEG due to the electrostatic barrier. It has been argued that dislocations could form a leakage path through the pn-diode barrier for the trapped electrons [127]. This has been partially verified in experiments with devices of different surface area [128]. Here, smaller devices display larger dispersive effects and a larger device-to-device spread compared to larger devices. This is attributed to a lateral charge transport mechanism that is highly localized and distributed with a \( \sim 100 \text{\mu m} \) scale of separation. The large distance excludes dislocation as a possible candidate for these vertical leakage paths since these are much more abundant. However, as discussed in [33], dislocations can getter C from the surrounding GaN, forming a C-depleted region around itself. When two disloca-
tions are close to each other a "deep carbon depletion"-region may be formed, drastically decreasing vertical breakdown. Possibly, the same mechanism could be responsible for the behavior found in [128] since the separation of the "deep depletion"-regions were found to be around 10 µm.

**Moderately C-doped GaN buffers** The theories on trapping mechanisms in HEMTs using highly C-doped, p-type, GaN are indeed interesting. However, for microwave HEMTs (the topic of this thesis) vertical breakdown is rarely an issue so lower C-concentrations are generally used. In [113] it was found that GaN shifted from n-type to p-type at a C-concentration of $1.6 - 2.9 \cdot 10^{18} \text{ cm}^{-3}$. In a general GaN sample the shift from n-type to p-type should not only depend on the C-concentration but also on the background impurity levels. For lower Si and O impurity levels a lower C-concentration is required in order to render GaN p-type.

**Fermi level position in moderately C-doped GaN** Kelvin probe force microscope (KPFM) measurements (similar to those in [113]) have been used to estimate the Fermi level’s position in a typical C-doped buffer used in this thesis. The GaN layer has been doped using a residual process to a C-concentration of $1 \cdot 10^{18} \text{ cm}^{-3}$. An Fe-doped sample was also measured for comparison. The Fe-concentration is in this case unknown due to the proprietary doping process. However, the Fe-doped sample is still interesting as a reference considering the Fermi level in Fe-doped GaN is usually pinned at 0.6 eV below the conduction band. The samples were cleaned using diluted (1:10) HCl and HF solutions to remove potential surface oxides. A Ti/Au-stack (5/100 nm) was deposited directly on the surface. This metal stack has been shown to have a work function of 4.95 eV [129], thus providing a reference potential value. KPFM scans were performed across the edge of the deposited metal, including both the GaN and metal surfaces in a single scan, Fig. 4.3. This way the potential difference between the metal and the GaN layer can be measured. The Fermi level position is calculated using the following equation:

$$\Delta E_F = \phi_{Ti/Au} + e\Delta V - \chi_{GaN} - \Delta \phi.$$  \hspace{1cm} (4.4)

Here, $\Delta E_F$ is the Fermi level to conduction band distance, $\phi_{Ti/Au}$ is the work function of the metal stack (4.95 eV), $e$ is the electron charge,
ΔV is the measured potential difference between the GaN surface and the Ti/Au metal stack, χ_{GaN} is the electron affinity of GaN, and Δφ is the net band bending caused by surface or dipole charges. From [113]; χ_{GaN} = 3.5 eV for a cleaned surface and Δφ = 0.4 eV for semi-insulating GaN. Fig. 4.3 gives a ΔV of roughly -0.4 V for the C-doped sample and -0.05 V for the Fe-doped. This results in a Fermi level position 0.65 eV and 1 eV below the conduction band for the C-doped and Fe-doped GaN respectively. In a hand waving argument, 0.4 eV can be taken a rough uncertainty in the measurement since a value of 0.6 eV is expected for the Fe-doped sample. Regardless, it is clear that the C-doped GaN is more n-type than the Fe-doped GaN in this case. This was also confirmed in mesa isolation measurements where the Fe-doped buffer offered 20 times lower leakage currents at 200 V.

**C-doped buffers for microwave applications** In the literature only a handful of studies have investigated the use of C-doped buffers for microwave applications [130, 131, 132, 133]. In these it is not verified
whether the GaN buffer is p-type or n-type. For C-concentrations low enough to form n-type GaN (moderately C-doped GaN) no pn-diode should exist between the GaN buffer and the 2DEG. Consequently, a different trapping behavior than described for highly C-doped GaN buffers could be expected. Using the results from the KPFM measurements and what was found in [113], a reasonable assumption is that C-concentrations $\leq 1 \cdot 10^{18} \text{ cm}^{-3}$ should give n-type GaN. From the references this leaves [130] and [132]. In both of these cases a clear reduction in output power is measured for increasing C-concentration in the buffer. However, no deeper analysis on the origin of the trapping effects have been performed.

One of the advantages with C-doped buffers is the possibility to tailor the doping profile with a high precision. In paper [C] this was used to develop a stepped C-profile, with low C-concentration in vicinity of the 2DEG and a high concentration deep in the buffer. The stepped profile (Stepped:C) was compared to an unintentionally doped sample (Low:C) and a sample with a constant, high C-concentration (High:C). The exact doping profiles are shown in Fig.4.4. The C-concentrations in the three samples are expected to give n-type GaN. The three epi-structures were evaluated with respect to leakage and dispersion. Figures of merit such as drain induced barrier lowering (DIBL) and dynamic $R_{ON}$ were extracted. DIBL is a measure of how much the pinch-off voltage shifts with increasing $V_{DS}$ and give a measure of confinement. Pulsed-IV measurements were used to extract the dynamic $R_{ON}$ as the increase (in %) between the quiescent bias points $(V_{GSQ},V_{DSQ}) = (0,0)$ and (-6,15) V. It was found that the stepped C-profile gave a good trade off between short channel effects, leakage, and dispersion, as indicated by a low value of DIBL (1.2 mV/V) and dynamic $R_{ON}$ (35 %). Corresponding values for High:C and Low:C were 0.1 mV/V and 750 %, and 22.4 mV/V and 10 % respectively. Even though an extensive trapping analysis was performed, no clear results regarding the origin of the C-induced trapping was found.

**Buffer traps in n-type, C-doped GaN** The work in paper [C] was continued in paper [E]. A more thorough trap characterization was performed in order to understand which trapping centers are important in n-type, C-doped buffers. Here, two C-doped epi-structures were investigated, Stepped:C and Exp:C (see Fig. 4.4 for exact profiles). Low:C from paper [C] was also used to facilitate further discussion. Tem-
Figure 4.4: Doping profiles for the C-doped epi-structures presented in this thesis.

Temperature and filling time dependent DCT measurements were used to extract three traps, denoted T1, T2 and T3. The DCT measurements for Exp:C are presented in Fig. 4.5, where the three traps have been indicated at their respective peak. T1 had a room temperature (RT) emission time of $\sim 50 \, \mu s$, for T2 the RT emission time was $\sim 5 \, s$, and for T3 $\sim 500 \, ms$.

The processes responsible for the three traps are summarized in Fig. 4.6. T1 is associated with the largest current decrease and seems to be related to trapping at C-clustering around dislocations. This is supported by an increasing amplitude as well as a widening of the peak of T1 for longer filling times, indicating that the trap is due to extended defects. Furthermore, by comparing the amplitude of T1 between the three samples it is found to correlate with a high C-concentration. Additionally, gettering of C to dislocations is a well known effect in GaN [33]. The main current transport mechanism for T1 is believed to be hopping or tunneling as indicated by an activation energy close to 0 eV. In paper [E] it is proposed that a reduction of the dislocation density might be a way to reduce the impact of T1.

T2 and T3 only account for a few percent of the total current decrease but the mechanisms behind them are interesting. In a sense, the process is similar to the problems associated with the pn-diode present for high C-concentrations. The amplitude of T3 is negative and is believed to be related to hole emission from the $C_N$ level. As indicated in Fig. 4.6, band bending will occur at the GaN/AlN-nucleation interface due to the polarization gradient present there. The band bending will create vacant $C_N$ levels which can be filled by electrical stimulation, as
Figure 4.5: (a) Temperature and (b) filling time dependent DCT measurements for Exp:C from paper [E]. The high stress voltage was \( (V_{GS}, V_{DS}) = (V_P - 2.50) \) V and the low stress voltage was \( (1.7) \) V. A filling time of 1 ms was used in (a) and the measurements in (b) were performed at 20 °C.

Figure 4.6: Schematic figure depicting the trapping processes of T1, T2, and T3. The band diagram shows the different trap levels (C-clusters (●), \( C_N \) (○), and defect band (DB)), as well as the intrinsic and approximate Fermi levels in our C-doped samples.
explained in [126]. The trapped electrons at the GaN/AlN interface are transported through the GaN buffer by means of the recently discovered defect band [121]. The leakage process is registered as trap T2 which has the same non-Arrhenius behavior as found in [121].

**Extrinsic C-doping for a reduced dislocation density** By controlling the C-concentration using a C-carrying gas, a lower dislocation density could be achieved for the same C-concentration. In this way, the importance of the T1 trap might be reduced. It is also possible that the different growth conditions could alter the gettering rate of the C atoms. An initial experiment using extrinsic C-doping is presented in paper [D]. In this paper, propane is used as C-carrying gas and the C-profile in Fig. 4.4 is achieved. The buffer supplied an excellent confinement resulting in a DIBL of 0.13 mV/V at $V_{DS} = 30$ V. However, large dispersive effects leading to knee-walkout, and thus limited output power, were also present. The C-concentration of Extrinsic:C was slightly larger compared to what was used in the residually doped samples in paper [E]. Probably, the larger C-concentration counteracted the lower dislocation density in this case. Another possibility is that the larger C-concentration rendered the GaN p-type, giving rise to the pn-diode related issues described for the highly C-doped buffers. Without further extrinsically doped samples to compare with it is difficult to draw any clear conclusions given the different growth conditions and C-profiles used in the two cases.

4.3 **Back-barrier**

A different way to increase the confinement is to introduce a back-barrier. The back-barrier is a high energy barrier that prevents the electrons from extending down into the heterostructure at larger drain biases. In this case the 2DEG has large energy barriers on both sides, sometimes called double heterostructure- (DH-) HEMT. To exemplify, the band diagram of an AlGaN/GaN/AlGaN structure, compared to a regular AlGaN/GaN structure, is shown in Fig. 4.7. In this particular case, the electron concentration decreases by $\sim 20\%$ by including the back-barrier. However, the confinement is increased, making it ideal for high frequency operation. This is also what the back-barrier is mostly used for in the literature. For example, the highest reported $f_T$ and $f_{max}$ for a GaN based HEMT has been achieved using an AlN/GaN/AlGaN heterostructure [2]. Several other devices showing impressive high fre-
Figure 4.7: Simulated conduction band energies and electron densities for an AlGaN/GaN heterostructure with and without an Al$_{0.05}$Ga$_{0.95}$N back-barrier.

Figurary performance using AlGaN or InGaN back-barriers have also been reported [52, 134, 135].

However, some drawbacks are also associated with the use of back-barriers. For example, Al$_x$Ga$_{1-x}$N has a significantly lower thermal conductance compared to GaN and AlN. This is attributed to an increase in phonon scattering caused by the increased disorder in the crystal [6]. Therefore, devices with Al$_x$Ga$_{1-x}$N back-barriers often show an obvious decrease in drain currents at large dissipated power [134, 136, 137]. The effective thermal conductance can be increased by thinning down the back-barrier layer and growing a GaN buffer underneath (as explained in Chapter 2 the whole epi-structure still needs to be roughly 2 $\mu$m thick in order to get a good crystal quality). However, this can introduce a parasitic channel in the interface between the AlGaN back-barrier and the GaN buffer. If this design is chosen the parasitic channel is usually removed by introducing deep acceptors in the GaN buffer [131, 138].

In theory, the back-barrier structure should be able to minimize trapping effects since no deep acceptors are required to get a good confinement. However, the Al$_x$Ga$_{1-x}$N ternary alloy is intrinsically more difficult to grow with a high crystal quality [139]. As described above, crystal defects can also contribute extensively to trapping effects. Furthermore, even though dopants are not required, the background doping for AlGaN is usually higher compared to GaN growth [140]. Generally,
trapping in devices utilizing back barriers has not been as extensively investigated as for compensation doped GaN buffers. Therefore, important trapping centers in back barriers are difficult to find in the literature.

**Back barrier materials in this thesis** HEMTs on epi-structures with AlGaN back-barriers were processed in order to gain further knowledge of important trapping effects. The devices were the first try on back barrier structures with the main idea to investigate the effect of the uid GaN channel thickness on different performance figures. Two epi-structures with designs described in Fig. 4.8 were used. BB1 had a uid GaN thickness of 50 nm and BB2 100 nm. A large C-concentration in the AlGaN back-barrier was included to suppress leakage through this layer. Although, in hindsight, these values are probably too large. Regardless, the GaN channel thickness did not affect the 2DEG significantly and both structures showed reasonable values of sheet carrier density and a high electron mobility, Fig. 4.8.

**DC-characteristics** DC-characteristics were measured on devices with $L_G = 100$ nm in order to verify the functionality of the HEMTs. The saturated drain current ($I_{DSS}$, $I_{DS}$ at $V_{GS} = 1$ V) was 0.6 A/mm and 0.8 A/mm for BB1 and BB2 respectively. Comparing to a regular AlGaN/GaN structure with similar 2DEG properties this current
is lower than expected. This could be due to the back-barrier limiting the band bending in the uid GaN region. This would also explain the lower current in BB1 since this sample has a thinner GaN channel. The maximum transconductance \( g_m \) was around 350 mS/mm in both samples even though BB2 had a larger current. This was a result of the lower pinch-off voltage in BB2 (-2.0 and -2.5 V for BB1 and BB2 respectively). Overall, BB1 and BB2 were found to function properly although their performance were worse compared to a regular AlGaN/GaN epi-structure without back barrier.

**Trapping evaluation** Filling time dependent DCT measurements were performed to investigate trapping effects, see Fig. 4.9. An off-state voltage of \((V_p - 2.30)\) V was used in order facilitate complete current recovery after 10 s. The DCT signatures of both BB1 and BB2 shared similarities with the C-doped samples discussed above. A fast time constant, similar to T1, with a large dependence on filling time was present in both samples. A slow time constant was also registered. However, for the slow time constant no dependence on filling time was found. With the discussion regarding the C-doped buffers in mind, it seems likely that the fast time constant is related to trapping at dislocations. The origin of the slow trap is more difficult to explain, although it is less important in terms of associated current decrease. Comparing BB1 to BB2 the current decrease is obviously much larger in BB1. This most likely means that the dislocations responsible for the trapping is located in the back barrier since this is closer to the 2DEG in BB1. Since the back barrier is C-doped it is possible that the same C-clustering as discussed for C-doped GaN buffers is present also in these structures.

4.4 Thin buffer

Many of the problems associated with both compensation doped GaN buffers and back barriers are due to the fact that the buffer needs to be grown to a thickness of around 2 µm. If a high quality GaN layer could be achieved for a much lower thickness, the AlN-nucleation layer would function as a back-barrier and no compensation doping would be required. Furthermore, growth times would be decreased leading to reduced epi-wafer costs. However, worse thermal behavior could be expected due to the smaller separation between the device and the high thermal boundary resistance of the AlN-nucleation layer [141].
a thin GaN buffer has previously been investigated with poor results [142, 143, 144]. In these cases the low crystalline quality impede the HEMT performance significantly. However, using an optimized AlN-nucleation process [5], thin HEMT structures of high quality have been achieved in this thesis. The epi-structure design is presented in Fig. 4.10. For an epi-structure with a 200 nm thick GaN layer excellent values of $\mu$ and $n_s$ were measured ($2050 \text{ cm}^2/\text{Vs}, 1.1 \cdot 10^{13} \text{ cm}^{-2}$) using van der Pauw structures, showing no indication of low crystalline quality around the 2DEG. HEMT devices were fabricated in order to evaluate the performance also for larger electric fields.

**DC-characteristics** The output characteristics are presented in Fig. 4.11a. The low on-resistance was achieved through a combination of low $R_{sh}$ and low $R_C$ (0.3 $\Omega$mm). No short channel effects are present, as indicated by an extracted DIBL of 1.0 mV/V at 27 V. This value can be compared to 1.2 mV/V for a C-doped buffer with $\sim 2 \mu$m thick buffer (paper [C]). Furthermore, the thermal performance does not
**Figure 4.10:** Design of the thin HEMT epi-structure.

**Figure 4.11:** Output (a) and transfer (b) characteristics measured for devices with $L_g = 200$ nm. In (a) $\Delta V_{GS} = 0.5$ V and the largest current is measured for $V_{GS} = 1$ V. In (b) the solid line is $I_{DS}$ and the dashed line is $I_{GS}$, the measurements are performed at $V_{DS} = 10$ V.

seem to be severely degraded by the thin GaN buffer. In the transfer characteristics a clear pinch-off behavior and a large transconductance (450 mS/mm) are found, Fig. 4.11b. For compensation doped buffers using the same barrier design the transconductance is usually closer to 400 mS/mm (paper [E]).

**DCT evaluation**  An extensive DCT evaluation was performed in order to identify important trapping processes. Temperature dependent DCT measurements are presented in Fig. 4.12a. One trap, with and emission time of around 10 $\mu$s were identified. However, no temperature dependence was seen. This most likely implies that the trap mechanism
Figure 4.12: (a) Temperature and (b) filling time dependent DCT measurements for the thin buffer sample. The high stress voltage was \((V_{GS}, V_{DS}) = (V_{P-2,50}) \) V and the low stress voltage was \((1,7) \) V. A filling time of 1 ms was used in (a) and the measurements in (b) were performed at 20 °C.

is governed by tunneling [145].

Filling time dependent measurements are performed at room temperature to gain further insight into the trap’s origin, Fig. 4.12b. A large dependence on filling time is found for the amplitude of the trap, indicating that it is due to extended defects. Probably, the trap is due to dislocations in the AlN-nucleation layer which are accessed through a tunneling process.

4.5 The impact of buffer design on output power

Load-pull measurements were performed as an application relevant comparison between the various buffer designs that have been investigated in this thesis, Table 4.1. The measurements were performed at 30 GHz
with a quiescent $V_{DS}$ of 10 and 30 V, and a quiescent drain current of around 10 % of $I_{DSS}$. The load and source impedance were optimized for maximum output power. For comparison, Table 4.2 contains literature values of achievable output power at similar frequencies for the different buffer designs.

Low:C does not suffer from buffer related dispersive effects and therefore deliver the largest output power of all samples in this thesis. This was somewhat unexpected given the similar performance to Stepped:C in paper [C]. However, the load-pull measurements in paper [C] were performed at $V_{DSQ} = 15$ V, for which the trapping effects in Stepped:C were limited. This clearly exemplifies the importance of evaluating buffer trapping effects at relevant operating voltages. Comparing to literature values of uid GaN buffers the Low:C sample offers exceptional performance. However, for all of these devices the efficiency is fairly limited, most likely due to difficulties in reaching pinch-off. Therefore, uid GaN buffers are not desirable in real applications since this will decrease their reliability [87].

The C-doped devices in this thesis performed similarly (except for High:C which is also limited by a small gain at this frequency). For the low $V_{DSQ}$ all of them supplied output powers in line of what is expected from the DC-data. However, for the large $V_{DSQ}$ they all suffered from trapping effects, limiting the maximum output power and decreasing the efficiency. Compared to the literature values in [133], the C-doped devices in this thesis perform significantly worse. This should partially be related to the larger $n_s$ ($1.8 \cdot 10^{13}$ cm$^{-2}$) and thinner barrier layer (giving less short channel effects) in [133], but could also be related to a different doping profile which unfortunately is not disclosed. The Fe-doped device showed both increased output power and efficiency when increasing $V_{DSQ}$ from 10 to 30 V. However, compared to Low:C the output power is obviously lower, indicating that the Fe-induced trapping limits the output power in this case. Similar results have been found in [110, 111].

BB2 offered performance in line with the C-doped GaN buffers while the output power of BB1 was very limited. This was expected from the lower current of BB1 and the extensive trapping found in Fig. 4.9. Comparing to the literature, the output power of BB2 is similar to that reported in [149] but significantly lower than in [150]. In [149] the AlGaN back barrier was grown directly on the nucleation layer (similar to this work) but in [150] the AlGaN back barrier was combined with a
C-doped GaN buffer. Possibly, the lower output power for the devices in this thesis (and in [149]) can be explained by thermal issues or increased trapping due to worse crystalline quality.

Devices on the thin HEMT structure showed excellent performance, similar to the Exp:Fe sample. However, comparing to the Low:C sample it is clear that the trap identified in the DCT measurements limit performance. This is further indicated by the decrease in efficiency when increasing $V_{DSQ}$ from 10 V to 30 V. To improve the output power further, structural improvements of the AlN-nucleation layer should be prioritized. Nevertheless, the thin HEMT structure offers competitive performance already at this stage.

In conclusion, the results in this thesis indicate that Fe-doped buffers remain the benchmark which other buffer designs should be compared to. The uid GaN buffers supply the highest output power but is limited in efficiency and reliability. The extensive trapping effects in C-doped buffers needs to be addressed in order establish this as a viable option for microwave applications. Back barrier designs also requires further optimization to minimize trapping and thermal effects. The thin buffer structure is an interesting option that showed performance in line with the Fe-doped buffer. However, also in this case the trapping effects reduced the achievable output power. For C-doped GaN, AlGaN back barrier, and thin buffer designs, improving the crystalline quality is believed to be a possible route for enhanced performance.
<table>
<thead>
<tr>
<th>Device [Ref.]</th>
<th>( V_{DSQ} = 10 \text{ V} )</th>
<th>( V_{DSQ} = 30 \text{ V} )</th>
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<tbody>
<tr>
<td>Low:C [C]</td>
<td>1.8 (W/mm) 20 (%)</td>
<td>5.7 (W/mm) 20 (%)</td>
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<tr>
<td>High:C [C]</td>
<td>0.3 (W/mm) 3 (%)</td>
<td>0.1 (W/mm) 1 (%)</td>
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<tr>
<td>Stepped:C [C]</td>
<td>1.5 (W/mm) 30 (%)</td>
<td>3.3 (W/mm) 23 (%)</td>
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<td>Extrinsic:C [D]</td>
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<td>2.0 (W/mm) 15 (%)</td>
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<tr>
<td>Exp:C [E]</td>
<td>1.8 (W/mm) 26 (%)</td>
<td>2.6 (W/mm) 15 (%)</td>
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<tr>
<td>Stepped:C [E]</td>
<td>1.6 (W/mm) 30 (%)</td>
<td>2.5 (W/mm) 15 (%)</td>
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<tr>
<td>Exp:Fe [E]</td>
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<td>3.9 (W/mm) 25 (%)</td>
</tr>
<tr>
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<td>0.7 (W/mm) 30 (%)</td>
<td>0.5 (W/mm) 5 (%)</td>
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<tr>
<td>BB2</td>
<td>1.1 (W/mm) 30 (%)</td>
<td>2.7 (W/mm) 20 (%)</td>
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<tr>
<td>Thin buffer</td>
<td>1.8 (W/mm) 35 (%)</td>
<td>3.9 (W/mm) 25 (%)</td>
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</table>

Table 4.1: Load-pull measurements for devices with various buffer designs. Listed are the maximum output power and associated power added efficiency at two quiescent bias points. The devices have a gate length of 100 nm and source drain distance of \( \sim 2.8 \text{ \mu m} \).
Table 4.2: Literature values of achievable output power for devices with different buffer designs.

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<th>freq. (GHz)</th>
<th>$P_{out}$ (W/mm)</th>
<th>PAE (%)</th>
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<td></td>
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<td>15</td>
<td>18</td>
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<td>28</td>
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<td></td>
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<tr>
<td>[148]</td>
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<td>15</td>
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<td></td>
<td>(2/25 nm)</td>
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<td><strong>C-doped GaN buffers</strong></td>
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<tr>
<td>[149]</td>
<td>In$<em>{0.17}$Al$</em>{0.83}$N/AlN</td>
<td>20</td>
<td>29</td>
<td>2.1</td>
<td>22</td>
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<tr>
<td></td>
<td>(7/1 nm)</td>
<td></td>
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<tr>
<td>[150]</td>
<td>InAlGaN/AlN</td>
<td>20</td>
<td>30</td>
<td>6.0</td>
<td>36</td>
</tr>
<tr>
<td></td>
<td>(6/1 nm)</td>
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<td></td>
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</tr>
</tbody>
</table>
Chapter 5

Conclusions and future outlook

The aim of this thesis has been to optimize the buffer design to improve the performance in terms of output power and time variant effects in GaN HEMTs for microwave applications. The thesis has also presented work done to reduce losses in GaN HEMT technology, in the form of low resistive ohmic contacts and improved barrier quality.

A Ta-based recessed ohmic contact have been presented which show close to state of the art performance with an \( R_C \) of 0.14 \( \Omega \text{mm} \). Compared to the most commonly used, Ti/Al/Ni/Au contact, the contact presented in this thesis requires lower anneal temperature (550-600 °C) leading to better edge acuity and no degradation of the 2DEG sheet resistance. The lowest contact resistance was found for a recess depth close to the barrier thickness. A general problem for recess etched contacts is the optimization of the etching depth and the repeatability of the etching process. Future work should focus on increasing the repeatability of the ohmic process rather than just aiming for low \( R_C \)’s. The results presented in this thesis also hint that a more repeatable process might be possible by etching deeper, well past the barrier layer. Investigations into these areas are currently ongoing, showing promising results.

The higher mobility associated with the inclusion of an AlN-exclusion layer (>2000 \( \text{cm}^2/\text{Vs} \)) can also be achieved by a more well defined AlGaN/GaN interface. The sharper interface leads to less dispersion and lower \( C_{gs} \) at large drain bias compared to a diffuse AlGaN/GaN in-
interface. Furthermore, the sharp AlGaN/GaN interface enables a low access resistance while simultaneously allowing for easier formation of ohmic contacts, which can be hindered by the large band gap of AlN. Possibly, the high mobility achieved with an AlN-exclusion layer is not only related to the large band gap of AlN but also due to a good interface quality, inherently achieved by the large growth difference between GaN and AlN growth.

The trapping behavior of C-doped buffers for microwave applications have been thoroughly investigated in this thesis. The lower C-concentrations required for microwave applications compared to power applications is showed to result in n-type GaN. Consequently, the trapping behavior of such buffers is not limited by the formation of a pn-diode between the GaN buffer and the 2DEG. Instead, it is suggested that trapping at dislocations covered with C-clusters is the main source of dispersion. The trapping effects severely limited the output power to 2.5 W/mm at 30 GHz. Future work should target C-doped buffers with reduced dislocation densities. This could verify the ideas presented in this thesis and possibly reduce the dispersive effects in C-doped buffers. Freestanding GaN substrates could be used to decrease the dislocation density by at least two orders of magnitude [151]. The C-incorporation would have to be controlled using an external C-source, as not to degrade the crystal quality.

AlGaN Back back barriers with a large C-concentration is shown to suffer from extensive trapping effects. However, a epi-structure with a 100 nm uid GaN channel showed performance in line with C-doped GaN buffers. Similarly to the C-doped buffers, the trapping in the back barrier devices also seemed to be enabled by extended defects. Therefore, improved crystal quality is of large interest also in this case. Furthermore, the C-concentration should be minimized in the back barrier to assess its contribution to the total trapping behavior. In the literature, the best results seems to be enabled when the back barrier is grown on a GaN buffer layer. Future works should adopt this method and investigate how this affects trapping.

The thin HEMT structure showed excellent DC characteristics and RF output power (3.9 W/mm at 30 GHz). However, the performance is limited by trapping at dislocations, most probably originating from the AlN-nucleation layer. Therefore, future work should focus on further optimizing the nucleation layer. Furthermore, an extensive thermal evaluation should be undertaken, to verify that the thin GaN buffer
does not degrade the thermal performance of the epi-structure.

Looking in to the future of epi-design for GaN HEMTs, N-polar structures offer interesting opportunities for high frequency operation. The N-polar case intrinsically offers a good electron confinement due to the high energy barrier below the 2DEG and the polarization fields "pushing" the electrons upwards [152]. Furthermore, both surface and buffer trapping effects can be mitigated in interesting ways [153]. For a highly optimized N-polar material an extremely impressive output power density of 6.5 W/mm at 94 GHz has been reported [152].
Chapter 6

Summary of appended papers

This chapter summarizes the publications which are included in this thesis. An abstract and my contributions are presented for each publication.

Paper A


The paper investigates the formation of recessed, Ta/Al/Ta, ohmic contacts to an InAlN/AlN/GaN heterostructures. A contact resistance ($R_C$) as low as 0.14 $\Omega \text{mm}$ is found for contacts where the recess etch has stopped just above the 2D electron gas channel. At this depth the contacts are also found to be less sensitive to other process parameters, such as anneal duration and temperature. For deeper recesses $R_C$ remains low but requires annealing at higher temperatures for contact formation. An optimum bottom Ta layer thickness of 5–10 nm is found. Two reliability experiments preliminary confirm the stability of the recessed contacts.

**My contribution:** I designed the experiments, fabricated the test-structures, performed the measurements, and wrote the paper with feedback from the co-authors.
Paper B


High-electron mobility transistors (HEMTs) with different sharpness of the AlGaN/GaN interface are investigated. Two structures, one with an optimized AlGaN/GaN interface and another with an unoptimized, are grown using hot-wall metal-organic chemical vapor deposition. The electron mobility of the optimized structure is 1760 cm$^2$/Vs compared with 1660 cm$^2$/Vs for the unoptimized structure. The higher mobility manifests as lower parasitic resistance yielding a better dc and high-frequency performance. A small-signal equivalent model is extracted, which indicate a lower electron penetration into the buffer in the optimized sample. Pulsed-IV measurements imply that the sharper interface provides less dispersive effects at large drain biases.

My contribution: I fabricated the HEMTs, performed the measurements as well as the physical and compact modelling, and wrote the paper with feedback from the co-authors.

Paper C


HEMTs have been fabricated on three epitaxial structures: two with uniform C doping profile but different concentration and one with a stepped doping profile. The leakage currents in OFF-state at 10 V drain voltage were in the same order of magnitude ($10^{-4}$ A/mm) for the high-doped and stepped-doped buffer. The highly doped material had a current collapse (CC) of 79 % compared with 16 % for the stepped-doped material under dynamic I–V conditions. The low-doped material had low CC (5 %) but poor buffer isolation. Trap characterization revealed that the high-doped material had two trap levels at 0.15 and 0.59 eV, while the lowly doped material had only one trap level at
0.59 eV. This paper indicates that carbon is a potential substitute to iron as a deep level acceptor.

**My contribution:** JB and NR fabricated the HEMTs, SG and JB performed the measurements and wrote the paper with feedback from the co-authors.

### Paper D


AlGaN/GaN epi-structures are grown by metalorganic chemical vapor deposition using propane as precursor to achieve a C-doped GaN buffer. This approach allows for optimization of the GaN growth conditions without compromising material quality to achieve semi-insulating properties. HEMTs are fabricated and evaluated in terms of isolation and dispersion. Good isolation with OFF-state currents of $2 \cdot 10^{-6}$ A/mm, breakdown fields of 70 V/µm, and low drain induced barrier lowering of 0.13 mV/V are found. However, severe dispersive effects are identified using pulsed-IV measurements. Current collapse and knee walkout effects limit the maximum output power to 1.3 W/mm.

**My contribution:** I fabricated the HEMTs, performed the measurements, and wrote the paper with feedback from the co-authors.

### Paper E


AlGaN/GaN high electron mobility transistors (HEMTs) fabricated on epi-structures with C-doped buffers are investigated. Changes in growth parameters are used to control the C-concentration in metalorganic chemical vapor deposition. The C-concentration is low enough to result in n-type GaN. Reference devices are also fabricated on a structure us-
ing Fe as dopant, to exclude any process related variations and provide a relevant benchmark. Pulsed-IV measurements show extensive dispersion in the C-doped devices, with values of dynamic $R_{ON}$ 3-4 times larger than in the DC-case. In drain current transient measurements the trap filling time is varied, finding large prevalence of trapping at dislocations for the C-doped samples. The measurements indicate that clusters of C around the dislocations are the main cause for the increased dispersion.

**My contribution:** I designed the experiments, fabricated the HEMTs, performed the measurements, analyzed the results, and wrote the paper with feedback from the co-authors.
I would like to extend my thanks to the people who made this work possible.

I would like to thank Prof. Herbert Zirath for giving me the opportunity to work and conduct this research at the Microwave Electronics Laboratory.

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Paper A

Low resistive Au-free, Ta-based, recessed ohmic contacts to InAlN/AlN/GaN heterostructures


Low resistive Au-free, Ta-based, recessed ohmic contacts to InAlN/AlN/GaN heterostructures

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Abstract
The formation of recess etched Au-free ohmic contacts to an InAlN/AlN/GaN heterostructure is investigated. A Ta/Al/Ta metal stack is used to produce contacts with contact resistance ($R_c$) as low as 0.14 $\Omega$ mm. It is found that $R_c$ decreases with increasing recess depth until the InAlN barrier is completely removed. For even deeper recesses $R_c$ remains low but requires annealing at higher temperatures for contact formation. The lowest $R_c$ is found for contacts where the recess etch has stopped just above the 2D electron gas channel. At this depth the contacts are also found to be less sensitive to other process parameters, such as anneal duration and temperature. An optimum bottom Ta layer thickness of 5–10 nm is found. Two reliability experiments preliminary confirm the stability of the recessed contacts.

Keywords: Au-free, ohmic contact, recess etch, InAlN, high electron mobility transistor, GaN

1. Introduction
InAlN/AlN/GaN high electron mobility transistor (HEMT) technology has been studied extensively due to potentially improved power performance at higher frequencies compared to AlGaN/GaN HEMTs. This is due to a larger polarization field in InAlN [1], providing higher 2D electron gas (2DEG) densities with downscaled barriers. Furthermore, InAlN with a 17% Indium content is lattice-matched to GaN, giving strain free heterostructures and potentially improved device reliability [2]. InAlN/AlN/GaN HEMTs have demonstrated excellent high frequency performance; $f_T$ and $f_{max}$ above 300 GHz have been reported [3–6]. Furthermore, an output power of 5.8 W mm$^{-1}$ at 40 GHz with a power added efficiency of 16% have been demonstrated [7].

Ohmic contacts with low contact resistance ($R_c$) are vital for high frequency performance of extremely scaled GaN HEMTs [8], noise performance, high efficiency and reliability. Previous studies on InAlN/AlN/GaN employ ohmic contacts formed using different techniques. The standard Ti/Al/Ni/Au metallization has yielded low resistive contacts with values of $R_c$ of 0.15 and 0.39 $\Omega$ mm [9, 10]. Recessed Mo/Al/Mo/Au contacts have produced $R_c$ of 0.15 $\Omega$ mm [11], Au-free Ta/Si-based contacts have reached 0.33 $\Omega$ mm [12] and re-grown, highly n-doped GaN contacts have achieved $R_c$ of 0.10 and 0.16 $\Omega$ mm [4, 13]. Ti/Al based contacts often exhibit a low contact resistance but require a high anneal temperature. This leads to a rough surface morphology and potentially increased semiconductor sheet resistance ($R_{sh}$) [14, 15]. Various attempts have been made to circumvent these issues. Recess etching prior to metallization has shown to decrease the required anneal temperature [10]. The use of a Ta diffusion barrier was found to mitigate intermetallic reactions which improved contact morphology [16]. An alternative metallization that has shown to require a much lower anneal temperature is Ta/Al/Ta. This metallization has...
yielded very low $R_c$ when optimized for AlGaN/GaN heterostructures [17]. Good results for Ta/Al/Ta metallization have also been achieved on InAlN/GaN heterostructures [18].

Although low-resistive ohmic contacts to GaN HEMT heterostructures are frequently reported, a general, reliable fabrication process is not yet available. Especially variations in the AlN-exclusion layer, which is required in InAlN/GaN heterostructures, are likely to make contact formation more difficult [19]. This may be circumvented by recess etching prior to metallization. Recess etching has previously shown to decrease $R_c$, and enable ohmic contact formation to GaN heterostructures [10, 11, 19–22]. However, the optimum recess depth and other process parameters are not established. In this study, we investigated the impact of recess etch depth on the contact formation for Ta/Al/Ta contacts to InAlN/GaN/GaN HEMT structures. Furthermore, the impacts of the bottom Ta-thickness, the anneal duration and temperature were investigated. In section I, the experimental methods for InAlN/GaN epitaxial growth, ohmic contact process, and characterization are presented. Results from measurements and characterization including HR-TEM analysis and reliability measurements are shown in section 3. Conclusions are presented in section 4.

2. Experimental

2.1. Epitaxial growth

Using low pressure metal-organic vapor phase epitaxy the InAlN/GaN heterostructure was grown on a 3 inch SiC substrate using a close coupled multizwafer reactor. Trimethyl gallium (TMGa), trimethyl indium (TMIn), and trimethyl aluminum (TMAI) were used as group III precursors and ammonia (NH$_3$) as group V precursor. First, a 100 nm high temperature AlN nucleation layer was grown, followed by a high resistive 1.9 μm GaN buffer layer. A 2 nm thick AlN interlayer and 6 nm undoped InAlN (18% In) was then grown on the GaN buffer. The In concentration is selected in order to achieve lattice matching to GaN. The total barrier thickness (AlN + nAlN) was found to be 7.8 nm through XRD measurements. The thickness uniformity of the epi-structure was 1.9%. Details on the growth of InAlN/GaN/GaN HEMT structures may be found in [23].

Contactless resistance measurements on the as-grown heterostructure indicated a sheet resistance of 232 $\Omega$/square with a wafer uniformity of 2.6%. The mobility and sheet charge density was $1500 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and $1.8 \times 10^{13} \text{ cm}^{-2}$ respectively.

2.2. Test structure fabrication

Transfer length method (TLM) structures were fabricated on several samples ($15 \times 15 \text{ mm}^2$) cut from the same wafer. First, mesas were defined with optical lithography and dry etching. Ohmic contacts were defined with optical lithography followed by recess etching in a Cl$_2$/Ar plasma for different durations. One major challenge for recessed ohmic contacts (or gates) is the uniformity and repeatability of the etch process. In this work we have developed a Cl$_2$/Ar based ICP/RIE process with low ICP and RIE power levels of 25 W for low etch rate. The Cl$_2$ and Ar ratio was 4:1 (40 sccm and 10 sccm, respectively) and the process pressure was 3 mTorr. Six etch durations were investigated; 0, 30, 50, 70, 90 and 120 s. The recess etch depth was measured using atomic force microscope on parts of the chips that were masked during metal deposition. The etch rate was found to be $0.16 \pm 0.03 \text{ nm s}^{-1}$ after an initial ‘dead time’, presumably due to the presence of a native oxide (figure 1) [24]. The uncertainty has been extracted from the data in figure 1 and from unpublished data.

After recess etching an O$_2$-plasma was applied for 1 min to remove possible residues from the recess etch. Before evaporation of the metal stack oxide strips were performed. The samples were dipped for 30 s each in H$_2$O:HCl (10:1) and H$_2$O:HF (10:1) respectively. An ohmic metallization stack consisting of Ta(t$_{Ta1}$)/Al(t$_{Al}$ = 280 nm)/Ta (t$_{Ta2}$ = 20 nm) was evaporated using the same resist mask as for the recess etch, making the ohmic contact self-aligned to the recess. The thickness of the bottom Ta-layer, t$_{Ta1}$, was 2.5, 5, 10, or 20 nm. The top Ta-layer was used to prevent oxidation of the Al-layer. In total, processing yielded 24 combinations of recess depths and metallizations. A 70 nm thick Al$_2$O$_3$ passivation layer was deposited by plasma-assisted atomic layer deposition (ALD) [25]. Openings in the passivation layer were defined with photolithography followed by wet-etching in a DI:HF (10:1) solution.

3. Results

3.1. Anneal experiments

The samples were annealed in an N$_2$ ambient in a rapid thermal processor. TLM measurements were performed with
a four point measurement setup using a semiconductor parameter analyzer to extract $R_c$ and $R_{sh}$. A simple experiment dealing with just the recess depth is presented in figure 2. The contacts were annealed at 550 °C for 1 min and $t_{\text{r}}=5$ nm. The lowest $R_c$ (0.21 Ω mm) was found at a recess depth just above the channel. To find the optimum anneal conditions for each contact configuration two annealing experiments were performed. Firstly, samples were annealed repeatedly for 1 min at increasing temperatures, from 500 °C to 675 °C in steps of 25 °C. Secondly, the dependence of $R_c$ on anneal duration while the temperature was kept constant at 550 and 600 °C, respectively. Figure 3 shows the anneal temperature dependence of $R_c$ for three recess-etch depths while $t_{\text{r}}=5$ and the anneal duration were fixed. The 7 nm etch-depth produced the lowest $R_c$ (0.21 Ω mm) and was relatively insensitive to anneal temperature. Without recess etching $R_c$ never drops below 1 Ω mm. Each of the three contacts have a minimum in the graph but at different anneal temperatures. Comparing the non-recessed to the 7 nm etch depth clearly displays the lower anneal temperatures required for recessed contacts. The deeply etched contacts required higher annealing temperature to produce low resistive contacts. For recessing beyond the barrier layer, the electric contact is made on the sidewall of the recess. This may increase the importance of damages or re-deposition as compared to contacts made on the bottom of the recess. Possibly this explains the higher temperatures required to reach low $R_c$. Figure 4 shows the $R_c$ dependence on annealing duration for the same contact configurations as in figure 3 at 550 °C and 600 °C. The contact with 7 nm etch-depth produced low values of $R_c$ for all anneal conditions. After 8 min of annealing at 550 °C $R_c$ saturated at 0.14 Ω mm. Annealing at 600 °C for more than 2 min slightly degraded the contact performance. The non-recessed contact saturated at around 1 Ω mm with a lowest value of 0.94 Ω mm after 2 min of annealing at 600 °C. The deeply etched contacts were found to improve a lot from longer annealing at 550 °C. Its lowest value (0.30 Ω mm) was found after 4 min of annealing at 600 °C. The longer anneal durations required for the deeply etched contact is believed to have the same effect as the increased temperature. Extended annealing at 600 °C increased $R_c$ for all contact configurations. The slow saturation of $R_c$ seen at 550 °C is in stark contrast to the formation of Ti-contacts. These are annealed during a very short period (usually 30–60 s) at a high temperature. The lower temperature annealing for Ta-based contacts aid in maintaining good crystallographic quality, good contact morphology and minimizing thermal stress. After annealing at 650 °C $R_{sh}$ increased 15% on average as compared to annealing at 500 °C. During the time dependent annealing at 550 °C $R_{sh}$ was not affected by anneal duration, at 600 °C $R_{sh}$ increased around 5% comparing samples annealed for 1 min with samples annealed for 16 min.

3.2. Impact of recess depth

Table 1 shows the lowest $R_c$ obtained for each contact configuration together with the corresponding anneal condition. The best contacts were found when the recess had stopped just above the 2DEG, at 7 nm recess depth. However, deeper etching also showed to produce low resistive contacts. Similar results have been obtained in other studies [11, 19, 21, 22]. The contacts which were recessed below the 2DEG channel (10 and 15 nm) required long annealing at 600 °C. Furthermore, these two depths showed very similar values of $R_c$. This was expected since they both rely on the formation of a sidewall contact to the 2DEG. As previously discussed, we believe that this deep recessing introduced damages or re-deposited material around the contacting area. The impact of the sidewall slope was not investigated in this work. A
shallower slope could potentially be more favorable for ohmic contact formation [21].

Table 1 also shows that shallow recess etching may increase $R_c$ in some cases. For $t_{Ta1} = 10$ and 20 nm, $R_c$ increased for an etch-depth of 2.5 nm as compared to the non-recessed case.

3.3. Impact of metallization

The influence of $t_{Ta1}$ on $R_c$ can be seen in figure 5 for three recess depths. Again, only the lowest $R_c$ for each contact configuration is considered (same as table 1). The thickness of the Al- and top Ta-layer were kept constant (280/20 nm). The non-recessed contact showed a clear minimum at $t_{Ta1} = 10$ nm. Looking at the two recessed contacts the behavior was somewhat different. The sample with 7 nm recess depth still had a minimum but increasing the $t_{Ta1}$ thickness caused a small increase in $R_c$. For the deeply etched contact no minimum was found, instead a minimum thickness of $t_{Ta1}$ (5 nm) above which $R_c$ was constant was discovered. A similar dependence could be found for contacts with 10 nm recess depth, table 1. Possibly this behavior was related to the formation of a sidewall contact. It indicates a large process window for deeply etched recessed ohmic contacts. Both the deeply etched contacts showed a sharp increase in $R_c$ for $t_{Ta1} = 2.5$ nm.

![Figure 4. $R_c$ plotted versus anneal duration at (a) 550 °C and (b) 600 °C for three different etch-depths with $t_{Ta1} = 5$ nm.](image)

![Figure 5. $R_c$ plotted versus $t_{Ta1}$ for three different etch-depths at each contacts configurations optimal anneal settings.](image)

### Table 1

<table>
<thead>
<tr>
<th>Etch depth (nm)</th>
<th>Bottom Ta-layer thickness, $t_{Ta1}$ (nm)</th>
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<th>5</th>
<th>10</th>
<th>20</th>
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<td>3.8</td>
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<td>0.62, 550, 1</td>
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<tr>
<td>7.0</td>
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<tr>
<td>10</td>
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<td>15</td>
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<td>0.30, 600, 4</td>
<td>0.27, 600, 16</td>
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</table>
The required anneal temperature and duration increased with increasing $t_{\text{Tal}}$. This indicated that Al indeed plays a role in the contact formation.

### 3.4. HR-TEM analysis

HR-TEM and energy-dispersive x-ray spectroscopy (EDX) were performed to study the contact-semiconductor interface properties. For conventional Ti-contacts the formation of TiN through extraction of nitrogen from the semiconductor, creating N-vacancies in the barrier, acting as n-doping, is proposed as an important part of ohmic contact formation [26–29]. The fact that TaN has a lower enthalpy of formation compared to TiN (−251 and −338 kJ mol$^{-1}$ respectively) gives an indication that the same process might apply also for Ta-based contacts. Figure 6 shows the HR-TEM image and EDX line scan of the 7 nm etched contact with $t_{\text{Tal}} = 5$ nm annealed for 8 min at 550°C. From the EDX-analysis there was no clear indication of TaN formation, although a very thin layer ($<3$ nm) cannot be ruled out. In the metal stack an apparent mixing of Ta and Al was observed.

For Ti/Al-contacts several other models for ohmic contact formation exists. Many of them can be translated to the Ta/Al case. For example, the increase of electrons in the channel under the contact may be due to tensile strain induced by annealing of the metal stack [30]. It is believed that Al has a key role in inducing a strain, whereas Ti prevents relaxation. Another mechanism is the reduction of the barrier height due to formation to Al–Ti bonds to the Al-rich phase of the barrier layer [31]. All these models could explain the low $R_c$ ohmic contacts obtained through the Ta/Al-based contact but neither of them could be confirmed or disproved through our experiments.

Figure 6. (a) Cross-sectional HR-TEM image, (b) EDX line scan. The investigated contact had a 7 nm etch-depth, $t_{\text{Tal}} = 5$ nm and were annealed for 8 min at 550°C.

### 3.5. Reliability measurements

Contact reliability was measured through a storage test and a dc-stress test. The storage test was performed at 300°C in air ambient. $R_c$ and $R_{sh}$ were measured approximately once a day over a period of two weeks. Figure 7 shows the evolution of $R_c$ and $R_{sh}$ for two recess etched samples. The measurements were only performed on one set of samples. The starting values (0.27 and 0.20 $\Omega$ mm) are within the normal spread of ohmic contact processes ($\pm0.1 \Omega$ mm) as compared to the values in table 1.

The deeply etched sample showed a very stable $R_c$ over the whole interval. The sample with an etch depth of 7 nm, on
the other hand, showed an increasing $R_c$. $R_{dd}$ decreased with time for both samples in a similar fashion.

In the dc-stress test a constant current was forced through two contacts while monitoring the voltage drop. The same two contact configurations were used as in the storage test. Two current levels were used, corresponding to 20% and 50% of the current at the knee voltage. The measurement was performed under dark conditions during 24 h. Both samples showed the same behavior; at 20% the contact resistance decreased slightly over time and at 50% a slight increase was found. In both cases the deeply etched sample showed a larger variation. It is reasonable to assume that a sidewall contact leads to a smaller contact area. The larger variations in the deeply etched sample might be explained by a larger current density.

4. Conclusion

We have investigated the ohmic contact formation of Au-free, recessed ohmic contacts to an InAlN/AIn/GaN HEMT structure. A Ta/Al/Ta metal stack was used to produce contacts with $R_c$ as low as 0.14 $\Omega \cdot \text{mm}$. Our results showed that recessed contacts offer a large process window. Even though the lowest $R_c$ was found for an etch-depth in the vicinity of the 2DEG, $R_{dd}$ remained low for a wide range of deeper recesses as well. For non-recessed contact we found an optimum thickness of the bottom Ta-layer. However, for the recessed contacts we found a minimum thickness (5 nm) above which $R_c$ was constant. This behavior was especially prominent for the deeply etched contacts. Although $R_c$ for many configurations were in the same order of magnitude the annealing conditions differed. It was found that in general deeply etched contacts or thick bottom Ta-layers required longer annealing or higher temperatures to reach low $R_c$. In summary, this indicates that in order to maximize the chances of a low $R_c$, with different epi-structures, the recess should be etched beyond the 2DEG and a thick bottom Ta-layer should be deposited.

In conclusion, we have demonstrated Au-free, recessed ohmic contacts to InAlN/AIn/GaN with very low $R_c$ achieved at low anneal temperatures. Furthermore, the results show promise of a repeatable process.

Acknowledgments

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Performance Enhancement of Microwave GaN HEMTs Without an AlN-exclusion Layer Using an Optimized Al-GaN/GaN Interface Growth Process


Performance Enhancement of Microwave GaN HEMTs Without an AlN-Exclusion Layer Using an Optimized AlGaN/GaN Interface Growth Process

Johan Bergsten, Jr-Tai Chen, Sebastian Gustafsson, Student Member, IEEE, Anna Malmros, Urban Forsberg, Mattias Thorsell, Member, IEEE, Erik Janzén, and Niklas Rorsman, Member, IEEE

Abstract—The impact of the sharpness of the AlGaN/GaN interface in high-electron mobility transistors (HEMTs) is investigated. Two structures, one with an optimized AlGaN/GaN interface and another with an unoptimized, were grown using hot-wall metal-organic chemical vapor deposition. The structure with optimized sharpness of the interface shows electron mobility of 1760 cm²/V·s as compared with 1660 cm²/V·s for the nonoptimized interface. Gated Hall measurements indicate that the sharper interface maintains higher mobility when the electrons are close to the interface compared with the nonoptimized structure, indicating less scattering due to alloy disorder and interface roughness. HEMTs were processed and evaluated. The higher mobility manifests as lower parasitic resistance yielding a better dc and high-frequency performance. A small-signal equivalent model is extracted. The results indicate a lower electron penetration into the buffer in the optimized sample. Pulsed-IV measurements imply that the sharper interface provides less dispersive effects at large drain biases. We speculate that the mobility enhancement seen AlGaN/GaN structures compared with the AlGaN/GaN case is not only related to the larger conduction band offset but also due to a more well-defined interface minimizing scattering due to alloy disorder and interface roughness.

Index Terms—AlGaN/GaN interface, GaN high-electron mobility transistor (HEMT), interface sharpness.

I. INTRODUCTION

AlGaN/GaN high-electron mobility transistors (HEMTs) are recognized as good candidates for high-power, high-frequency power amplifiers. Due to their high breakdown voltage, high cutoff frequency, and good thermal capabilities, devices have shown excellent performance, including $f_{\text{max}}$ of 300 GHz [1] and 40-W/mm power density [2]. High-performance HEMT devices rely on high-quality heterostructures with large carrier concentration, high-electron mobility, and good electron confinement in the channel.

III-nitride heterostructures are usually grown with metal-organic chemical vapor deposition (MOCVD). The growth of different types of III-nitride compounds has extensively been investigated, and is now used commercially to grow epitaxial layers for HEMTs and light-emitting diodes. For standard AlGaN/GaN structures, the mobility of 1300–1500 cm²/V·s is usually obtained, and the carrier concentration depends on the AlGaN thickness and composition. Electron mobility may be enhanced by incorporating an AlN-exclusion layer between the channel and the AlGaN barrier layer. This layer reduces the penetration of the electrons into the AlGaN layer and may increase mobility to above 2000 cm²/V·s [3]–[5]. However, the exact thickness of the AlN-exclusion layer is difficult to control and may complicate the formation of ohmic contacts [6]–[9]. During the transition from GaN to AlN or AlGaN, residual Ga in the reactor may still be incorporated in the growth. This renders a diffused interface where Al content gradually increases within the first few nanometer AlN or AlGaN. This increases the alloy and interface roughness scattering, which adversely affect the electron mobility. By optimizing the growth process in the interfacial region, a heterostructure with a sharp AlGaN/GaN interface has been achieved yielding the mobility of the same order as with an AlN-exclusion layer [10].

In this paper, an AlGaN/GaN HEMT heterostructure with a sharp interface is compared with an unoptimized structure. The difference in sharpness at the AlGaN/GaN interface was physically investigated using a scanning transmission electron microscope (STEM) and electrically through mobility and carrier concentration measurements. Temperature-dependent Hall and gated Hall measurements were performed to investigate the dominant electron scattering processes. HEMTs were fabricated to study the influence of the interface on device characteristics. The HEMTs were characterized via dc, pulsed IV, and S-parameters. Frequency figure of merits...
Fig. 1. Schematic epitaxial HEMT structure with step-like carbon profile in the GaN layer for the two different AlGaN/GaN interfaces. Image is not to scale.

and equivalent circuit parameters were extracted from the S-parameters. The pulsed-IV measurements were used to compare lagging effects.

II. EXPERIMENT

A. AlGaN/GaN Epitaxy

The epitaxial HEMT structures were grown on 3-in semi-insulating SiC substrates by hot-wall MOCVD [11]. The growth was initiated with a high-temperature-grown AlN nucleation layer, followed by a 1.8-μm-thick carbon-doped GaN buffer layer and a 15-nm-thick Al0.3Ga0.7N barrier layer. On top of this, a 3-nm GaN cap was grown. A step-like carbon profile, which was controlled by the growth conditions [12], was used for the GaN buffer layers to achieve a low dispersion and high isolation [13] (Fig. 1). The top GaN channel-layer was unintentionally C-doped GaN buffer (1 · 1016 cm−3) acting as the channel. The interface conditions of the two AlGaN/GaN HEMT epiwafers, denoted as sharp and standard, differed in their sharpness of the Al transition at the AlGaN/GaN interface. The interface sharpening was achieved via a growth interruption together with a low flow rate of trimethylaluminum prior to the AlGaN growth. The details of the interface engineering are presented elsewhere [10].

B. HEMT Fabrication

A 55-nm silicon nitride passivation layer was deposited with low-pressure chemical vapor deposition at 820 °C on the two heterostructures. Mesas were defined using optical lithography and dry etching using a Cl2-based plasma process. Ohmic contacts were defined with photolithography, followed by recess etching for 100 s (corresponding to an etch depth of ~16 nm). A Ta/Al/Ta (10/280/20 nm) metal stack was evaporated and annealed in N2 ambient at 550 °C–600 °C for 5–16 min [14]. The contact resistance, as measured with transmission line method, was 0.27 and 0.21 Ωmm for the sharp and standard samples, respectively. Block gates with gate lengths of 0.2 μm were defined in a two-step electron beam lithography process. The first step defined the gate footprint, which was etched in the SiNx passivation, and the second defined the gate metallization. This method effectively defines a mushroom-shaped cross section with a gate-integrated field plate. The gate metal stack consisted of Ni/Pt/Au (30/20/400 nm). Finally, electrodes were defined with photolithography and Ti/Au/Ti metallization. The source–drain distance was 2.5 μm, and the gate–drain distance was 1.7 μm. Fig. 2 shows a finished 2 × 25-μm HEMT. In Fig. 2 (inset), the block gate is depicted, and the SiNx gate recess can be seen in the center of the gate metal.

III. RESULTS

A. Characterization of Material Structure and Electronic Properties

Cross-sectional STEM images were acquired of the standard and sharp AlGaN/GaN interfaces (Fig. 3). The standard sample showed an obscure interface, suggesting a diffuse transition from GaN to AlGaN. The sharp sample, on the other hand, showed a sharper interface and a more well-defined growth transition.

The sheet resistance ($R_{sh}$) of the as-grown epiwafers was measured by a contactless eddy-current technique, and the two-dimensional electron gas (2DEG) carrier concentration ($n_s$) and mobility ($\mu$) were determined by a contactless Lehighton measurement. The electrical properties of the as-grown epiwafers are listed in Table I. The sharp sample showed higher values of $\mu$ and $n_s$ as compared with the standard sample. However, $\mu$ for the sharp sample was lower than expected. This is most likely due to the growth process being optimized for 2 × 2 cm2 pieces of SiC substrates rather than 3-in wafers. On small pieces values over 2200 cm2/V · s have been achieved using the optimized growth conditions for the AlGaN/GaN interface [10], which is in the same range as structures with AlN-exclusion layers [11], [15]. The wafer uniformity of $R_{sh}$ was 3% for the sharp wafer and 4.3% for the standard wafer.
After HEMT processing, $R_{sh}$, $\mu$, and $n_s$ of the heterostructures were measured using Hall measurements on van der Pauw structures (Table I). $n_s$ and $\mu$ increased for both samples after processing, leading to a decrease in $R_{sh}$.

### B. Gated and Temperature-Dependent Hall Measurements

Gated and temperature-dependent Hall measurements were performed to investigate the scattering processes in the 2DEG channels (Fig. 4). Scattering mechanisms in the AlGaN/GaN 2DEG channel have been studied extensively [16]–[21]. At room temperature, mobility is limited by scattering at optical phonons. At lower temperature, phonon scattering decreases and temperature-independent processes scattering mechanisms, such as scattering at dislocations, ionized impurities, and interface roughness, become more important. Their relative importance is determined by the heterostructure properties which depend on the growth. The electron mobilities of the heterostructures showed similar temperature dependence which indicated that the difference in room-temperature mobility was caused by temperature-independent scattering mechanisms [21]. The sharp interface exhibited higher mobility for all temperatures demonstrating similar material quality except the intentional variation in AlGaN/GaN interface sharpness.

Hall measurements on gated van der Pauw structures were used to measure the dependence of $\mu$ on $n_s$ (Fig. 4(b)). According to [21], a decreasing $\mu$ with increasing $n_s$ indicates that alloy disorder is the prominent scattering mechanism, while a constant $\mu$, with no dependence of $n_s$, implies interface roughness. For a carrier concentration below $1 \cdot 10^{13}$ cm$^{-2}$, the samples showed similar behaviors, with the standard sample approximately 100 cm$^2$/V $\cdot$ s below the sharp. For higher $n_s$, the mobility of the sharp sample saturated around 1700 cm$^2$/V $\cdot$ s, while the standard sample rapidly decreased. At this large forward bias, the impact of the channel/barrier interface is expected to be the most prominent.
Consequently, we believe that the sharp sample suffers from less alloy disorder scattering, making the mobility limited by interface roughness scattering. This behavior was attributed to the optimized growth process.

C. DC

DC characteristics were measured with a parameter analyzer. Fig. 5 and Table II show the dc characteristics of HEMTs on the two epistuctures. Both samples showed very similar behavior. The maximum drain current ($I_{\text{MAX}}$) was measured by driving a constant current (1 μA) through the gate while sweeping the drain bias. Both samples showed a transconductance of around 400 mS/mm. The difference in ON-resistance mirrored the difference in sheet resistance created by the difference in AlGaN/GaN interface sharpness of the two structures.

D. S-Parameters

S-parameters were measured from 10 to 110 GHz. $f_T$ and $f_{\text{max}}$ were extracted from $h_{21}$ and maximum available gain, respectively (Table III). The sharp sample produced $f_T$ and $f_{\text{max}}$ around 6%–8% higher than the standard sample. A small-signal equivalent circuit model was extracted by a direct extraction method [22] to examine $C_{gs}$ as a function of $V_{GS}$ (Fig. 6). At low $V_{DS}$, the sharp and standard samples show similar behavior, with slightly lower values for the sharp sample. For higher $V_{DS}$, the standard sample showed a second increase in the slope of $C_{gs}$. This behavior has been associated with electron accumulation in the barrier [23]. Probably, the large drain bias enabled electron penetration into the barrier, even at a small negative gate bias, in the standard sample. The sharp sample showed no signs of any additional accumulation in the barrier as compared with the $V_{DS} = 1$ V case.

E. Pulsed IV

Pulsed-IV measurements were performed to investigate trapping and knee walkout effects using a dynamic IV analyzer. The pulsewidth was 1 μs with 1-ms period time. Fig. 7(a) shows measurements pulsed from two different quiescent points; the reference point ($V_{GSQ}, V_{D SQ}$) = (0, 0)
and \((V_p - 2, 15)\) V where the latter quiescent bias should mimic class B operation. Both samples suffered from a slight knee walkout. The current collapse was quantified via the current slump ratio. It is defined as the percentage drop of the current at \(V_{DS} = 20\) V and \(V_{GS} = 1\) V when pulsed from a certain quiescent bias \((V_{GSQ}, V_{DSQ})\) compared with the current resulting from the reference quiescent bias \((0, 0)\)

\[
Z(V_{GSQ}, V_{DSQ}) = \frac{I_{DS}|V_{GSQ}, V_{DSQ} - I_{DS}|0, 0}{I_{DS}|0, 0} \cdot 100. \tag{1}
\]

Fig. 7(b) shows the slump ratio versus the quiescent drain voltage at a constant quiescent gate voltage \((V_{GSQ} = V_p - 2\) V). The sharp and standard samples demonstrated similar results except at higher \(V_{DSQ}\) where the slump ration of the standard sample increases more rapidly. Possibly, the standard sample suffers from increased electron trapping in the drain access region where the large drain voltage can allow electron to access trap states at the AlGaN/GaN interface or inside the barrier.

**IV. CONCLUSION AND DISCUSSION**

The sharpness of transitions between different materials in heterostructures is an important aspect of epitaxial growth. In this paper, we show some of the advantages a sharp AlGaN/GaN interface gives to the 2DEG properties and HEMT characteristics compared with a diffuse interface. To visualize the difference between the samples, a simple Poisson–Schrödinger simulation has been performed (Fig. 8). The ideal interface switches from GaN to AlGaN instantaneous, while the diffuse interface changes Al-concentration gradually over a distance of 3 nm. The diffuse interface gives a wider distribution of the 2DEG and shifts it toward the surface, decreasing the mobility due to larger alloy disorder scattering. The common way to prevent this behavior in AlGaN/GaN heterostructures is to include an AlN-exclusion layer. The large bandgap of the AlN-exclusion layer is generally thought to decrease electron penetration into the barrier. With the large electron mobility achieved using a sharp interface [10], we speculate that the large conduction band offset created by the AlN-exclusion layer is not the only factor responsible for the enhanced mobility. The rapid change in growth conditions while changing from growing GaN to AlN and subsequently AlGaN gives a sharper transition compared with changing from GaN to AlGaN directly. The AlN-exclusion layer would effectively minimize scattering due to alloy disorder due to less electron penetration into the AlGaN barrier.

HEMT devices on an optimized AlGaN/GaN heterostructure with a sharp AlGaN/GaN interface, demonstrating mobility enhancement similar to structures with an AlN-exclusion layer, were fabricated. For comparison, devices on a heterostructure with an unoptimized interface were fabricated. The sharp interface gave higher electron mobility, probably due to lower levels of interface roughness scattering, and scattering due to alloy disorder, as indicated by gated Hall measurements. Compared with the two samples, it was clear that the sharp interface improved all aspects of the HEMT performance. The higher carrier concentration and mobility gave slightly higher current, larger gain, and higher \(f_t/f_{max}\). Interestingly, the sharp interface also gave a lower current slump at higher \(V_{DSQ}\). The improved electron confinement due to the more ideal transition from GaN to AlGaN in the sharp

Fig. 7. (a) Pulsed-\(IV\) measurements for two quiescent biases. (b) Slump ratio versus quiescent drain bias.

Fig. 8. Poisson–Schrödinger simulation of two GaN/AlGaN/GaN (3/15/1000 nm) heterostructures. The ideal sample has an instantaneous AlGaN/GaN interface, while in the diffuse interface, the Al content gradually changes over 3 nm.
sample was confirmed in gate voltage-dependent small-signal measurements.

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Dispersive Effects in Microwave AlGaN/AlN/GaN HEMTs With Carbon-Doped Buffer


Dispersive Effects in Microwave AlGaN/AlN/GaN HEMTs With Carbon-Doped Buffer

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Abstract—Aluminium gallium nitride (AlGaN/GaN) high-electron mobility transistor performance is to a large extent affected by the buffer design, which, in this paper, is varied using different levels of carbon incorporation. Three epitaxial structures have been fabricated: 1) two with uniform carbon doping profile but different carbon concentration and 2) one with a stepped doping profile. The epitaxial structures have been grown on 4H-SiC using hot-wall metal–organic chemical vapor deposition with residual carbon doping. The leakage currents in OFF-state at 10 V drain voltage were in the same order of magnitude ($10^{-4}$ A/mm) for the high-doped and stepped-doped buffer. The high-doped material had a current collapse (CC) of 78.8% compared with 16.1% for the stepped-doped material under dynamic $I–V$ conditions. The low-doped material had low CC (5.2%) but poor buffer isolation. Trap characterization revealed that the high-doped material had two trap levels at 0.15 and 0.59 eV, and the low-doped material had one trap level at 0.59 eV.

Index Terms—Current collapse (CC), dispersion, gallium nitride (GaN), high-electron mobility transistor (HEMT), trap levels.

I. INTRODUCTION

GALLIUM nitride (GaN)-based high-electron mobility transistors (HEMTs) offer exceptional high frequency and power performance due to its high-electron mobility and wide bandgap. In terms of traditional high-frequency figures of merit GaN devices have matured in the last decade, reaching $f_T/f_{max}$ of up to 450/600 GHz [1] and output power up to 40 W/mm [2].

High output power is enabled by a highly semi-insulating buffer, which improves breakdown characteristics, minimizes buffer leakage, and short-channel effects [3]. Buffer isolation can be achieved using intrinsic growth defects to form deep donors and acceptors [4]. This approach yields highly resistive (HR) buffers but at the expense of crystal quality. Alternatively, an intentional dopant, such as iron (Fe), carbon (C), or magnesium (Mg), enables HR buffers without compromising crystal quality [5], [6]. Both procedures introduce trap states which may reduce the ON-state conductance and maximum drain current under dynamical conditions, effectively limiting the RF output power and efficiency [7].

The most commonly used buffer dopant is Fe, which suffers from memory effects during growth, rendering arbitrary design of the doping profile impossible [6]. The carbon doping process lacks such memory effects, making it possible to have discontinuous C-doping profiles and sharp transitions to the GaN channel [8]. However, simulations on carbon-doped HEMTs indicate a problem where the buffer can become floating, possibly pinching the active channel [9]. Nevertheless, both iron and carbon doping suffer from severe current collapse (CC) if the compensation-doped buffer is placed close to the GaN channel [10]–[13]. Several reports show that the doped buffer should be placed at a sufficiently long distance from the GaN channel to reduce CC [10], [14]. The optimal buffer design is a tradeoff between several HEMT characteristics (e.g., breakdown voltage, short-channel effects, subthreshold leakage, CC, and maximum drain–source current) and may vary for different applications.

In this paper, we have fabricated three types of AlGaN/AlN/GaN:C HEMTs with different carbon doping concentration and profile. A comprehensive characterization, including dc, small signal RF, and large signal RF, has been carried out in order to evaluate the device performance, focusing on microwave power amplifiers. Trap characterization has been carried out using pulsed $I–V$, drain current transient (DCT), and conductance dispersion measurements. This paper will also form a foundation for physical device simulations to further understand carbon trapping phenomena, and to optimize the carbon doping profile in the buffer.

This paper is organized as follows. Material growth and the HEMT fabrication process is covered in Section II. The device characterization and measurements are presented in Section III. Finally, the conclusion is drawn in Section IV.

II. EXPERIMENT

A. Growth of AlGaN/AlN/GaN Heterostructures on SiC

The epitaxial structures were grown by a hot-wall metal–organic chemical vapor deposition system [15], [16].
The heterostructure consisted of a 100-nm high-temperature AlN nucleation layer, a thick GaN layer with different carbon doping profiles followed by a 2-nm AlN exclusion layer, and an undoped AlGaN layer grown on semi-insulating 4H-SiC. The carbon doping in the GaN layer was realized using residual carbon impurities, which is controlled by the growth temperature [17]. Four different carbon levels were utilized in this paper, i.e., 1×10¹⁵ cm⁻³, 5×10¹⁷ cm⁻³, 1×10¹⁷ cm⁻³, and 1×10¹⁶ cm⁻³ that were prepared at the growth temperatures of 980 °C, 1000 °C, 1040 °C, and 1080 °C, respectively. Three epiwafers were grown to study the dispersion and memory effects, denoted as High-C, Low-C, and Stepped-C. The structural parameters and carbon profiles of the epiwafers are shown in Fig. 1. Two single-level carbon profiles were designed for the GaN layers in High-C and Low-C, respectively. The Stepped-C wafer contains a three-level carbon profile.

The crystalline quality of the three epiwafers was assessed by high-resolution X-ray diffraction rocking curve measurements. The values of full width of half maximum of the GaN (102) peaks for High-C, Low-C, and Stepped-C were 365, 282, and 436 arcsec, respectively.

The sheet resistance was measured using a noncontact eddy-current technique. The mobility and the sheet carrier density were determined using a noncontact low-power microwave reflectance technique supplied by Lehighton on the center position of each epiwafer (Table I) [18].

### B. HEMT Fabrication

The HEMT process used in this paper is a passivation-first process. Silicon nitride (SiNₓ) was deposited at 820 °C with low-pressure chemical vapor deposition. H₂SiCl₂ and NH₃ were used as precursor gases at a flow ratio of 6:1. These parameters resulted in a 60-nm thick Si-rich SiNₓ with a refractive index of 2.3. The mesas were then defined with a stepper and etched with a inductive coupled plasma/reactive ion etch (ICP/RIE) using NF₃-plasma (to etch the SiNₓ) and Cl/Ar-plasma (to etch the AlGaN/AlN/GaN heterostructure). Ohmic contacts were formed by self-aligned recessing, metal-stack evaporation, and liftoff. The structure was recessed to a depth just above the AlN exclusion layer [19] and a Ta/Al/Ta (20/280/100 nm) ohmic metal stack was electron beam evaporated [20]. The gates were defined in a two-step electron beam lithography process. In the first step, the footprint of the gate was defined and patterned with a low-bias ICP/RIE NF₃-plasma process. The resulting gate length was 0.2 μm. In the second stage, the gate metalization pattern was defined. The gate metalization, Ni/Pt/Au, was evaporated with a thickness of 20/10/400 nm. Finally, gate, source, and drain electrodes were defined and metalized with sputtering of Ti/Au with a thickness of 30/320 nm. All measurements were performed on HEMTs with a total gate width of 50 μm. The gate–source and gate–drain distances are 0.75 and 2 μm, respectively, for the High-C and Low-C HEMTs. The corresponding dimensions of the Stepped-C HEMT are both 0.9 μm. Transfer length method (TLM) and van der Pauw structures were also defined simultaneously on all wafers.

### III. Results

This section describes and discusses the HEMT measurements. The Stepped-C device has a different layout and structure compared with the Low-C and High-C devices, which has been accounted for where necessary. Overall, the Stepped-C HEMT has lower parasitic resistance due to shorter source–drain distance.

#### A. Hall

After processing, Hall measurements were performed using a Hall effect measurement system (HL5500PC, Biorad). The measured quantities are in good agreement with the preprocessing measurements (Table I). The passivation-first process, with a high-quality SiNₓ combined with a low-temperature ohmic contact anneal, preserves the mobility and electron density. However, the High-C structure showed a large nonuniformity. This is likely associated with nonuniform carbon distribution over the epiwafer. As mentioned in Section II-A, the residual carbon from the growth chamber and the precursor itself (tri-methyl gallium) were utilized as the carbon source. The carbon incorporation rate was controlled by the growth conditions. Therefore, the uniformity of the carbon doping depends greatly on the temperature and deposition profiles in the growth zone. In this investigation, no focus has been in optimizing the carbon

![Fig. 1. Specification of the epitaxial design. (a) High-C. (b) Low-C. (c) Stepped-C. Figures are not to scale.](image-url)
uniformity over large area. Since carbon is known for its adverse impact on two-dimensional electron gas properties, it is reasonable to attribute the variance of $R_{sh}$ to the uniformity of the carbon distribution. The mobility of the Stepped-C wafer was not as high as expected, and the mechanism is not completely understood. However, it should be noted that its AlGaN structure contained a high Al content, 30%, that accordingly built up high strain on the GaN, which might give rise to an early partial relaxation of the AlGaN, leading to a degraded mobility.

### B. DC

TLM measurements were performed on three positions on each wafer (Table II). All materials show a similar contact resistance ($R_c$), demonstrating the feasibility of a repeatable recessed ohmic contact process. The $R_{sh}$ after device fabrication is in good agreement with the preprocess and Hall measurements (Table I).

The $I$–$V$ characteristics were measured with a parameter analyzer and are shown in Fig. 2(a) and (b). A significantly lower leakage current is seen for devices with a high and stepped carbon doping. The higher gate leakage for the low-doped device can be affiliated with the pinchoff voltage, which is more negative compared with the high-doped device. This will increase the slope of the energy band in the AlGaN/GaN interface. Therefore, electron tunneling is more prominent, effectively increasing the gate leakage. Drain-induced barrier lowering (DIBL) is comparably small for the Stepped-C and High-C devices, but severe for the Low-C device [Fig. 2(b) (inset)]. For Low-C HEMTs, the threshold voltage is continuously lowered as the drain voltage increases and drops dramatically beyond 30 V. This can be explained by high-energy electron injection into the buffer. Table III contains extracted values of the subthreshold slope (SS), ON-resistance ($R_{on}$), saturated drain current ($I_{DSS}$), transconductance ($g_m$), and DIBL. As expected the SS is higher for devices with better electron confinement (High-C and Stepped-C). The variation in ON-resistance between the devices is due to differences in $R_{sh}$, $R_c$, and the device layout. The lower saturation current and transconductance for the High-C device can be attributed to the lower carrier density and carrier mobility in the material. The Low-C and Stepped-C devices are comparable in terms of saturation current, while Stepped-C has slightly higher transconductance.

Breakdown was measured using a drain current injection technique [21] [Fig. 2(c)]. A sharp step is seen at the pinchoff voltage for the High-C and Stepped-C materials. The step follows by a slope, where channel breakdown occurs. Eventually, gate breakdown occurs in the last region where $V_{DG}$ saturates. The measurement of the Low-C material shows a different behavior with no sharp transitions. This is explained by the electron injection in the low-doped buffer, and the majority of the drain current in this device is leaking through the buffer.

### C. S-Parameters

S-parameters were measured from 10 MHz to 110 GHz. The measured $S_{11}$, $S_{22}$, $|U|$, and $|h_{21}|$ at the bias point with
maximum \( f_T \) are shown in Fig. 3. The devices have similar small signal behavior in terms of input and output impedance, while the device with Stepped-C has noticeably higher gain than devices with High-C and Low-C. Table IV summarizes the small signal characterization in terms of maximum \( f_T \), maximum \( f_{\text{max}} \), extrinsic \( g_m \), extrinsic \( g_{ds} \), and extrinsic \( C_{\text{out}} \). The small signal parameters were extracted at 285 MHz at the bias point for maximum \( f_T \) (\( V_{\text{GS}} = -2 \) V and \( V_{\text{DS}} = 4 \) V for High-C, \( V_{\text{GS}} = -3.5 \) V and \( V_{\text{DS}} = 7 \) V for Low-C, and \( V_{\text{GS}} = -2.5 \) V and \( V_{\text{DS}} = 4 \) V for Stepped-C). The Stepped-C device shows the best performance in terms of \( f_T \) and \( f_{\text{max}} \) mostly due to its different layout and structure.

D. Output Conductance Dispersion

An investigation of the output conductance dispersion was performed by measuring low-frequency Y-parameters at different ambient temperatures. This enables extraction of the activation energies of trap states [22]. The temperature was swept from 20 °C to 160 °C. Calibrated two-port Y-parameter measurements were made from 5 Hz to 3 GHz with the quiescent drain current set to 15% of \( I_{\text{DSS}} \). The quiescent drain voltage was adjusted so that the dissipated power was equal to 0.1 W, resulting in low self-heating.

The measurements are shown in Fig. 4. The High-C device is suffering from severe dispersion with two prominent peaks and the Low-C device is showing similar dispersion at low frequencies as the High-C device. The activation energies of traps \( E_2 \) and \( D_1 \) are extracted from an Arrhenius diagram (Fig. 5); \( E_2 = 0.59 \) eV and \( D_1 = 0.15 \) eV. Traps associated with the \( E_2 \) activation energy are interesting because this trap level is also found in devices with iron doping. It is speculated that this trap is related to defects in the GaN material, which is dependant on the buffer doping concentration. The physical origin of the trap is not determined, but can be due to either impurities or intrinsic defects, such as vacancies or antisites [23]. The \( D_1 \) trap is also related to defects and dislocations in the GaN material [24].

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**TABLE IV**

<table>
<thead>
<tr>
<th>Material</th>
<th>( f_T ) (GHz)</th>
<th>( f_{\text{max}} ) (GHz)</th>
<th>( g_m, \text{ext} ) (mS/mm)</th>
<th>( g_{ds, \text{ext}} ) (mS/mm)</th>
<th>( C_{\text{out}} ) (pF/mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>High-C</td>
<td>27</td>
<td>61</td>
<td>282</td>
<td>23.2</td>
<td>0.57</td>
</tr>
<tr>
<td>Low-C</td>
<td>32</td>
<td>92</td>
<td>298</td>
<td>23.5</td>
<td>0.67</td>
</tr>
<tr>
<td>Stepped-C</td>
<td>46</td>
<td>146</td>
<td>390</td>
<td>26.6</td>
<td>0.71</td>
</tr>
</tbody>
</table>
In [25], a trap with similar activation energy (0.18 eV) is found, and is suggested to be located at the surface. The Stepped-C device does not show any consistent shift in the dispersion peaks versus frequency and no activation energy could, therefore, be extracted.

**E. Drain Current Transient**

Trapping time constants were investigated using an oscilloscope-based DCT measurement setup. The gate was biased at a constant voltage, setting the quiescent drain current to 25% of $I_{DSS}$. The drain voltage was pulsed from $V_{DSQ}$ to $2 \cdot V_{DSQ}$. Measurements with this pulse type and bias point will probe channel trapping and deep buffer traps under ON-state device operating conditions. The drain voltage is normalized to consider the different layout of the Stepped-C device.

Application-like conditions were invoked by having a short and periodic trap filling pulse. The trap filling pulse was 10-μs long and the period time was set to 1 s to facilitate full recovery of the drain current. The drain current was monitored from $1 \mu s$ to $10 \mu s$. The measured DCT is shown in Fig. 6 (inset). The time constants were extracted using a polynomial fitting method [26], and are shown in Fig. 6. A trap with an emission time of $\sim 50 \mu s$ is observed for both the High-C and the Low-C materials. However, the high-doped material also has a trap with an emission time of $\sim 1 \mu s$, indicating the presence of another trap level. This is in line with the trap state characterization in Section III-D. Even though no trap levels were identified for the Stepped-C material in Section III-D, it has a large peak emission at $\sim 0.3 \mu s$. The amplitude of the current lag is higher than for the other materials and may be due to errors in normalization of the quiescent voltages, but does not affect the qualitative analysis.

**F. Pulsed I–V**

CC and knee walkout effects were characterized using a dynamic $I–V$ analyzer (Accent D225). The pulselength was set to $1 \mu s$ with a 1 ms period time. The gate voltage was pulsed from $−6$ to $1 \mu V$ in $0.5 \mu V$ steps and the drain voltage was pulsed from $0$ to $15 \mu V$ in $0.1 \mu V$ steps. This measurement was carried out to investigate surface trapping and deep buffer trapping under OFF-state quiescent conditions.

The magnitude of the CC is given by the slump ratio defined as

$$Z(V_{GSQ}, V_{DSQ}) = \frac{I_{DS}|_{V_{GSQ}, V_{DSQ}} - I_{DS}|_{0, 0}}{I_{DS}|_{0, 0}} \cdot 100 \quad (1)$$

where $I_{DS}|_{V_{GSQ}, V_{DSQ}}$ and $I_{DS}|_{0, 0}$ are the drain current measurements with a quiescent state of $(V_{GSQ}$ and $V_{DSQ})$ and $(0$ and $0)$, respectively. The drain currents used for calculating the slump ratio are taken from readings

---

**TABLE V**

<table>
<thead>
<tr>
<th>Material</th>
<th>$Z(−6, 0)$ (%)</th>
<th>$Z(−6, 15)$ (%)</th>
<th>$R_{on}(0, 0)$ (Ωmm)</th>
<th>$R_{on}(−6, 15)$ (Ωmm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>High-C</td>
<td>-7.6</td>
<td>-78.8</td>
<td>2.3</td>
<td>17.3</td>
</tr>
<tr>
<td>Low-C</td>
<td>-1.4</td>
<td>-5.2</td>
<td>2.0</td>
<td>2.2</td>
</tr>
<tr>
<td>Stepped-C</td>
<td>-11.2</td>
<td>-16.1</td>
<td>1.1</td>
<td>1.5</td>
</tr>
</tbody>
</table>

---

**Fig. 7.** Current slump (1) versus different quiescent states. (a) $V_{DSQ} = 0 \mu V$, $V_{GSQ}$ stepped. (b) $V_{GSQ} = −6 \mu V$, $V_{DSQ}$ stepped.
GUSTAFSSON et al.: DISPERSIVE EFFECTS IN MICROWAVE AlGaN/AlN/GaN HEMTs WITH CARBON-DOPED BUFFER

Fig. 8. Pulsed $I-V$ measurements showing the dynamic $I_{DS}-V_{DS}$ behavior for different quiescent states. (a) High-C. (b) Low-C. (c) Stepped-C.

at $V_{GS} = 1$ V and $V_{DS} = 10$ V. The current slump and dynamic $R_{ON}$ is given for two quiescent states in Table V. The slump ratio versus $V_{DSQ}$ and $V_{GSQ}$ is shown in Fig. 7. The dynamic $I_{DS}-V_{DS}$ characteristics for five different quiescent states are shown in Fig. 8.

The High-C device exhibits a major CC and drops to $\sim 75\%$ of the reference current, while the Low-C device has very slight CC throughout the $V_{DSQ}$ stepping. The Stepped-C HEMT shows similar $V_{DSQ}$ dependence as the Low-C device. However, the Stepped-C device has larger CC due to the drop in drain current when a nonzero quiescent gate voltage is applied. The current slump performance of the Stepped-C device is not entirely in line with the DCT measurements, which might be due to the normalization in the DCT measurements. The high-doped device shows large dynamics in $R_{ON}$ and severe knee walkout, with a near eightfold increase in $ON$-resistance. The significant increase in $ON$-resistance for the high-doped device confirms that the $D_1$-trap is located on the surface.

Fig. 9. Delivered output power and drain efficiency versus delivered input power.

G. Load-Pull

Large signal device characterization was carried out using an active load-pull setup [27] at a fundamental frequency of 3 GHz. The devices were biased in Class AB, with a quiescent current of $15\%$ of $I_{DSS}$ and $V_{DSQ} = 15$ V.

An input power sweep was carried out for each device with the load impedance optimized for maximum output power, and the corresponding output power and drain efficiency is shown in Fig. 9. The Low-C and Stepped-C devices show comparable performance and deliver similar output powers. The gain is slightly higher for the Stepped-C device, resulting in higher drain efficiency at lower input powers and earlier saturation. As expected from the previous measurements, the large signal RF performance of the High-C device is degraded due to the severe CC, effectively lowering the output power and drain efficiency. The maximum obtained output power is in good agreement with estimations from pulsed $I-V$ measurements and amount to $\sim 0.9$, $2.4$, and $2.3$ W/mm for High-C, Low-C, and Stepped-C, respectively.

IV. CONCLUSION

We have shown an extensive characterization of GaN HEMTs fabricated from three different materials with a high, low, and stepped carbon doping profile. Results show that low leakage current and low CC can be achieved by optimizing the doping profile, thus maintaining good large signal RF performance. In consistency with other reports, placing a highly doped buffer close to the GaN channel severely degrades large signal RF performance due to the severe CC. The Low-C and Stepped-C devices show similar performance in terms of dc and RF, where the former offers slightly less CC and the latter lower leakage current.

The use of carbon doped buffer in [9] is shown to form a floating p-n junction, causing severe dispersion. The characterizations carried out in this paper indicates that the dispersion of C-doped GaN HEMTs is not as severe, and in line and even better than the previous work on Fe-doped buffers. The dispersion in C-doped buffers might, therefore, be due to other defects in the crystal not considered, but discussed, in [9]. A recent meta study on iron-doped buffers has found a trap with an activation energy of $0.6$ eV, which is not directly related to the Fe-atoms in the buffer [13]. In this paper, we have found a trap with a similar activation energy ($E_2 = 0.59$ eV). We also observe another defect-related surface trap in the high-doped HEMT with an activation energy of
$D_1 = 0.15 \text{ eV}$. These traps may explain the different results in this paper and in [9]. Furthermore, as explained in [28], if vertical leakage paths exist between channel and buffer the device can still have low CC.

Trapping effects can be extremely dynamic and sensitive to the stimuli. Depending on application needs, certain measurements can be focused on and different device properties can be emphasized by optimizing the buffer. Carbon is indeed a viable dopant for low-dispersive, HR buffers, and there is room for further development and improvement of the doping profile.

REFERENCES


Urban Forsberg received the M.Sc. degree in applied physics and electrical engineering and the Ph.D. degree in material physics from Linköping University, Linköping, Sweden, in 1998 and 2001, respectively. He was with Norstel, Linköping, where he was involved in epitaxial growth of SiC from 2002 to 2004. He joined Linköping University, in 2004, where he has been involved in the development of the hot-wall technique for III–nitrides.

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AlGaN/GaN high electron mobility transistors with intentionally doped GaN buffer using propane as carbon precursor


AlGaN/GaN high electron mobility transistors with intentionally doped GaN buffer using propane as carbon precursor

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AlGaN/GaN high electron mobility transistors (HEMTs) fabricated on a heterostructure grown by metalorganic chemical vapor deposition using an alternative method of carbon (C) doping the buffer are characterized. C-doping is achieved by using propane as precursor, as compared to tuning the growth process parameters to control C-incorporation from the gallium precursor. This approach allows for optimization of the GaN growth conditions without compromising material quality to achieve semi-insulating properties. The HEMTs are evaluated in terms of isolation and dispersion. Good isolation with OFF-state currents of 2 × 10⁻⁶ A/mm, breakdown fields of 70 V/µm, and low drain induced barrier lowering of 0.13 mV/V are found. Dispersive effects are examined using pulsed current–voltage measurements. Current collapse and knee walkout effects limit the maximum output power to 1.3 W/mm. With further optimization of the C-doping profile and GaN material quality this method should offer a versatile approach to decrease dispersive effects in GaN HEMTs. © 2016 The Japan Society of Applied Physics

1. Introduction

GaN-based high electron mobility transistors (HEMTs) combine high frequency with high output power and are therefore regarded as good candidates for future RF power amplification applications. An important aspect for HEMT performance is the buffer isolation which affects e.g., leakage currents and breakdown characteristics.1–3) The buffer is also an important factor for trapping phenomenon, causing e.g., current collapse (CC) or knee-walkout, in the transistor.4–8) Much work has therefore been put into optimizing the buffer layer, both with respect to trapping effects and to isolation.

Buffer isolation is usually achieved by introducing acceptor-like impurities, like iron (Fe) or carbon (C) atoms, which compensate for the residual silicon and oxygen. This prevents conduction in the GaN buffer, resulting in reduced leakage currents and increased breakdown voltage.6,9) Growing iron doped GaN layers using metalorganic chemical vapor deposition (MOCVD) has shown to suffer from memory effects.9) Even after the precursor has been removed from the growth chamber, iron will be present on the GaN surface. This allows for further incorporation and gives an exponential decrease of Fe-concentration versus thickness. Therefore, obtaining a low doped channel region together with a highly doped buffer is a big challenge.

Carbon may be incorporated by tuning the growth process parameters such as pressure, temperature and precursor flow rates. This procedure may introduce a trade-off between C-concentration and the general crystalline quality of the GaN. An alternative method is to add a carbon precursor. Using this procedure, the growth can be optimized for GaN material quality and the C-concentration is solely controlled by the flow of C precursor gas. This method could lead to better crystal quality and at the same time provide a large freedom in designing the doping profile. In a recent study several carbon containing gases that potentially could be used for in-situ carbon doping of GaN were examined.10)

In this study we present fabrication and characterization of a HEMT fabricated on an AlGaN/GaN heterostructure with a stepped C-doped buffer, which is grown using propane as a carbon precursor. DC measurements were performed to characterize isolation properties and pulsed current–voltage (I–V) measurements were used to characterize trapping effects. Finally, large signal RF performance was measured by load–pull.

2. Methods

The AlGaN/GaN heterostructure was grown in a horizontal hot-wall MOCVD reactor11) on a quarter of a 3-in. (0001) 4H-SiC on-axis semi-insulating wafer. The HEMT heterostructure consisted of five III-nitride layers; in the bottom an AlN nucleation layer, a 23 nm Al0.19Ga0.81N barrier layer, on top a 3 nm GaN cap layer, Fig. 1. When growing the AlN nucleation layer the temperature was 1170 °C and the remaining GaN/AlGaN/GaN structure was grown at 1040 °C. All layers were grown at a process pressure of 50 mbar. Trimethylgallium (TMGa), trimethylaluminum (TMAI), and ammonia (NH3) were used as precursors for Ga, Al, and N, respectively. Propane (C3H8)
gas was used as a carbon doping precursor during the growth of the doped GaN layer. The carbon concentration in the GaN-layers was measured using secondary ion mass spectrometry (SIMS) as shown in Fig. 1. A more detailed description is presented elsewhere.\(^{12}\)

HEMT fabrication started with deposition of 55 nm of Si-rich SiN passivation layer in a low pressure chemical vapor deposition (LPCVD) system.\(^{13}\) Mesas were made with optical lithography and dry etching. Self-aligned recessed ohmic contacts were defined using optical lithography, followed by recess etching with a Cl–Ar plasma and evaporation of the metal stack, Ta/Al-Ta (10/280/20 nm).\(^{14}\) The contacts resistance was 0.33 \(\Omega\) mm as measured with the transfer length method. Gates with length of 0.2 \(\mu\)m were defined in a two-step electron beam lithography process. In the first step the gate footprint was defined and etched in the SiN-passivation. The second step defined the gate-metallization consisting of a Ni/Pt/Au-stack (30/20/400 nm). Contact pads were defined with optical lithography and a Ti/Au/Ti metallization was evaporated. The source–drain distance was 2.4 \(\mu\)m and the gate–drain distance was 1.7 \(\mu\)m.

### 3. Results and discussion

Using Eddy current technique and a contactless Lehighton system on the bare, unprocessed wafer the carrier concentration \((n_s)\), mobility \((\mu)\), and sheet resistance \((R_{sh})\) were measured. After passivation and HEMT fabrication the same parameters were extracted again using Hall measurements on van der Pauw structures, Table I. When comparing the two measurements it was found that \(R_{sh}\) remained unchanged while \(\mu\) increased and \(n_s\) decreased.

DC measurements were performed on 2 × 25 \(\mu\)m devices using a parameter analyzer. The \(I–V\) measurements showed no indication of short channel effects suggesting good carrier confinement in the channel [Fig. 2(a)]. Table II contains extracted values of the saturated drain current \((I_{DSS})\), on-resistance \((R_{ON})\), transconductance \((g_m)\), subthreshold slope (SS), and drain induced barrier lowering (DIBL). SS was extracted from the transfer characteristics in the subthreshold regime using

\[
SS = \frac{\delta V_{GS}}{\delta \ln I_D},
\]

where \(V_{GS}\) is the gate source voltage and \(I_D\) is the drain current. DIBL was calculated using

\[
\text{DIBL} = \frac{V_{DD} - V_{TH}}{W/L},
\]

![Fig. 2. (Color online) DC characteristics: Drain current versus drain voltage for \(V_{GS} = -3 : 0.5 : 1\) V (a). The leakage current in the GaN buffer layer (b). Threshold voltage versus drain voltage (c). (Inset) Drain and gate currents at \(V_{DS} = 10\) V as a function of gate voltage. Drain–gate voltage as a function of gate–source voltage whilst keeping a constant drain current (d).](image-url)
was so severe that current saturation did not occur even at the whole doping concentration comparable to the concentration in the much larger value of DIBL. The highly doped sample had a to the UID channel presented in this paper, which resulted in value of DIBL. The low value of DIBL presented in this measurement setup).

Fig. 2(a) shows a sharp step in drain current when the drain voltage reached 25 V, which is the maximum rating of the isolation was very good up to at least 200 V (which is the maximum rating of the isolation in Fig. 2(c)]. The isolation was very good up to at least 200 V (which is the maximum rating of the measurement setup). Breakdown was measured using a drain-current injection technique with a constant current of 1 mA/mm [Fig. 2(d)]. A sharp step was seen at $V_{DS} = -2.5$ V followed by a shallower slope where channel breakdown occurs. $V_{DS}$ finally saturated at 120 V, giving a breakdown field of 70 V/µm. This value was twice as high as for the highly doped sample in Ref. 15, Table III.

These buffers had a uniform doping throughout the whole buffer while the device layout was the same. The lowly doped sample had a doping concentration comparable to the UID channel presented in this paper, which resulted in a much larger value of DIBL. The highly doped sample had a doping concentration comparable to the concentration in the buffer presented in this paper and showed a very similar value of DIBL. The low value of DIBL presented in this paper was attributed to the high buffer isolation.

The isolation of the buffer was further characterized by measuring the current between two mesa-isolated contacts with a distance of 5 µm [Fig. 2(c)]. The isolation was very good up to at least 200 V (which is the maximum rating of the measurement setup). Breakdown was measured using a drain-current injection technique with a constant current of 1 mA/mm [Fig. 2(d)]. A sharp step was seen at $V_{GS} = -2.5$ V followed by a shallower slope where channel breakdown occurs. $V_{DS}$ finally saturated at 120 V, giving a breakdown field of 70 V/µm. This value was twice as high as for the highly doped sample in Ref. 15, Table III.

Pulsed $I-V$ measurements were performed from different quiescent bias points (Fig. 3). The pulse length was set to 1 µs and a period time of 1 ms was used. Profound knee walk-out effects were found starting from $(V_{GSQ}, V_{DSQ}) = (-6, 15)$. At $(V_{GSQ}, V_{DSQ}) = (-6, 25)$ the knee walk-out was so severe that current saturation did not occur even at a $V_{DS}$ of 20 V. The more severe dispersive effects at larger quiescent drain biases indicate that the responsible traps are located in the buffer region and should be related to the C-incorporation.

Large signal measurements were performed in an active load–pull setup at 3 GHz on a 2 × 50 µm device. A Class AB condition was used with a quiescent current of 15% of

$$DIBL = -\frac{\delta V_{TH}(V_{DS})}{\delta V_{DS}},$$

where $V_{TH}(V_{DS})$ is the threshold voltage, extracted at a drain current of 1 mA/mm, as a function of drain bias.

The large $R_{ON}$ was mainly influenced by the high $R_{db}$. Due to the good isolation of the buffer, low leakage currents of 2 × 10$^{-6}$ A/mm were measured. The threshold voltage ($V_T$) remained very stable for wide range of drain voltages [Fig. 2(b)], giving low values of DIBL. The results can be compared with values from residually C-doped buffers, Table III. These buffers had a uniform doping throughout the buffer in this work. The lowly doped sample had a doping concentration comparable to the UID channel presented in this paper, which resulted in a much larger value of DIBL. The highly doped sample had a doping concentration comparable to the concentration in the buffer presented in this paper and showed a very similar value of DIBL. The low value of DIBL presented in this paper was attributed to the high buffer isolation.

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Large signal measurements were performed in an active load–pull setup at 3 GHz on a 2 × 50 µm device. A Class AB condition was used with a quiescent current of 15% of

Table II. DC characterization results. $I_{DSS}$ was extracted at $V_{GS} = 1$ V, $g_m$ and SS at $V_{DS} = 10$ V. DIBL was extracted at $V_{DS} = 30$ V.

<table>
<thead>
<tr>
<th>$I_{DSS}$ (A/mm)</th>
<th>$R_{ON}$ (Ω-mm)</th>
<th>$g_m$ (mS/mm)</th>
<th>SS (mV/dec)</th>
<th>DIBL (mV/V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.7</td>
<td>2.6</td>
<td>300</td>
<td>140</td>
<td>0.13</td>
</tr>
</tbody>
</table>

Table III. DIBL and breakdown fields for residually C-doped buffers compared with the intentionally C-doped buffer in this work.

<table>
<thead>
<tr>
<th>Reference</th>
<th>C-conc. (cm$^{-2}$)</th>
<th>DIBL (mV/V)</th>
<th>Breakdown field (V/µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td>$1 \times 10^{16}$</td>
<td>22.4</td>
<td>25</td>
</tr>
<tr>
<td>15</td>
<td>$5 \times 10^{17}$</td>
<td>0.12</td>
<td>35</td>
</tr>
<tr>
<td>This work</td>
<td>$3 \times 10^{16}/1.5 \times 10^{18}$</td>
<td>0.13</td>
<td>70</td>
</tr>
</tbody>
</table>

Fig. 3. (Color online) Pulsed $I-V$ measurements showing $I_{DSS}$–$V_{DS}$ for $V_{GS} = 1$ V when pulsed from different quiescent states, $(V_{GSQ}, V_{DSQ})$.

Fig. 4. (Color online) Delivered output power, transducer gain and drain efficiency versus available input power for $V_{DSQ} = 25$ V (a). Load-lines from the measurements resulting in the highest output power for four different $V_{DSQ}$ (b).

$I_{DSS} = 15, 20, 25$, and 30 V. A power sweep was performed at the load optimized for highest output power. At a quiescent drain bias of 25 V the largest output power was measured to 1.3 W/mm with a drain efficiency of roughly 25% [Fig. 4(a)]. The highest output power along with gain and drain efficiency for the four quiescent biases are listed in Table IV. Even though the largest output power was found at $V_{DSQ} = 25$ V, biasing at 15 and 20 V gave virtually equal...
output power while offering larger drain efficiencies. By examining the load-lines this behavior was attributed to severe knee walkout and current collapse [Fig. 4(b)]. A further increase of $V_{DSQ}$ to 30 V resulted in a reduced output power. It can be noted that the magnitude of the current collapse and knee walkout effects seen in the load-lines corresponds well with the results from the pulsed $I–V$ measurements.

4. Conclusions

HEMTs have been fabricated on an AlGaN/GaN heterostructure with a C-doped GaN buffer. Carbon incorporation was achieved by introducing propane gas in the growth chamber and the doping concentration was controlled by the gas flow. As compared to C-incorporation using residual carbon in the growth chamber this method enables optimization of high quality GaN growth and control of the C-doping concentration simultaneously.

The HEMTs were characterized with respect to isolation and dispersion. The devices showed low OFF-state current and values of DIBL, owing to the good isolation in the buffer. Large dispersive effects, such as current collapse and knee walkout, were measured using pulsed $I–V$ and load–pull. The passivation used in this work has previously been shown to result in low current collapse and little knee walkout.\(^{18}\) The dispersive effects can therefore be attributed to traps in the GaN buffer layer demonstrating the need for further optimization of the carbon doping profile of the buffer and the material quality of GaN in the channel region.

Table IV. Maximum output power, gain and drain efficiency for four different quiescent drain biases.

<table>
<thead>
<tr>
<th>$V_{DSQ}$ (V)</th>
<th>$P_{out}$ (dBm)</th>
<th>Gain (dB)</th>
<th>Drain efficiency (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td>21.0</td>
<td>8.4</td>
<td>35.5</td>
</tr>
<tr>
<td>20</td>
<td>21.1</td>
<td>8.4</td>
<td>28.6</td>
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<tr>
<td>25</td>
<td>21.1</td>
<td>9.5</td>
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</tr>
<tr>
<td>30</td>
<td>20.8</td>
<td>9.2</td>
<td>21.0</td>
</tr>
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</table>

**Acknowledgements**

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Paper E

Electron Trapping in Extended Defects in Microwave Al-GaN/GaN HEMTs with Carbon Doped Buffers


Submitted to IEEE Transactions on Electron Devices.
Electron Trapping in Extended Defects in Microwave AlGaN/GaN HEMTs with Carbon Doped Buffers

Johan Bergsten, Mattias Thorsell, Member, IEEE, David Adolph, Jr-Tai Chen, Olof Kordina, Einar Ö. Sveinbjörnsson, and Niklas Rorsman, Member, IEEE

Abstract— This paper investigates AlGaN/GaN high electron mobility transistors (HEMTs) fabricated on epi-structures with carbon (C) doped buffers. Metalorganic chemical vapor deposition is used to grow two C-doped structures with different doping profiles, using growth parameters to change the C-incorporation. The C-concentration is low enough to result in n-type GaN. Reference devices are also fabricated on a structure using iron (Fe) as dopant, to exclude any process related variations and provide a relevant benchmark. All devices exhibit similar DC-performance. However, pulsed-IV measurements show extensive dispersion in the C-doped devices, with values of dynamic Ron 3-4 times larger than in the DC-case. Due to the extensive trapping, the devices with C-doped buffers can only supply about half the output power of the Fe-doped sample, 2.5 W/mm compared to 4.8 W/mm at 10 GHz. In drain current transient measurements the trap filling time is varied, finding large prevalence of trapping at dislocations for the C-doped samples. The measurements indicate that clusters of C around the dislocations are the main cause for the increased dispersion.

Index Terms— GaN HEMT, Dispersion, Buffer doping, Iron, Carbon, Dislocations

I. INTRODUCTION

Output power and linearity in GaN HEMTs is still limited by DC-RF dispersion in form of current collapse (CC) and increased ON-resistance (Ron). Dispersion is due to trap states in the device, mainly at the surface of the barrier or in the GaN buffer [1]. The effect of the surface traps can be mitigated by the use of passivation layers and field-plates [2], [3]. Electron trapping in the buffer is perhaps more challenging since it involves both unintentional doping as well as intentional deep level acceptors (to render the buffer semi-insulating). A highly resistive buffer is critical in order to prevent short channel effects and decrease leakage currents [4]. A tradeoff between dispersion and insulation has to be made.

The most common way to achieve high resistive GaN is to introduce iron (Fe) or carbon (C) which form deep acceptors [5], [6]. Currently, doping the buffers with Fe is the industry standard, although C-doped buffers are still intensely investigated [7]–[10]. The advantage with C-doping, compared to Fe-doping, is the ability to control the doping concentration in a step like fashion, enabling better control of the impurity level in the channel region [5]. In metalorganic chemical vapor deposition (MOCVD) the most common way to control the C-concentration is to change growth conditions to control incorporation of residual carbon in the chamber [11], [12], but adding a separate C-precursor is also possible [13].

For power applications a high C-concentration (~10^19 cm^-3) is usually required to enable high breakdown voltages. Such high concentrations have shown to render GaN p-type [14]. Several studies have dealt with the behavior of such buffers, where the pn-diode formed between the 2DEG and the buffer results in almost complete current collapse [15], [16]. In these cases dislocations are regarded necessary to provide a discharging path for trapped charge [17]. However, in microwave applications lower biases are used and lower C-concentrations (<10^18 cm^-3) are needed for proper isolation. For GaN grown with MOCVD, C-concentrations around 10^18 cm^-3 gives a net n-type doping [14]. Since C is used to compensate donors it is likely that the C-concentration required to render GaN p-type varies depending on other impurity levels. In weakly compensated structures a different trapping behavior is expected since no pn-diode is present and the dislocations could have a different and adverse effect [18], [19]. However, this has not been thoroughly investigated and it is rarely indicated in the literature whether the C-doped buffers are actually p- or n-type.

This paper aims to improve the understanding partially compensated C-doped buffers in relation to trapping effects. This is achieved by investigating three AlGaN/GaN epitaxial structures utilizing different doping strategies. Two structures with different C-doping profiles are used, with C-concentration low enough to expect a n-type buffer [14]. Furthermore, a Fe-doped sample is used as a reference to verify that the HEMT-process itself is not limiting the performance of the C-doped samples. It also provides a benchmark to an industry standard.
HEMTs are fabricated and are evaluated in terms of insulation, breakdown, trapping effects, and output power. The main part of the trapping analysis is carried out using drain current transient measurements, performed at both different temperatures and with different trap filling times [18]. The results demonstrate the importance of the interplay between dislocations in the GaN buffer and the C dopants.

II. EXPERIMENTAL

The HEMT structures were grown on 4-inch semi-insulating SiC substrates. The C-doped structures were grown using a hot-wall MOCVD system [20] and the carbon incorporation was controlled by changing the growth conditions [12]. The first structure had a stepped doping profile (denoted Stepped:C), previously shown to give a good trade-off between insolation and dispersion [21]. The second had an exponential C-doping profile (Exp:C), made to mimic the profile of a Fe-doped structure. Fig. 1 shows the doping profiles together with C-concentration of the two samples. The Fe-doped sample was grown by Cree using their proprietary Fe-doping process (Exp:Fe). The three structures had a barrier consisting of 1 nm AlN exclusion layer, 11 nm of AlGaN with 30% Al content and a GaN cap with a thickness of 2 nm. Furthermore, the unintentionally doped (uid) structure from [21] is used to facilitate the discussion of the role of dislocations in C-doped buffers (denoted Low:C). Since this sample has already been thoroughly investigated, it is only included where new information is presented (section III-A and III-E). In short, Low:C is virtually dispersion free but its output power is limited by higher leakage current at high V_DS.

The HEMT processing follows the procedure already described in [22]. The devices were passivated using a 55-60 nm silicon nitride layer, deposited by low pressure chemical vapor deposition (LPCVD). Recessed, Ta-based ohmic contacts [23] produced contact resistances of ~0.4 Ω·mm for all samples. The devices had a gate length of 0.2 µm, a source-drain distance of 2.8 µm and a gate-drain distance of 1.8 µm.

III. RESULTS

A. Material characterization

The three buffers were confirmed to be n-type using the Kelvin-probe force microscopy (KPFM) technique used in [14]. Hall measurements were performed on van der Pauw structures. The three samples showed similar values of electron mobility (~1800 cm²/V·s) and carrier concentration (~1.1·10¹³ cm⁻²), indicating that the buffer compensation did not affect the channel region.

The structural quality of the GaN buffer layers were examined with X-ray diffraction (XRD) using a Panalytical X’Pert PRO MRD. Table I shows the mosaicity (tilt Δω₀ and twist Δωₖ) which was determined by recording the full-width-at-half-maximum (FWHM) of x-ray rocking curves (XRCs) across the on-axis symmetric (0002) reflection and across the skew-symmetric (3032) reflection. The (3032)-reflection was chosen due to the large lattice plane inclination (70.5°) with respect to the (0002)-plane, giving a larger sensitivity to edge-type threading dislocations (TD:s). Equation (2) from [24] was used to calculate the amount of screw (ρₛ) and edge (ρₑ) type TD:s as presented in Table I. It should be noted that although this method gives an overestimation of the dislocation densities, the relative difference between the samples is still comparable. Approximately the same densities of screw TD:s are observed for all four samples indicating a similar crystal quality with respect to the tilt. However, about three times more edge TD:s are present for samples Stepped:C and Exp:C compared with Low:C and Exp:Fe. This is an indication that changing C incorporation by adjusting GaN growth parameters sacrifices crystal quality.

B. DC

The output characteristics and transconductance of the HEMTs were measured as shown in Fig. 2. Overall, the different buffer doping strategies did not affect the channel region, since the maximum current (I_DS ≈ 1.0 A/mm), on-resistance (R_ON ≈ 2 Ω·mm), and transconductance (g_m ≈ 400 mS/mm) was similar in all samples. However, in contrast to Exp:Fe, the C-based samples showed an obvious kink effect, causing a shift in V_T for large V_DS. The absence of the kink effect in Exp:Fe indicates that the responsible trap could be associated with the C-incorporation. Alternatively, it could be related to some other defect caused by the different growth conditions used for the C-doped samples. DC-parameters related to buffer insulation were extracted, Table II. The breakdown voltage was measured using the drain current injection technique described in [25] with a current of 1 mA/mm. The similar breakdown values indicated comparable Schottky contacts in the three samples. From the breakdown measurement the drain induced barrier lowering (DIBL) was calculated as a derivative of V_DS with respect to V_DS. Using this technique DIBL can be extracted as a function of V_DS. The DIBL of Exp:C was distinctly higher than the other samples, indicating a poor confinement at high voltages. The mesa isolation was measured at 15 µm separation at 200 V. The C-
doped samples showed similar resistance levels whereas the isolation in Exp:Fe was approximately an order of magnitude larger.

C. Pulsed-IV

Pulsed IV-measurements were performed to investigate trapping effects using a dynamic IV analyzer (AMCAD AM3200). The pulse width was 1 μs with 10 ms period time. Fig. 3 shows measurements pulsed from three different quiescent points; the reference point \((V_{GS0}, V_{DS0}) = (0,0)\ V\) and two active points; \((V_{T-2},0)\) and \((V_{T-2},50)\ V\). The \((V_{T-2},0)\) quiescent point is assumed to activate traps on the surface, close to the gate. For Exp:Fe the measurements at quiescent point \((0,0)\) and \((V_{T-2},0)\) overlap, indicating no trapping in the gate region. The C-doped samples both showed a slight decrease in current (~5 %). Since the same passivation was employed for all samples the current decrease could possibly be related to trapping in the barrier layers. By also including a quiescent state of 1 mA/mm, DIBL was extracted at \(V_{DS} = 40\ V\) and the mesa isolation at \(V_{DS} = 200\ V\).

\[ I_{DS} = \frac{1}{1 - \sum_{i=1}^{N} \alpha_i \cdot \exp\left(-\frac{t}{\tau_i}\right)^{\beta_i}} \]

where \(I_{DS}/I_{DS,q}\) is the drain current normalized by the quiescent drain current, \(\alpha_i\) is the amplitude of the trapping effect, \(\tau_i\) is the trapping/de-trapping time constant, \(\beta_i\) is the stretching term and \(N\) is the number of traps. This model has been found to give the most accurate results in terms of time constants and activation energies [18]. Furthermore, the stretching term can give additional information regarding the trapping/de-trapping processes. A stretching term close to 1 implies that the trap behaves like a point defect with a distinct energy level, whereas a small stretching term has been connected to trapping centers forming a continuous distribution of energy levels rather than a discrete level [26], or the trapping/de-trapping kinetics being governed by hopping [27] or tunneling [28]. An Arrhenius plot was used to extract the activation energies and capture cross sections of the traps as shown in Fig. 5 and Table IV. The effects of self-heating was taken into account by evaluating the thermal resistance of the devices (~5 K mm/W) using the method described in [29] and calculating an effective device.

D. Drain Current Transient – Temperature Dependence

To investigate trapping time constants and activation energies, drain current transient (DCT) measurements were performed. The devices were pulsed to an off-state bias point \((V_{GS},V_{DS}) = (V_{T-2},50)\) for 1 ms, followed by sampling of the current response in an on-state bias point for \((1,7)\ V\) 10 s. The off-state bias point was chosen to mostly activate traps in the buffer region. Measurements were performed at temperatures ranging from 0 to 100 °C, Fig. 4. Four different traps, labeled T1-T4, were identified. T1 and T2 were present in both the C-doped samples, whereas T3 was only found in Exp:C. T4 were found in Exp:Fe.

To further analyze the data and extract the trapping/de-trapping time constants, the measurement data was fitted to a model based on stretched exponentials;
The activation energy of trap T1 was close to zero in both Stepped:C and Exp:C. Furthermore, the stretching term of T1 was small (~0.5). Due to this, hopping or tunneling are the likely mechanisms governing the emission process of T1. The trap T2 showed a bent, non-Arrhenius behavior so no activation energy could be extracted. The same response has recently been found for a leakage process through C-doped GaN and is explained by conduction through a defect band [31]. In our case, this should imply that negative charge is trapped deep in the structure and is functioning as a back-gate until it is released to the 2DEG through the leakage process, as discussed in [16]. In [31], the defect band is shown to be close energetically to the \( C_N \) level \((C\text{ in nitrogen substitutional position})\) which is situated at \( E_V + 0.9 \text{ eV} \). Furthermore, charge trapped at \( C_N \) is assumed to be emitted through the defect band. In our samples, the activation energy and capture cross section of T3 corresponds well with that of hole emission from \( C_N \) [8]. Furthermore, the stretching term of T3 was close to 1, supporting \( C_N \) as a likely origin. Since T3 was only detected in Exp:C, and the amplitude of T2 was obviously larger in Exp:C, this supports a similar process (emission assisted by the defect band) in our samples. In Exp:Fe, both the activation energy and the stretching term (~1) strongly suggests that T4 was related to a well-known point defect which has been found to correlate with Fe-incorporation [32], [33].

By varying the time spent in the off-state (filling time), further information regarding the trapping kinetics can be obtained [18]. In this type of measurement a dependence of trapping amplitude on filling time is related to the presence of highly localized defect states, such as dislocations. This is due to the buildup of a repulsive Coulomb barrier formed by the already trapped electrons, decreasing the capture cross-section [34]. Furthermore, trap-states along dislocations can have capture cross-sections varying with several orders of magnitude [35]. Thus, for longer filling times traps with smaller capture cross-sections are more likely to be filled. Reversely, the smaller capture cross-section will also increase the time for emission.

Measurements with filling times ranging from 100 \( \mu \text{s} \) to 10 s were performed using the same bias as in section III-D, Fig. 6. The two C-doped materials showed similar behavior; T1 and T2 were largely dependent on filling time. The amplitude of T1 saturated at a filling time of 10 ms but a second peak was formed with a larger time constant. The second peak was shifting and increasing in amplitude with longer filling times and did not saturate even at a filling time of 10 s. The results give a clear indication that T1 in Stepped:C and Exp:C are related to trapping at highly localized states, most probably dislocations. The increasing amplitude of T2 with increasing filling time could be due to the charging being limited by the rather slow leakage process.

In Exp:Fe, T4 was unaffected by filling time, in agreement with it being due to point defect. However, for longer filling times, a trap similar to T1 was found. The Fe-doped sample required approximately a factor of 1000 longer filling time to reach the same amplitude of T1 as in the C-doped samples. If
this trap is indeed related to the same defect as T1, the lower dislocation density alone could not explain the large difference in capture cross section. In any case, a direct comparison between Exp:Fe and the C-doped samples in this regard is difficult since they have been grown in different reactors using different growth recipes. For filling times longer than 100 ms some charging and subsequent discharging was also recorded around 1 s after the start of sampling. The signature is similar to T2 so it is possible that the process explained above is also present in the Fe-doped buffer.

Measurements were also performed using an off-state bias of \((V_{GS},V_{DS}) = (V_T-2,20)\) V, Fig. 7. For a lower drain bias, buffer traps close to the channel will still be activated whereas traps deep in the buffer will not. This allows us to probe an area of the buffer where the largest difference between Exp:C and Stepped:C is expected (see Fig. 1). In this case, Stepped:C showed the same general behavior as in Fig. 6 (large off-state drain bias), aside from lower amplitudes of the peaks. However, Exp:C did not show T1 or the broadening of T1 for longer filling times. Given the similar dislocation densities for Stepped:C and Exp:C, this implies that T1, and the broadening of T1, was rather related to the difference in C-concentration. According to [36], [37] C-dopants can form complexes along dislocations. It is likely that this is the case also in our samples. The complexes are presumably accessed through the dislocations, leading to the observed filling time dependence.

The de-trapping mechanism is likely tunneling based which would explain the low activation energy and capture cross section for T1 [38].

For Exp:Fe the amplitude of T4 decreased slightly for the low off-state drain voltage, and no sign of the trap similar to T1 was found.

Filling time dependent measurements were also performed on the Low:C sample, Fig. 8. In this case the off-state voltage was set to \((V_{GS},V_{DS}) = (V_T-2,25)\) V. Due to the poor insulation of the buffer this was the maximum off-state drain bias which could be properly pinched off in the transistor. The on-state bias was kept at \((V_{GS},V_{DS}) = (1,7)\) V. For Low:C only a slight trace of T2 was found for a 10 s filling time. Other than that no trapping was recorded for any filling time. Therefore, it is reasonable to assume that the T1 trap is enabled by a C-presence, confirming what was found when comparing Exp:C and Stepped:C at a low off-state drain bias.
Load-Pull

Load-pull measurements were performed at 10 GHz at quiescent drain biases of 10 V and 30 V for a class AB bias point ($I_{DS} = 15\%$ of $I_{DSS}$) using an active load-pull system [39]. The output impedance was optimized for high output power. Delivered output power and drain efficiency are plotted versus input power for the two quiescent drain biases in Fig. 9a. At $V_{DSQ} = 10$ V the three samples behaved similarly, achieving the same output power (~1.6 W/mm) and efficiency (~50%). However, at $V_{DSQ} = 30$ V the gain in Exp:C and Stepped:C decreased rapidly at higher input power levels, causing a lower output power and drain efficiency. Exp:Fe, exhibited no such problems and reached a maximum output power of 4.8 W/mm, compared to 2.0 and 2.6 W/mm for Stepped:C and Exp:C respectively. The drain current-voltage waveforms (load-lines) for the measurement resulting in the maximum output power at each quiescent bias is shown in Fig. 9b. Trapping was clearly limited for low drain biases. On the other hand, at $V_{DSQ} = 30$ V the performance of the C-doped samples was limited by a severe increase in $R_{ON}$ and a large decrease in $I_{DS}$. Exp:Fe suffered from increased $R_{ON}$ and only a minor decrease in drain current.

From the filling time measurements it is clear that a long time has to be spent in a high field bias point to fill a large number of the available trap states. However, in the CW case, the trap filling time is related to the operating frequency and should in our case be of the order of 0.1 ns. Still, the current available in the CW case is much lower than expected from the DCT case with an assumed filling time of 0.1 ns. This is because the time the device is biased in a discharging state is also related to the operating frequency in the CW case. At each new period, instead of a recovered buffer, some traps will still be filled. By extension, a steady-state condition will form, where a certain number of traps are always filled and only a few are filled and discharged during a full cycle. This would explain the consistency between the increased trapping in the DCT case and the lower output power in the CW case for the C-doped materials compared to Exp:Fe.

IV. DISCUSSION

Since C-doped buffers are mainly used in power switching applications the trapping evaluation is usually performed with these applications in mind. For these devices a high C-concentration is required which has shown to render the GaN p-type [40]. The pn-diode formed between the p-type GaN and the 2DEG is expected to lead to extensive current collapse [15], and dislocations are expected to mitigate these effects [17]. In our case the C-concentration is significantly lower, giving n-type GaN. In this case, the dislocations may have an adverse effect, acting as trapping centers. The filling time dependent DCT measurements show an increasing amplitude of trap T1 for longer filling times, indicating trapping at dislocations [18]. However, T1 still seems to be enabled by a C-presence, since no sign of T1 is found in Low:C. Even though Low:C has a lower dislocation density it is unlikely that the large difference in T1 amplitude is related to the relatively small difference in dislocation density as compared to the large difference in C-concentration. C has previously been found to form clusters around dislocations [36]. Consequently, T1 can be attributed to trapping at C-clusters around dislocations, schematically depicted in Fig. 10. The main current transport mechanism is thought to be tunneling or hopping since the activation energy of T1 is close to 0 eV.

From the DCT measurements the T2 and T3 traps seem to be connected. As explained in [16], charge can be trapped in the GaN/AlN-nucleation interface if the CN level is present. The polarization gradient produces a band bending in the GaN, creating vacant CN levels, as indicated in Fig. 10. Under electrical stress these states will be filled, acting as a back-gate. This process is observed as T3 in our samples. When the
trapped electrons are released they are transported to the 2DEG by means of a defect band, as described in [31]. It is this defect band that gives the characteristic temperature dependence of the T2 signature. Since T2 was detected in all sample (although very weakly in some cases), the defect band is most probably always present. However, in order for any significant charge to get trapped in the GaN/AIN interface an acceptor close to the valence band maximum are needed. Such a state was only present in large concentration for Stepped:C and Exp:C. Currently, it is not clear how the defect band is formed. Possibly, it is also related to dislocations. It should also be noted that the amplitude of T2 is much smaller compared to T1 in Exp:C and Stepped:C. A possible solution for T1 in these structures might be n-doping or polarization engineering in the GaN/AIN interface, removing the vacant C− levels.

Interestingly, only Exp:C showed the discrete C-related trap level, T3, even though the C-concentration for Stepped:C was larger in the vicinity of the channel. Since three different growth conditions were used to grow the GaN in Stepped:C and a continuous set was used in Exp:C this indicates that the growth conditions do not just affect the C-concentration, but also where C is incorporated in the crystal. Further investigations on the dependence of growth conditions on the C-incorporation in the GaN crystal are required and the importance of the defect band should be explored in both n- and p-type C-doped buffers.

V. CONCLUSION

We have found that trapping at highly localized states in weak C-doped buffers severely limits microwave output power for GaN-based HEMTs at large electrical fields. The majority of the trapping seems to be enabled by C forming complexes around dislocations and, to a smaller extent, trapping at the GaN/AIN-nucleation interface. To enable a legitimate comparison between C and Fe as deep acceptors in GaN, precise control of the configuration of C in the GaN crystal is desirable. Future studies on C-doped buffers for microwave applications should focus on minimizing the interaction between C and the dislocations. Probably, this is easier to achieve if the C-concentration is controlled by adding a C-carrying gas instead of changing growth parameters [13] and by using semi-insulating GaN substrates to minimize the dislocation density. Possibly, this could also reduce the presence of the defect band.

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REFERENCES


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