Design and fabrication of hidden hinge monocrystalline silicon micromirrors for maskless lithography

MARTIN BRING
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Cover:
Scanning electron microscope image of a 16×16 μm monocrystalline silicon hidden hinge mirror and a color illustration of the measurement method for high spatial resolution characterization of bond-interfaces.

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Abstract

Micromirror-based maskless lithography has recently received attention as an attractive candidate to tackle challenges associated with the continued device scaling in the semiconductor industry. The micromirrors work by diffraction and the requirements on planarity are very tough, e.g. peak-to-valley differences of a few nanometers. Increasing the resolution in future systems by decreasing the wavelength further increases the planarity requirements. This thesis deals with a novel micromirror structure intended to meet the planarity requirements in future optical maskless lithography systems.

The mirror consists of standing flexure hinges hidden underneath the mirror surface. Comprehensive mechanical analysis and simulations of the structure is presented and it is shown that the mirror can be designed to meet future planarity requirements. Even though the rewards are clear the realization poses several challenges which are addressed in this thesis.

The proposed fabrication process relies on aligned low temperature transfer bonding where the bond alignment accuracy is a critical parameter. A method to achieve submicron post bond alignment accuracy of non-transparent substrates is presented. Successful fabrication requires bonding of μm²-sized areas. A novel method for high spatial resolution mechanical characterization of such small bond interfaces is presented. The method achieves more than two orders of magnitude higher resolution than has been reported previously.

Another important challenge is the formation of the hidden monocrystalline silicon hinges. Simulations show that hinge widths down to tens of nanometers are required for future mirrors. A method based on local oxidation of silicon has been used to achieve hinge widths down to 20 nm. This method also tends to increase the uniformity across hinges due to stress dependent oxidation.

Arrays of monocrystalline silicon hidden hinge mirrors have been fabricated using a low temperature transfer process. Down to 16×16 μm² sized mirrors have been realized and actuation characteristics of fabricated mirrors agree with theory and simulations.

Keywords: micromirror, maskless lithography, low temperature transfer bonding, chevron notch, fracture toughness, isotropic etching, LOCOS
List of appended papers

This thesis is based on the work contained in the following papers:

A. **Novel monocrystalline silicon micromirrors for maskless lithography**
   Martin Bring and Peter Enoksson

B. **Monocrystalline silicon micromirror arrays fabricated by bulk micromachining and wafer bonding**
   Martin Bring and Peter Enoksson
   *Submitted to Journal of MEMS*

C. **Asymmetric oxidation in closely spaced trenches**
   Martin Bring and Per Lundgren
   *Submitted to Applied Physics Letter*

D. **Method for measuring fracture toughness of wafer-bonded interfaces with high spatial resolution**
   Martin Bring, Anke Sanz-Velasco and Peter Enoksson
   *Journal of Micromechanics and Microengineering, v16, n6 (2006) S68-S74*

E. **Submicron bond alignment accuracy using through-wafer holes**
   Martin Bring and Peter Enoksson
   *Proceedings of the 18th Micromechanics Europe Workshop, MME’07 Guimarães, Portugal (2007)*

F. **Micro pinball game demonstrating an easy MEMS transfer process using room temperature plasma bonding**
   Martin Bring, Anke Sanz-Velasco, Henrik Rödjegård and Peter Enoksson
   *Journal of Micromechanics and Microengineering, v13, n4 (2003) S51-S56*
The contribution by the author to the papers included in the thesis is as follows (see Figure I for the nomenclature used):

A. All experimental work, evaluation, and writing, major part of planning. Original idea from Professor Peter Enoksson.

B. All planning, experimental work, evaluation, and writing.

C. All planning, experimental work, and writing, major part of evaluation (all except SEM of 900 °C cross-sections).

D. All planning and writing, major part of experimental work (all except DCB sample preparation), evaluation (all except DCB measurements).

E. All planning, experimental work, evaluation, and writing.

F. Significant part of planning, all experimental work, evaluation, and writing. Original idea from Dr. Henrik Rödjeård and Dr. Anke Sanz-Velasco.

Figure I Explanation of the nomenclature used to describe the author’s contribution to the appended papers.
Papers not included due to overlap or being outside the scope of the thesis:

Novel monocrystalline silicon micromirrors for maskless lithography
Martin Bring and Peter Enoksson
Transducers’07, Lyon, France (2007)

Calibration methods of force sensors in the micro-Newton range
A. Nafari, F. A. Ghavanini, M. Bring, K. Svensson and P. Enoksson
Journal of Microengineering and Microengineering v17 (2007) S2102-2107

Sensors and actuators based on SOI materials
Anke Sanz-Velasco, Alexandra Nafari, Henrik Rödjegård, Martin Bring, Karin Hedsten, Peter Enoksson and Stefan Bengtsson
Solid State Electronics, v50 (2006), S865-876

Method for measuring fracture toughness of wafer-bonded interfaces with high spatial resolution
Martin Bring, Anke Sanz-Velasco and Peter Enoksson
Eurosensors XX, Göteborg, Sweden (2006)

Resonant mass loading calibration method for nanoindenter force sensor
A. Nafari, F. A. Ghavanini, M. Bring and P. Enoksson
Eurosensors XX, Göteborg, Sweden (2006)

Low temperature plasma-assisted-wafer-bonding for MEMS
Anke Sanz-Velasco, Martin Bring, Henrik Rödjegård, Gert I. Andersson and Peter Enoksson
210th Meeting of The Electrochemical Society, Cancun, Mexico (2006)

Method for measuring fracture toughness of wafer-bonded interfaces with high spatial resolution
Martin Bring, Anke Sanz-Velasco and Peter Enoksson

Method for measuring fracture toughness of wafer-bonded interfaces with high spatial resolution
Martin Bring, Anke Sanz-Velasco and Peter Enoksson
2nd international workshop on wafer bonding for MEMS technologies, Halle, Germany (2006)
A micro direct methanol fuel cell demonstrator
Konrad Wozniak, David Johansson, Martin Bring, Peter Enoksson and Anke Sanz-Velasco

Novel method for evaluating bond strength of very small areas
Martin Bring, Peter Enoksson
Proceedings of the 16th Micromechanics Europe Workshop, MME’05 Göteborg, Sweden (2005)

Wafer bonding for MEMS
Peter Enoksson, Cristina Rusu, Anke Sanz-Velasco, Martin Bring, Alexandra Nafari, Stefan Bengtsson
Proceedings of the 8th International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, Quebec City, Canada (2005)

System aspects of a micro direct methanol fuel cell
David Holmdahl, Peter Enoksson, Martin Bring, Jonas Berg, Alexandra Nafari, David Karlén
Proceedings of the 16th Micromechanics Europe Workshop, MME’05 Göteborg, Sweden (2005)

Applications of SOI materials to quantum devices and microsystems
J. Piscator, A. Nafari, M. Bring, H. Rödjegård, A. Sanz-Velasco, P. Enoksson, O. Engström and S. Bengtsson
Presented at EUROSOI-2005 (Granada, Spain, January 17-19, 2005)

A micro direct methanol fuel cell demonstrator
Konrad Wozniak, David Johansson, Martin Bring, Peter Enoksson and Anke Sanz-Velasco

Micro pinball game demonstrating an easy MEMS transfer process using room temperature plasma bonding
Martin Bring, Anke Sanz-Velasco, Henrik Rödjegård and Peter Enoksson
Applications of plasma assisted wafer bonding
Petra Amirfeiz, Anke Sanz-Velasco, Martin Bring and Stefan Bengtsson
Proceedings of the Workshop on wafer bonding, Barcelona, Spain (2002)
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Acknowledgement

Many people have contributed in many different ways to this thesis. First of all I want to thank Prof. Peter Enoksson for the support you have given me during these years. I know we have not always agreed on everything but you have always been open for dialogue. I really appreciate all the discussions we have had on all various subjects ranging from the influence of the platen power on notching in the Bosch process to much more philosophical discussions. Your feedback has been indispensable for this thesis, thank you Peter.

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The financial support from VINNOVA under grant Nr P24336-1 is gratefully acknowledged.

Last but not least I thank my family for all their support and especially my fiancée Anna and my son Noel for reminding me that life do not only consist of micromachined silicon but is also plenty of other wonderful things.

Martin Bring

Göteborg
March 2008
**Acronyms**

<table>
<thead>
<tr>
<th>Acronym</th>
<th>Description</th>
</tr>
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<tbody>
<tr>
<td>ARDE</td>
<td>Aspect ratio dependent etching</td>
</tr>
<tr>
<td>BCB</td>
<td>Benzocyclobutene</td>
</tr>
<tr>
<td>BOE</td>
<td>Buffered oxide etch</td>
</tr>
<tr>
<td>BOX</td>
<td>Buried oxide</td>
</tr>
<tr>
<td>CMOS</td>
<td>Complementary metal oxide semiconductor</td>
</tr>
<tr>
<td>CVD</td>
<td>Chemical vapor deposition</td>
</tr>
<tr>
<td>DBR</td>
<td>Distributed Bragg reflector</td>
</tr>
<tr>
<td>DCB</td>
<td>Double cantilever beam</td>
</tr>
<tr>
<td>DRIE</td>
<td>Deep RIE</td>
</tr>
<tr>
<td>DUV</td>
<td>Deep UV</td>
</tr>
<tr>
<td>EUV</td>
<td>Extreme UV</td>
</tr>
<tr>
<td>FEA</td>
<td>Finite element analysis</td>
</tr>
<tr>
<td>FEM</td>
<td>Finite element method</td>
</tr>
<tr>
<td>IC</td>
<td>Integrated circuit</td>
</tr>
<tr>
<td>IR</td>
<td>Infrared</td>
</tr>
<tr>
<td>LOCOS</td>
<td>Local oxidation of silicon</td>
</tr>
<tr>
<td>LPCVD</td>
<td>Low pressure CVD</td>
</tr>
<tr>
<td>MEMS</td>
<td>Microelectromechanical system</td>
</tr>
<tr>
<td>MST</td>
<td>Microsystem technology</td>
</tr>
<tr>
<td>PECVD</td>
<td>Plasma enhanced CVD</td>
</tr>
<tr>
<td>PMGI</td>
<td>Polymethylglutarimide</td>
</tr>
<tr>
<td>RIE</td>
<td>Reactive ion etch</td>
</tr>
<tr>
<td>SCREAM</td>
<td>Single crystal silicon reactive etch and metal</td>
</tr>
<tr>
<td>SEM</td>
<td>Scanning electron microscope</td>
</tr>
<tr>
<td>SLM</td>
<td>Spatial light modulator</td>
</tr>
<tr>
<td>SOI</td>
<td>Silicon on insulator</td>
</tr>
<tr>
<td>TEOS</td>
<td>Tetra-ethoxy-silane</td>
</tr>
<tr>
<td>TMAH</td>
<td>Tetramethylammonium-hydroxide</td>
</tr>
<tr>
<td>UV</td>
<td>Ultraviolet</td>
</tr>
<tr>
<td>WEC</td>
<td>Wedge error compensation</td>
</tr>
<tr>
<td>WPH</td>
<td>Wafers per hour</td>
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</table>
Chapter 1

Introduction and background

Maskless lithography using micromirror-based laser pattern generators is a potential technology to solve a range of challenges related to the continued device scaling in the semiconductor industry. Both economical and technological incentives make micromirror-based lithography very promising. However, going to shorter wavelengths increases the requirements on the micromirror structure, e.g., planarity, sagging, surface-roughness and stability. This thesis deals with a novel micromirror structure intended to meet the increased requirements in future maskless lithography systems.

Micromirrors belong to a group of devices known as microelectromechanical systems (MEMS). A little more about MEMS and why to use it in maskless lithography is explained in section 1.2. After that an outline of the thesis is given in section 1.3 where the content of each chapter is briefly described, but first an introduction to maskless lithography.

1.1 Maskless lithography

Nanolithography is one of the most important technologies for the fabrication of integrated circuits (ICs). Mass production of ICs is today based on duplicating a prefabricated pattern, a so-called photomask or just mask (or reticle when using reduction optics), onto the wafer using a wafer stepper. Wafer steppers feature high throughput with >100 wafers per hour at a sufficient resolution which is the reason for their success in mass production [1].
However, with the continued device scaling the cost for a single mask set is becoming a severe problem. Projected costs of well over $1.5M USD per mask set is expected for the 45 nm node [2]. Writing patterns directly onto the wafer without the use of a mask is a very basic idea and several systems mainly based on electron beam lithography have been developed over the years [3]. This used to be called direct write lithography but currently the term maskless lithography or ML2 is more common.

E-beam based systems usually features very high resolution with minimum features of tens of nanometers but poor throughput with several hours or even days per wafer [3]. Direct writing in IC fabrication is not a new concept and e-beam direct write lithography systems have been used in production especially for devices where the low gate density reduced the write time, e.g. GaAs MESFET and MMIC [3]. However, the cost and the technological challenges related to the development of a tool with higher throughput have long stifled the industry’s interest in maskless lithography. But recently economical incentives mostly related to the increasing mask cost but also reduction of time-to-market has again turned attention towards maskless lithography [3]. Another factor that contributes to the attention of maskless lithography is the coming of age of MEMS [1].

There are in principle two distinct technologies currently being pursued for maskless lithography; charged particle systems based on electron beams [4], and optical maskless lithography based on spatial light modulators (SLMs) consisting of arrays of micromirrors [5]. Common denominators can of course be identified but both technologies also have their own unique challenges. This thesis focuses on the opportunities and challenges related to designing and fabricating the micromirror array for a future optical maskless lithography system.

The working principle for optical maskless lithography has been described earlier [5-9] but for the sake of completeness a brief description is given here. Figure 1.1 shows the working principle for the only commercially available tool based on this technology, the Sigma7500 from Micronic Laser Systems AB [10]. This tool is intended for photomask manufacturing and the system can be described as a wafer stepper with a programmable reticle. The programmable reticle consists of the SLM into which the pattern data can be loaded. At the areas that are intended to be unexposed a voltage is applied which causes the micromirrors to be deflected. This deflection causes the incident light to be diffracted and stopped by the aperture. The diffractive operation of the SLM means that the mirrors only need to be deflected half a wavelength across the mirror in order to produce a black pixel. Further the SLM is operated in an analog mode which enables gray scaling. The gray scaling is
used to position the edges of features in the pattern on a finer grid than what correspond to the mirror size and reduction optics.

The mask blank which is placed on a continuously moving stage is unexposed at the areas where the mirrors are deflected and exposed at areas having flat mirrors. The light source used for the exposure is a pulsed laser with a very short pulse and high repetition rate. The short pulse generates a sharp image of the SLM in the resist despite the continuously moving stage. The next pattern is loaded into the SLM and the flash command which is controlled by an interferometer triggers the laser to flash again.

1.2 What is MEMS and why use it in maskless lithography?

Fabrication of devices with dimensions in the micrometer range is a popular field and consequently there are many names for what is in principle the same thing. In Japan it has been referred to as micromachines, in Europe the term microsystem technology or MST has frequently been used, and the most used acronym MEMS originates from the United States. Throughout this thesis the word MEMS will be used since it is very popular and has become synonymous with the art of miniaturizing mechanical elements like actuators and sensors. There are numerous examples of MEMS devices in everyday life, e.g. accelerometers as crash sensors for airbag systems in cars, printer heads in...
inkjet printers, pressure sensors for a wide range of applications, digital micromirror devices for projection display systems, and so on.

Needless to say the fabrication of devices with micrometer- or even nanometer-sized features is challenging. However, a part of the opportunity of miniaturization comes from the fabrication technique itself. The fabrication techniques used are adapted from IC manufacturing and allows for massive parallel fabrication. Each fabrication step can be performed on a high number (e.g. millions) of discrete components simultaneously (e.g. transistors, capacitors, mirrors, etc.) effectively reducing the fabrication cost per component. Another opportunity when miniaturizing devices is completely new fields of application due to the size of the device and/or utilization of the non-conventional behavior of miniaturized objects.

Micromirror arrays for maskless lithography constitute a good example of a device that utilizes many if not all of the advantages of miniaturization. As defined in Chapter 2 a micromirror chip needs several millions of individually movable mirrors which would be extremely hard to realize without the massively parallel fabrication offered by MEMS. Each mirror should also be able to move to distinct positions at a rate of several kHz which can be accomplished by electrostatic actuation and a high resonance frequency both of which are enabled by the miniaturization of the mirrors.

For the interested reader a good introduction to miniaturized transducers and microfabrication can be found in “Micromachined transducers source-book” by Gregory T.A. Kovacs [11] and “Fundamentals of microfabrication” by Marc J. Madou [12].

1.3 Thesis scope and outline

The scope of this thesis is the investigation of challenges and opportunities related to the fabrication of a novel micromirror structure suitable for future optical maskless lithography systems. The realization of large arrays based on this design is not investigated in this thesis but is of course considered, e.g. when choosing processes in the process plan.

Chapter 2 discusses requirements on the SLM and the general design of the electrostatically actuated micromirror with the emphasis on the deformation of the mirror surface. The impacts of fabrication related artifacts as well as the dynamics of the mirror structure are also discussed. Throughout the chapter comparisons are made to a current state-of-the-art deep ultraviolet (DUV) micromirror to illustrate the advantages of the herein presented micromirror. Most of Chapter 2 is based on Paper A and frequent references to this paper are made. The author recommends reading this paper before reading Chapter 2 since this will make it easier to follow the discussions in the chapter.
In Chapter 3 the experimental results from the fabrication of the micromirrors are discussed together with the pros and cons for the chosen fabrication process. The fabrication is done by a transfer process and requires the successful bonding of micrometer sized features. Already at an early stage it was clear that no suitable method existed to measure the bond strength of such small features. Chapter 3 also discusses and presents results from a new method that was developed within this work and which is capable of quantifying the bond strength of extremely small areas. The chapter is sprung from the results presented in Paper B-F which presents the bulk of the work on which this thesis is based.

The conclusions from the presented work are given in Chapter 4.
Chapter 2

Micromirror design

This chapter presents the requirements on micromirrors in order to be suitable for optical maskless lithography. The mirror structure related to the bulk of the work behind this thesis is also introduced and the challenges related to meeting the requirements for optical maskless lithography are discussed.

There are in principle two interesting types of mirrors for maskless lithography: tilting and piston micromirrors. The lithographic performance of both types has been investigated by others and it turns out that in order to achieve a comparable image fidelity between the two mirror types the arrays with piston micromirrors need to have around three times as many mirrors [6]. In section 2.1 it will be shown that even with tilting mirrors the number of mirrors needs to be extremely large and the mirror structure presented in section 2.2 is therefore a tilting micromirror.

2.1 Introduction and requirements on the micromirrors

Maskless lithography seems to be economically viable at a throughput of at least five 300 mm wafers per hour (WPH) [3]. This is equivalent to writing 100 mm² per second. Assuming a laser flash frequency of 10 kHz [9] the absolute minimum number of mirrors required on a chip in order to meet the throughput can be estimated. At $10^2$ mm²/s and $10^4$ Hz the required area to be printed each flash is $10^2/10^4=10^{-2}$ mm². For the 32 nm technology-node the number of “node pixels” per mm² is $(32\times10^{-6}\times32\times10^{-6})^{-1}\approx10^9$ mm⁻². This results in
10^9 \times 10^{-2} = 10^7 \text{ number of mirrors in order to meet the throughput of 5 WPH at the 32 nm node. This is the absolute minimum number of mirrors that are required given that it is possible to accurately write one “node pixel” with one mirror, Table 2.1.}

However, looking at the specifications for the only commercially available tool based on this technology, the Sigma7500 from Micronic Laser Systems AB [10], it has a useful resolution of about 130 nm which corresponds to approximately 1.5 mirror pixels [10,13]. The Sigma7500 also uses a multiple offset exposure scheme in order to average residual error sources. This increases the pattern accuracy but also lowers the throughput. Four exposures with different offsets are typically used for the tightest pattern requirements. A realistic DUV maskless lithography system for the 65 nm node with 60\times10^6 mirrors has been proposed [5]. This system is based on a flash frequency of 4 kHz, almost 5 mirrors per node pixel (30 nm mirror pixel size at wafer plane), and a 2 pass exposure scheme. 60\times10^6 is roughly 25 times more mirrors than stated in Table 2.1 which agrees well when updating the calculation for the 65 nm node with the new values for the flash frequency, mirrors per node pixel, and the number of passes, 10/4\times5\times2\times2.3\times10^6 = 25\times2.3\times10^6 = 60\times10^6. Needless to say this is a huge amount of mirrors and the realization of such an array, or large enough arrays for a multi-SLM approach [5], is challenging.

On top of this the continued device scaling demands higher resolution. The resolution in an optical system is limited by the wavelength of the light source which drives the industry to using shorter and shorter wavelengths. The next wavelength that is considered after 193 nm is 13.5 nm which is in the extreme ultraviolet (EUV) part of the spectrum [14]. Since the micromirror works by diffraction the maximum deflection across a tilting mirror is limited to only half a wavelength, which is a fact that is helpful. However, the diffractive operation also sets tough requirements on the micromirror planarity. The currently used mirrors in the Sigma7500 require a planarity of a few nanometers peak-to-valley [6]. This requirement is at a wavelength of 248 nm and translated to EUV the planarity needs to be almost a factor 20 better i.e. mere fractions of a nanometer. At EUV wavelengths there are no transparent materials and all optics including the SLM need to be reflective with Mo/Si multilayer coatings to enhance the reflectivity [15]. These multilayers also deform the

Table 2.1 Required number of mirrors for different technology-nodes in order to meet a throughput of 5 WPH with a flash frequency of 10 kHz.

<table>
<thead>
<tr>
<th>Technology-node (nm)</th>
<th>65</th>
<th>45</th>
<th>32</th>
<th>22</th>
<th>16</th>
</tr>
</thead>
<tbody>
<tr>
<td>node pixels (mm^2)</td>
<td>0.24x10^9</td>
<td>0.49x10^9</td>
<td>0.98x10^9</td>
<td>2.1x10^9</td>
<td>3.9x10^9</td>
</tr>
<tr>
<td>required number of mirrors</td>
<td>2.3x10^6</td>
<td>4.8x10^6</td>
<td>9.6x10^6</td>
<td>20.3x10^6</td>
<td>38.3x10^6</td>
</tr>
</tbody>
</table>
mirrors due to residual stress in the deposited stack. In order to meet the planarity requirements obviously a mechanically very stable mirror is required.

## 2.2 The hidden hinge monocrystalline silicon micromirror

The mirror structure investigated in this thesis was first presented in Paper A and is intended as a mechanically stable platform able to meet the increased requirements in future optical maskless lithography systems including systems using EUV radiation. An illustration of the structure can be seen in Figure 2.1a. The structure consists of one or more standing flexure hinges which are hidden beneath the optically active surface. The thickness of the material forming the optically active surface can be defined independently of the stiffness of the hidden hinge. Comparing this structure with a typical torsion mirror as shown in Figure 2.1b, which is the currently used mirror in the Sigma7500, there are obvious differences even though the application is the same. So what are the benefits of using this new design? This will be made clear in the following sections of this chapter where these two mirrors are compared.

The device which will be compared to the hidden hinge mirror is a monocrystalline silicon torsion mirror designed for 193 nm DUV wavelengths [16]. The dimensions of the compared mirrors are summarized in Table 2.2 where the dimensions of the hidden hinge mirror have been chosen so that the angular spring constant, $k_\theta$, is the same for both mirrors ($k_\theta=0.3 \text{ nNm}$). A case study for EUV mirrors based on the hidden hinge mirror is presented in Paper A. An expanded discussion of this EUV case study is given in parallel to the DUV mirror comparison.

As pointed out in the heading of this section the material used in the hidden hinge mirrors is monocrystalline silicon. This is a material that recently has attracted attention as a good material for micromirrors [16-19] because of its near ideal mechanical properties [20]. More about the mirror material is given in section 3.1 when presenting the fabrication of the hidden hinge mirrors.
2.3 Electrostatic actuation

Electrostatic actuation is not commonly used when dealing with macro scale objects. But in MEMS it is frequently employed since electrostatic forces scale favorably when miniaturized, is relatively easy to implement, and provide a fast actuation method. For devices with millions of individually addressable elements it is also a big advantage to use electrostatic actuation since it is possible to use the mature complementary metal oxide semiconductor (CMOS) technology to provide the addressing circuitry. The CMOS chip will limit the available actuation voltage but as mentioned in section 1.1 the mirrors work by diffraction and require only small deflections. This small stroke makes it possible to use a small electrode gap which greatly increases the magnitude of the electrostatic force since the force is inversely proportional to the square of the electrode gap. This inversely quadratic dependence in combination with linear springs can however make the structure unstable. If the deflection becomes larger than one third of the electrode gap the mirrors will be pulled in fully and make contact with the electrode. This makes it imperative to have electrode gaps larger than 3 times the maximum required deflection.

The analysis of the electrostatic actuation for the hidden hinge micromirror is given in Paper A. Figure 2.2 (a) shows the numerically simulated deflection for the hidden hinge mirror in Table 2.2. A curve which approximates the deflection of the torsion mirror [7] is also plotted in Figure 2.2 (a). It is clear that there is a good agreement between the two curves. From Figure 2.2 (b) which shows the difference in deflection between the two curves it is evident that the agreement is better than ±1 nm. The same type of plot can be done for the EUV mirrors in Paper A and the agreement for those curves is better than ±0.05 nm. This small discrepancy is not surprising since the described movements of the

Table 2.2 Dimensions and material parameters for the compared mirrors. The capital letters in brackets for the hidden hinge mirror correspond to the nomenclature used in Paper A.

<table>
<thead>
<tr>
<th>Torsion mirror [16]</th>
<th>Hidden hinge mirror</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mirror and hinge thickness (nm)</td>
<td>300</td>
</tr>
<tr>
<td>Hinge width (nm)</td>
<td>700</td>
</tr>
<tr>
<td>Hinge length (μm)</td>
<td>2.0</td>
</tr>
<tr>
<td>Mirror size (μm)</td>
<td>16×16</td>
</tr>
<tr>
<td>Young's modulus (MPa)</td>
<td>165</td>
</tr>
<tr>
<td>Poisson's ratio</td>
<td>0.3</td>
</tr>
<tr>
<td>Density (kg/m³)</td>
<td>2329</td>
</tr>
<tr>
<td>Young's modulus (MPa)</td>
<td>165</td>
</tr>
<tr>
<td>Density (kg/m³)</td>
<td>2329</td>
</tr>
</tbody>
</table>
electrodes are almost identical in both cases and both mirrors have linear springs. However, what does differ is the mechanical analysis of the structure.

For the torsion mirror $k_\theta$ can be calculated from [21]

$$
k_\theta = 2ab^3\left[\frac{16}{3} - 3.36\frac{b}{a^3}\left(1 - \frac{b^4}{12a^4}\right)\right]\frac{G}{L},
$$

(2.1)

where $G$ is the modulus of rigidity and $a$, $b$, and $L$ is half the width, half the thickness, and the length of the torsion hinge. For the hidden hinge the analysis is a little more complicated due to the rounded shape of the hinge and a numerical method to calculate $k_\theta$ is given in Paper A. This method seems to be fairly accurate when compared to finite element method (FEM) calculations. For the hidden hinge being compared here the numerical method gives an error of less than 0.3 % compared to the FEM value. For the two hinges in the case study in Paper A the error is larger but still below 7%. Part of the explanation for this larger error could be due to the low aspect ratio of the hinges in the case study as discussed in Paper A.

The standing flexure hinge has a very different response to the electrostatic force compared to the torsion hinge. The torsion hinge will not only twist but also deflect perpendicular to the optically active surface which is not desirable. The movement perpendicular to the optically active surface for the standing flexure hinge on the other hand is more determined by the geometry of the structure than by the stiffness of the hinge. This is discussed in further detail in connection to sagging in section 2.5. Another substantially different response to an applied electrostatic force is the deformation of the optically active surface. This is treated in the following section.
Mirror surface deformation

Ideally the optically active surface should be completely stiff since deformations could influence the lithographic performance of the mirror. However, for the typical torsion mirror the actuation is accompanied by a more or less unavoidable deformation of the optically active surface. This originates from the design of the mirrors where the optically active surface and the torsion hinges are defined in the same layer. This is not the case for the hidden hinge mirror where the hinge and the optically active surface are separated.

For the torsion mirror the deformation of the mirror surface during actuation is extracted by 3D finite element analysis (FEA), see Appendix A for details. The maximum deviation from an ideally stiff mirror, $\delta_{\text{def}} - \delta_{\text{stiff}}$, as illustrated in Figure 2.3, is close to 6 nm.

The mechanical analysis of the deformation of the hidden hinge mirror during actuation is carried out in Paper A. Using equation (21) from Paper A the maximum deviation from an ideally stiff mirror is around 0.3 nm. The stiffness of the mirror surface can be tailored independently of the dimensions of the hinge. Figure 2.4 shows the maximum mirror deformation during actuation as a function of the mirror thickness. A maximum deformation of 1 nm is achieved for a thickness of around 500 nm and an order of magnitude smaller deformation of 0.1 nm can be achieved for a thickness around 1000 nm.

For the two EUV cases in Paper A the deformation is on the order of picometers. This can be compared to the deformation for an isometrically scaled torsion mirror with the same mirror area. The same deformation for the scaled torsion mirror is close to 0.5 nm which is more than 2 orders of magnitudes larger than for the hidden hinge mirror.

The mirror surface could also be deformed from residual stress in a reflectivity increasing coating. For EUV wavelengths it is necessary to use such a coating and the common approach is to use a molybdenum and silicon multilayer stack [15]. A typical value for the Mo/Si period thickness is 7 nm and the total stack usually consists of around 50 periods resulting in a total stack thickness of 350 nm. Values for the residual stress in such stacks are typically around -400 MPa [22]. The modified Stoney’s equation [23] describes the cur-
 curvature of a substrate of uniform thickness due to a film of uniform thickness with uniform residual stress. This can be used to estimate the deformation of the mirror and the equation for the radius of curvature is

$$\frac{1}{R} = \frac{\sigma_f (1-\nu_f)}{t_s E_f} \frac{6mn(1+n)}{1+4mn+6mn^2+4mn^3+m^2n^4}, \quad (2.2)$$

where $R$ is the resulting radius of curvature, $\sigma_f$ is the residual stress in the film, $\nu_f$ is the Poisson’s ratio for the film, $t_s$ is the thickness of the substrate, $E_f$ is the modulus of elasticity of the film, $m$ is the ratio of the film’s biaxial modulus ($E'=E/(1-\nu)$) over the substrate’s, and $n$ is the ratio of the film’s thickness over the substrate’s.

Figure 2.5 shows the peak-to-valley deformation as a function of substrate thickness for the modified Stoney’s equation and the EUV case study mirrors in Paper A. The material properties for the film and the substrate were set to be identical, hence $m=1$, $E_f=165$ GPa, and $\nu_f=0.3$ while $t_f=350$ nm and $\sigma_f=-400$ MPa. As can be seen the deformation is on the order of nanometers which is unacceptable for the EUV application. A way of alleviating the requirements on deformations caused by uniform residual stress is to introduce a phase step in the mirror surface [6]. It will reduce the deformation requirements but at the same time doubles the required dose. For example this means that at the same intensity the pattern needs to be exposed for twice as long time which may lower the throughput.

If a phase step is not used the peak-to-valley deformation needs to be decreased by more than a factor of 10. This could be accomplished by simply increasing the thickness of the mirror. In order to reach a deformation of less than 0.2 nm the thickness should be larger than 4 $\mu$m. Another approach to lower the deformation could be to reduce the residual stress of the Mo/Si stack.
Experiments where multilayer stacks have been annealed at temperatures below 400 °C show that the residual stress can be lowered by more than a factor of 10 [24]. Using either approach (or a combination of them) makes it possible to design the hidden hinge mirror to meet EUV requirements.

### 2.5 Sagging

The sagging of the mirror as seen by the optical system is the average movement of the optically active surface in the direction perpendicular to the surface. As mentioned in section 2.3 the torsion mirror and the hidden hinge mirror behave very differently in this aspect. The sagging of the torsion mirror is determined by the stiffness of the structure and can be estimated by integrating the deflection over the mirror surface and dividing by the surface area. Carrying out this integration in the 3D FEA of the DUV torsion mirror the sagging is calculated to 3.5 nm, see Appendix A for details.

The sagging for the hidden hinge mirror is also determined by the deformation of the mirror surface but there is also a geometric contribution. This geometric sagging comes from that the rotational axis of the hidden hinge does not lie in the plane of the mirror surface. The analysis of the geometric sagging is given in Paper A and it becomes more important the thicker the mirror is and the larger the angular displacement is. For the DUV mirror the total sagging is 0.1 nm and 33% of this is due to the geometrical sagging. For the EUV mirrors in the Paper A case study the sagging is around 10 pm and more than 94% of this is due to the geometric sagging. Figure 2.6 shows the influence of the mirror deformation and geometric sagging on the total sagging for the hidden

![Figure 2.5 The influence of the substrate thickness on the peak-to-valley deformation due to a residual stress of -400 MPa in a 350 nm thick film.](image-url)
hinge DUV mirror. The FEA sagging goes asymptotically to the geometric sagging for thicker mirrors because the contribution from the mirror deformation becomes negligible.

Another unique concern for the standing flexure hinge is buckling. A slender beam subject to compressive load may become elastically unstable and buckle if the load exceeds a critical value. For a clamped-free beam the critical load, $P_c$, above which the beam becomes unstable is given by [21]

$$
P_c = \frac{\pi^2 EI}{4H^2},
$$

where $E$ is the modulus of elasticity, $I$ is the moment of inertia of the cross section area of the hinge, and $H$ is the height of the hinge. For both the DUV mirror and the EUV cases in Paper A it turns out that the hinge is rigid enough to avoid buckling. $P_c$ is more than 4 orders of magnitude larger than the electrostatic force required to deflect the mirror. For the considered forces and dimensions the aspect ratio of the hinge is clearly low enough for buckling to not become an issue.

### 2.6 Electrode misalignment

During the fabrication of the micromirrors a misalignment between the actuation electrodes may occur. If the misalignment is large it could decrease the overlapping electrode area which would result in an increase in the voltage required to achieve a certain deflection. Owing to the different fabrication method for the torsion mirrors this misalignment can be kept small enough not
to significantly affect the actuation characteristics. For the hidden hinge mirrors though the misalignment can be larger and needs to be considered.

The influence of a decrease in overlapping electrode area was incorporated in the analysis of the electrostatic actuation in Paper A. The highest alignment accuracy currently achieved for the relevant fabrication step is better than ±200 nm [25]. For the DUV mirror a misalignment of this magnitude results in a decrease of overlapping electrode area by 5% which increases the maximum required voltage by 7% from 15 V to 16 V as shown in Figure 2.7. This is a relatively low shift and it should be tolerable.

For the EUV mirrors in Paper A a misalignment of ±200 nm results in a decrease of overlapping electrode area by 40% which increases the maximum required voltage by around 35% for both cases. This is a significant shift and definitely needs to be considered. Nevertheless the maximum required voltage is still less than 3 V for EUV mirrors which should be feasible for CMOS.

Another parameter that is strongly influenced by the electrode misalignment is the unwanted actuation known as crosstalk that occurs between adjacent mirrors. For a perfect alignment the crosstalk is negligible but when the misalignment is close to or larger than the distance separating the mirrors the crosstalk can be significant. For the DUV mirror the distance separating the mirrors will be much larger than 200 nm and the crosstalk is negligible. For the case study in Paper A the crosstalk is less than 0.5% of the deflection of the actuated mirror as long as the mirrors are separated by a distance that is larger than 215 nm.

Both the change in overlapping electrode area and the crosstalk set constraints on the parameter window that can be used when designing the hidden

![Figure 2.7 The influence of a 200 nm misalignment between the actuation electrodes for the DUV hidden hinge mirror.](image)
hinge mirror. However, there may be ways of alleviating these constraints. Such an approach is discussed in more detail in section 3.6.2.

2.7 Dynamics

As pointed out in section 2.1 the SLM needs to be loaded with new data at a high speed. At laser flash frequencies of several kHz the data needs to be loaded within tens of microseconds. This means that the eigenfrequency of the mirrors needs to be high enough to allow the mirrors to deflect to a distinct position within the same amount of time. Owing to the low mass of the torsion mirrors the eigenfrequency is very high. For the DUV torsion mirror in this comparison it is greater than 1 MHz which is more than enough for the considered laser flash frequency. The relatively bulky design of the hidden hinge mirrors on the other hand will increase the inertia of the mirror which could be a potential problem.

The undamped eigenfrequency, $f_e$, of the hidden hinge mirror can be calculated by

$$f_e = \frac{1}{2\pi} \sqrt{\frac{k_\theta}{I_0}},$$

where $k_\theta$ is the angular spring constant and $I_0$ is the moment of inertia with respect to the rotational axis of the mirror. The curves in Figure 2.8 are calculated for the DUV mirror (a) and the case study mirrors in Paper A (b) using the numerically estimated angular spring constant, $k_{\theta,DUV}=0.3$ nNm, $k_{\theta,case1}=1.4$ pNm, and $k_{\theta,case2}=4.0$ pNm. $I_0$ is estimated assuming a rotational axis through the center of the hinge and some geometrical simplifications as presented in

Figure 2.8 Undamped eigenfrequency for the DUV hidden hinge mirror (a) and the two EUV mirror cases in Paper A (b) as a function of the minimum thickness of the optically active surface.
more detail in Appendix B. Values of the eigenfrequency from FEA agree with the analytically estimated values and are also plotted in Figure 2.8. Despite the increased mass of the hidden hinge mirrors the eigenfrequency is around 0.5 MHz for the DUV mirror and several MHz for the EUV mirror and this should be more than adequate for the intended application.

Another parameter that determines how fast the mirrors can reach a stable deflection is the damping of the system. DUV mirrors are typically actuated in an nitrogen ambient [26] at atmospheric pressure which gives access to strong enough damping through squeeze film damping. This type of damping will not be available in an EUV system since the lithographic chamber needs to be evacuated due to the severe attenuation of EUV radiation at high pressures. Alternative forms of damping for EUV mirrors relying on resistive damping have recently been presented [9]. Simulations show that this type of damping can be designed to allow sufficient damping for the intended operating speeds [9].
Chapter 3

Fabrication and characterization of micromirrors

This chapter deals with the challenges and opportunities related to the fabrication of the hidden hinge monocrystalline silicon micromirrors presented in Chapter 2. The fabrication of the mirrors is based on low temperature transfer bonding and a number of relevant transfer methods are compared in section 3.2. A process to fabricate the mirrors is presented in section 3.3 and sections 3.4 and 3.6 discuss in more detail the formation of the hidden hinges and the bonding which are two of the more critical process steps. Section 3.5 presents a measurement method developed to characterize the bond strength with a spatial resolution on the order of micrometers. The characterization of micromirrors fabricated with the presented process is discussed in section 3.7.

3.1 Introduction

The general approach when fabricating large arrays of micromirrors is surface micromachining of the mirrors on top of CMOS addressing electronics [8,27-31]. Due to high reflectivity and ease of use it has been very common to use aluminum as the material for the mirrors. However, deposited aluminum is known for mechanical memory effects [32,33] which limits the precision and lifetime of these mirrors. This has led to the search for mechanically more sta-
ble materials. SiGe [27], polycrystalline silicon [28], and different aluminum alloys [29,31] have been used to increase the performance of the mirrors.

Due to the near ideal mechanical properties of monocrystalline silicon it has recently attracted attention as a very promising candidate to further improve the performance. It is however not straightforward to integrate monocrystalline silicon into the process plan. All the previously mentioned materials can be deposited on top of the addressing electronics but this is not the case for monocrystalline silicon. Nevertheless much effort has recently been put into the area of integration and excellent performance of monocrystalline silicon micromirrors has been reported [16-19].

Another parameter to consider is of course reflectivity. Monocrystalline silicon actually has a rather high reflectivity for deep ultraviolet (DUV) wavelengths and for some applications it is not even necessary to have a reflective coating [16]. For EUV wavelengths on the other hand, as mentioned in Chapter 2, a rather thick (around 350 nm) reflective coating is needed in the form of a Mo/Si distributed Bragg reflector (DBR) [15]. To match the tough requirements on planarity, also discussed in Chapter 2, the surface of the DBR needs to be extremely smooth. A too high surface roughness of the DBR will also lower the reflectivity. Fortunately the deposition methods used for the multilayer stack has a substrate smoothing effect and root-mean-square (rms) values below 0.1 nm have been demonstrated for Mo/Si multilayers on monocrystalline silicon [15].

The hidden hinge monocrystalline silicon mirror combines the material benefits of using monocrystalline silicon [16,18] with the design benefits, as discussed in Chapter 2, of having the optically active surface on a different level than the hinges [29]. Hence, enabling the stiffness of the hinge to be independent of the mirror stiffness which makes it possible to design a very stable mirror platform e.g. for the DBR required in EUV applications. The fabrication of the hidden hinge monocrystalline silicon mirror is made possible by the use of low temperature transfer bonding.

3.2 Low temperature transfer bonding methods

Transfer bonding is a technique that enables the integration of devices, e.g. ICs and transducers, fabricated using processes and/or designs that are not compatible with each other as well as double sided micromachining of thin films. For the hidden hinge mirrors the actual mirror structure would in principle be impossible to realize in monocrystalline silicon without the use of transfer bonding. A common limiting factor when choosing transfer method is the thermal budget, especially for ICs. The definition of low temperature of course depends on the application but when dealing with transfer bonding the limit is
usually around 450 °C for the process to be regarded as low temperature [34]. This originates from limits caused by the metal layers in ICs built using CMOS technology, which is the dominating technology used for ICs.

Since the actuation of the micromirrors relies on CMOS addressing electronics it is crucial that the transfer method is CMOS compatible. Apart from the CMOS compatibility the transfer method should also be able to transfer features with bond areas on the order of 1 μm² with an alignment accuracy better than ±200 nm. It is also important to minimize the residual stress and topography introduced during transfer since this causes initial deformation and deflection of the finished mirrors.

### 3.2.1 Intermediate layer transfer bonding

Common for these methods is the need of one or more intermediate layers to promote the bonding. The intermediate layer is typically a polymeric-, ceramic-, or metallic-material.

**Adhesive bonding**

In adhesive bonding the intermediate layer can be either organic or inorganic. Typically the adhesive layer is deposited, e.g. by spin coating or spraying, on one or both wafers to be bonded. The wafers are aligned, brought in contact, and the layer is cured by applying heat and pressure.

Using adhesive bonding with epoxies to transfer circuits has been reported to affect the characteristics of CMOS circuits [35], e.g. leakage currents and threshold voltages. The reason for this was reported to be residual stress, induced by the circuit transfer which put further emphasis on the importance of low residual stress.

Adhesive transfer bonding has been used for fabrication of large arrays of monocrystalline torsion micromirrors [16]. Polymethylglutarimide (PMGI) was used to transfer the device layer of a silicon on insulator (SOI) wafer on to addressing electronics with very promising results. However, the adhesive was also used as a sacrificial layer and hence removed during the release of the mirrors.

Not many authors give values for the minimum sizes of the transferred structures. One of few reports mention transferred feature sizes down to 1.5 μm using benzocyclobutene (BCB) as the adhesive layer [36].

*Advantages* [37,38]:

- Strong bonding for in principle all material combinations possible.
- Not extremely sensitive for particle contamination, surface cleanliness and interface topography.
Reported transfer of small features.

Disadvantages [37,38]:
- Alignment accuracy decreased due to shear forces caused by bond tool during curing of the intermediate adhesive layer. However, schemes to circumvent this have been presented [39,40].
- Thermal mismatch during curing decrease overall alignment accuracy.
- Detrimental effects on transferred CMOS circuits have been reported [35].

Metallic bonding

Metallic bonding includes solder, eutectic and thermo-compression bonding. In solder bonding a metal or metal-alloy is usually deposited on both wafers and heated to the melting temperature of the solder. Solder bonding is widely used in flip-chip bonding and flip-chip techniques using solder bumps with a diameter of around 25 μm have been reported [41].

Eutectic bonding is very similar to solder bonding but the metal layer and wafer creates an alloy with lower melting temperature than the pure materials. Most common is gold and silicon with an eutectic temperature of 363 °C. The eutectic bonding introduces mechanical stresses that degrade circuit performance [42].

Thermo-compression uses elevated temperature and high pressure to bring the two surfaces into intimate contact. This technique has recently attracted attention for 3D stacked ICs using Cu-Cu bonding to form vias between the stacked circuits [34]. The pitch of the vias is tens of micrometers and the required pressure is ~1 MPa. The load required to achieve such a pressure over a large area, e.g. at wafer scale, decreases the alignment accuracy. Shifts in alignment accuracy of around 1 μm have been reported [43].

Advantages:
- Possible to join a large variety of materials especially for solder and thermo-compression bonding.
- Solder bonding is not very sensitive to particle contamination.

Disadvantages:
- Complete eutectic bonding of large areas is hard to achieve due to the presence of native oxides.
- The required high pressure limits the total bondable area in order to maintain alignment accuracy in thermo-compression bonding.
3.2.2 Direct transfer bonding

Common for these methods is the lack of any intermediate layer. Bonding of the substrates can be spontaneous or may require pressure or an applied voltage.

Anodic bonding

Anodic bonding is also known as field assisted bonding or electrostatic bonding. Typically anodic bonding is performed between an alkali containing glass and a silicon wafer at 300-450 °C and an applied voltage of 200-1000 V over the substrates. However, using intermediate layers to anodically bond wafers have also been reported [44-46]. Anodic bonding has been used in the so-called “dissolved wafer process” to transfer p++ boron doped silicon to a patterned glass substrate with Pt-electrodes [47]. It is reported that the size of the bondable area is determined by the residual stresses caused by thermal mismatch between glass substrate and silicon but no values are given. Anodic bonding has also been used to merge a 3 μm CMOS process with a dissolved wafer process to fabricate monolithic integrated pressure sensors [48]. The influence of the anodic bonding step on the CMOS devices were characterized by measuring the shift in threshold voltage and it was found that the overall shift was within tolerable limits for all analog circuits. However, the shielding of the CMOS circuits during anodic bonding has also been reported to be inadequate [49].

Advantages:

- High mechanical and chemical stability.

Disadvantages [50]:

- Residual stresses after bonding.
- High electric fields applied during bonding can damage electronic devices or create electrostatic forces causing unwanted bonding of free hanging structures.
- High alkali content can cause changes of electrical properties for adjacent materials.
Plasma assisted direct bonding

Plasma assisted direct bonding is a development of fusion bonding. Just as for fusion bonding there are stringent requirements on surface roughness and cleanliness in order to achieve a high quality bond. But in contrary to fusion bonding there is no need for high temperature annealing since plasma activation of the surfaces before bonding increases the bond strength [38,51-53]. Plasma assisted bonding has been used for several material combinations using different plasmas [54]. The most commonly used method though is to use an oxygen-plasma activation which creates hydrophilic surfaces. This is suitable for bonding silicon to either silicon or silicon oxide. An infrared (IR) transmission image of a pair of oxygen plasma bonded silicon wafers can be seen in Figure 3.1. The unbonded areas around the edges probably originate from careless handling, e.g. grabbing with tweezers. The small circular unbonded areas are due to particles and really emphasis the importance of cleanliness.

A transfer process using both oxygen as well as argon plasma assisted bonding has been reported [55]. Annealing temperatures up to 450 °C are used to increase the bond strength. To achieve a proper bond for the presented process the recommended minimum feature width is 100 μm. The suggested explanation is that gas formation during bonding prevents the bonding of smaller features. It is not explicitly mentioned but the test is probably performed without venting channels. In the appended papers oxygen plasma assisted bonding has been used in Si-Si and SiO₂-SiO₂ transfer processes with both wet and dry etchback. Features with aspect ratios of more than 30 as well as bonded areas of less than 1 μm² have been successfully fabricated. No tendency for smaller

Figure 3.1 IR transmission image of structured oxygen plasma assisted bonded wafer using the transfer process in Paper D.
areas to create a weaker bond has been observed when measuring the fracture toughness utilizing the method presented in Paper D. The explanation for the discrepancy between the reported minimum feature sizes is probably the use of venting channels and the lack of high temperature annealing steps in the appended papers.

The CMOS compatibility of oxygen plasma assisted wafer bonding has been investigated [38,53,56,57]. Given that the CMOS circuit is passivated, e.g. by silicon nitride, prior to the bonding step the oxygen plasma has no effect on the performance of the circuit. This condition may not be fulfilled when transferring the mirrors but the use of oxygen plasma treatment of large arrays of micromirrors on top of CMOS circuits has been reported before [16,31].

Advantages:
- High bond strengths possible for room temperature processes [51].
- Transfer of high aspect ratio and very small features possible.
- No intermediate layer adding topography and interfacial stress.

Disadvantages:
- The oxygen plasma could potentially damage exposed metal layers [50].
- High requirements on particle contamination, wafer bow and cleanliness to achieve high quality bonds.

3.2.3 Discussion & comparison of transfer methods

All the presented transfer methods are more or less CMOS compatible even though some have been shown to have detrimental effects on circuits. The transfer of micrometer sized features has only been shown for adhesive and plasma assisted bonding even though other methods could very well be suitable. However, minimizing the interfacial stress and topography differences introduced during transfer promotes the use of direct transfer methods since interfacial layer transfer methods inherently introduce stresses in the interface as well as uncertainties in topography. Even though adhesive bonding has successfully been used during the fabrication of large arrays of torsion micromirrors it is not part of the finished device and this is probably not a feasible approach for the presented micromirror. From this discussion the best candidate should be plasma assisted direct bonding which has also been used to fabricate working hidden hinge monocrystalline silicon micromirrors in Paper B. In the appended papers there are several more examples of structures and devices fabricated by using oxygen plasma assisted transfer bonding. The next section summarizes these structures and their fabrication.
3.2.4 Utilization of oxygen plasma assisted transfer bonding

In the appended papers transfer processes utilizing oxygen plasma assisted bonding is used to fabricate several different electrostatically actuated devices, see Figure 3.2, as well as the test structures for the measurement method presented in Paper D, see Figure 3.3. Both dry and wet etchback has been implemented using SF₆-plasma and tetramethylammonium-hydroxide (TMAH). When using wet etchback the structures need to be passivated. In Paper F this is achieved by thermally oxidizing the donor wafer prior to bonding, see Figure 3.2. For dry etchback the passivation can be implemented in the etch process using the Bosch process. However, creating a uniform etch rate when dry etching a 100% open wafer is in principle impossible. So if an etch stop layer like the buried oxide in an SOI wafer is not used the wafer needs to be diced before the etchback is completed to obtain a more uniform result. If a dicing step is needed to achieve a uniform etchback the dicing blade needs to be aligned to the patterned wafers. In Paper D the dicing blade was aligned to the revealed pattern at the edges of the wafer since the etch rate is highest at the periphery. The chips were then glued on a carrier wafer and the etchback was continued.

Demonstrators for the process in Paper F are in the form of a pinball game and a wobble motor and can be seen in Figure 3.2g and Figure 3.2h respectively.

![Figure 3.2 Illustration showing process flow cross sections for the demonstrator fabrication in Paper F.](image)

- (a) Oxidized and patterned wafer.
- (b) Dry etched wafer.
- (c) Oxidized structured wafer.
- (d) Room temperature oxygen plasma bonded structured wafer.
- (e) Wafer after etchback.
- (f) Wafer after wet etch of the intermediate sacrificial oxide layer.
- (g) Photograph of a micro pinball game and (h) a wobble motor fabricated using the transfer process to the left.
tively. A pillar on a chip ready for mounting in the sample holder from Paper D can be seen in Figure 3.4.

### 3.3 Hidden hinge mirror transfer process

For the hidden hinge mirror transfer process the mirrors are fabricated on the donor wafer and transferred by low temperature oxygen plasma assisted bonding to the addressing electrode target wafer. The process consists of three distinct parts which are described in this section; the fabrication of the mirrors (donor wafer), the fabrication of the addressing electrodes (target wafer), and the transfer of the mirrors to the electrodes.

![Diagram of process flow cross sections for the pillars fabrication in Paper D.](image)

**Figure 3.3** Illustration of process flow cross sections for the pillars fabrication in Paper D. (a) Patterned and dry etched chevron (b) Patterned pillar (c) Dry etched pillar (d) Cleaned wafer (e) Bonding step (f) Bonded wafers (g) Wafer after etchback.

![SEM image of a typical bonded pillar and its bond interface](image)

**Figure 3.4** SEM image of a typical bonded pillar and its bond interface fabricated using the transfer process in Paper D.
3.3.1 Mirror wafer

Figure 3.5 shows the process flow for the mirror wafer process used in Paper B. The starting material for this process is a 150 mm SOI wafer with a 15 μm thick p-type device layer, a 600 nm thick buried oxide (BOX), and a 380 μm thick handle wafer. A 50 nm dry silicon oxide is grown to protect the bond surface during continued processing and an 80 nm thick aluminum layer is deposited. The mirror pitch is patterned in the aluminum and in the silicon oxide by standard contact photolithography and wet etch and reactive ion etching (RIE) respectively, Figure 3.5a.

The subsequent deep RIE (DRIE) defines the individual mirrors in the device layer, Figure 3.5b. The BOX is used as an etch stop layer and to avoid notching at the Si-SiO₂ interface the SOI option of the DRIE machine is used. Figure 3.5b also shows a planarization performed by low pressure chemical

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Figure 3.5 Process flow for the mirror wafer. a) mirror pitch definition by wet etch and RIE b) DRIE down to the BOX and planarization by TEOS deposition c) hinge definition in thermal oxide d) shallow DRIE and PECVD silicon oxide passivation e) RIE to remove silicon oxide at trench bottom f) isotropic silicon etch to create hidden hinge g) BOE revealing silicon bond surfaces.
vapor deposition (LPCVD) of an 800 nm thick silicon oxide film using tetra-ethoxy-silane (TEOS). This planarization step is necessary to ensure good results in the next lithography step and to passivate the etched trenches. Figure 3.6 shows a cross section of a 4×4 mirror array after TEOS planarization. So called key-holes are visible in the trenches. Key-holes are cavities that are formed during the deposition due to a slightly higher deposition rate at the trench openings which closes the trench at the top. This does not cause any problem for the continued processing of the mirror wafer.

Next the bond surfaces and electrodes are defined on each individual mirror element by standard contact photolithography and RIE, Figure 3.5c. A DRIE defines at what depth the hinge will be placed, in this case 3 μm, Figure 3.5d. A 250 nm thick layer of plasma enhanced CVD (PECVD) silicon oxide inside the shallow trench is used to passivate the trench during the coming isotropic hinge etch.

The PECVD silicon oxide layer is removed at the bottom of the shallow trench using a CF4 RIE, Figure 3.5e. The hidden standing flexure hinge is defined by an isotropic SF6 etch, Figure 3.5f. This process is similar to the single crystal silicon reactive etch and metal (SCREAM) process [58] except that a thin silicon hinge is left between the trenches. The initial thermal oxide and the TEOS is stripped in buffered oxide etch (BOE) revealing the silicon bond surface and the mirrors are ready for transfer to the addressing electrodes, Figure 3.5g.

### 3.3.2 Electrode wafer

An illustration of the process flow for the electrode wafer as fabricated in Paper B can be seen in Figure 3.7. The starting material is a 150 mm, 500 μm thick p-type silicon wafer. All bond surfaces are protected with resist, Figure 3.7a, and to create the electrode gap, recesses are isotropically dry etched into the silicon using SF6 to a depth of 700 nm, Figure 3.7b.
A 100 nm thick dry oxide is grown to electrically insulate the substrate from the electrodes and protect the bond surfaces during the following process steps, Figure 3.7c. Next a 100 nm thick aluminum oxide layer is evaporated to act as an etch stop during the vapor HF-etching mirror release step, Figure 3.7d.

In Figure 3.7e 150 nm thick gold electrodes are formed by lift-off and protected with negative resist using the same photomask as in Figure 3.7a. Aluminum oxide etches in BOE and in the first batch BOE was used to remove both the aluminum oxide and the silicon oxide at the exposed areas. This resulted in a catastrophic underetch destroying most of the electrodes. An alternative process was found where the wafer is coated with a 50 nm PECVD silicon oxide prior to the lithography in Figure 3.7e. The thin PECVD silicon oxide is removed in a CF$_4$ RIE and the exposed aluminum oxide is removed by wet
etching in aluminum wet etch (\(H_3PO_4:HN0_3:CH_3COOH:H_2O\) proportions 16:1:1:2) at 40 °C. To reveal the bond areas the last silicon oxide is removed in BOE, Figure 3.7f. After stripping the resist the electrode wafer is ready for bonding, Figure 3.7g. A photograph of a wafer ready for bonding can be seen in Figure 3.8.

3.3.3 Bonding

The mirrors are now transferred to the electrode wafer using aligned low temperature oxygen plasma assisted wafer bonding. Both wafers are oxygen plasma treated [52], dipped in clean water, and spin dried. Aligned bonding using through-wafer holes is performed in a Karl Süss BA6 as described in Paper E. To make the mirror process more readable the through wafer holes are not illustrated in Figure 3.9 but the implementation of the method is straightforward and is presented in section 3.6. The wafers are then brought to a Karl Süss SB6 bond chamber. The chamber is evacuated and the top tool press the two wafers together with a pressure of 2 Bar, Figure 3.9a.

The bonded wafer stack is diced and the SOI handle wafer is removed by isotropic dry etching, Figure 3.9b. The BOX of the SOI wafer is used as an etch stop during the etchback. A highly smooth mirror surface and stiction free release can be achieved by using vapor HF-etching [59] Figure 3.9c.

![Figure 3.9 Process flow for the bonding process. a) oxygen plasma surface activation on both wafers and aligned bonding b) silicon etch to remove handle wafer c) release of mirrors by vapor HF etch.](image-url)
During the spin drying of the mirror wafer prior to bonding the key-holes from the TEOS planarization can become a problem. The TEOS is not only used for planarization but also fixes the silicon around the hinge so that the hinge cannot move. The key-holes could act as channels allowing the BOE in Figure 3.5g to penetrate into the trench and releasing the hinge. If this occurs the fragile hinge could be fractured during the continued processing, e.g. spin drying of the wafer. Indeed this has sometimes been observed for very small hinges after spin drying where silicon debris originating from the intended bond part of the mirror has been spread over the wafer. This does not only destroy the mirrors that have lost the bond area but also prevent successful bonding in a larger area wherever the silicon debris lands. A significant reduction in silicon debris on the wafer can be achieved if the wafer is spin dried with the bond side facing downward. Figure 3.11 shows two IR photographs of the influence of silicon debris on bond results. The left image shows very few bonded areas and is from a wafer that had clear signs of silicon debris prior to bonding. The right image on the other hand shows very few voids and is from a wafer without silicon debris.

Figure 3.11 IR photographs of bonded wafers with silicon debris prior to bonding (a) and wafer without silicon debris (b).

Figure 3.10 SEM image of a 16x16 μm pitch mirror with isotropically etched hinge and a close up showing the result from the isotropic hinge etch. The tunnels under the bond surface are clearly visible.
3.4 Formation of hidden standing flexure hinges

The formation of the hidden hinge is a critical step in the fabrication of the micromirrors. Here follows a presentation of two different bulk micromachining methods to produce a hidden standing flexure hinge in monocrystalline silicon. The first one is by isotropic etching as presented in Paper B and the other is by local oxidation of silicon (LOCOS) as presented in Paper C.

3.4.1 By isotropic etching

The process leading up to the isotropic hinge definition etch is illustrated in Figure 3.5a through Figure 3.5e. Figure 3.10 shows a 16x16 μm large mirror after the isotropic etch and a detailed view of the resulting hinge. Openings in the bond surface of the mirror have been used to design a total depth of the

![Figure 3.12](image-url)
hinge which is different from the depth of the mirror. The isotropic etch progress to achieve this is illustrated in Figure 3.12. The openings in the bond surface appear as circles in Figure 3.12b; they will allow the isotropic etch to create a tunnel under the bond surface, Figure 3.12d. This reduces the total depth of the hidden hinge and gives an extra parameter that can be used to control the angular spring constant of the structure.

The lateral etch rate of the isotropic etch has been measured and is plotted in Figure 3.13 as a function of trench width. A clear aspect ratio dependent etching (ARDE) is shown which is not surprising since ARDE is a well known phenomenon [60]. As discussed in Paper B the results are reproducible and this method has been used to successfully fabricate mirrors with hidden hinge widths down to 1 μm. It should be possible to optimize the process to achieve submicron hinge widths but there is also the non-uniform etch rate with up to 40% difference in etch rate over the 150 mm wafer. As also discussed in Paper B the non-uniformity problem may be partly solved in more modern equipments but the process still relies on a “time-stop” of the etch. This is not attractive when working with low tolerances and achieving hinge widths of tens of nanometers as for the EUV mirrors in Paper A may not be feasible even for an optimized process. The next section presents a different approach to fabricate monocrystalline silicon hidden hinges with widths down to a few tens of nanometers using a more forgiving process.

### 3.4.2 By LOCOS

This process relies on local oxidation of silicon (LOCOS). LOCOS can be achieved by depositing silicon nitride on the surfaces that should not be oxidized. The silicon nitride oxidizes around 30 times slower than silicon [12] and acts as a diffusion barrier preventing oxidation of the covered silicon. Thermal oxidation of silicon is heavily employed in the semiconductor industry and is a very well characterized process. During the oxidation the silicon is transformed...
into silicon oxide and 44% of the resulting oxide thickness is consumed silicon. This is used in the LOCOS process for the formation of the hidden hinges as illustrated in Figure 3.14.

This process is used in Paper C and the starting material is a 500 μm thick p-type 150 mm silicon wafer. A 10 nm dry oxide is grown on the silicon substrate to protect the silicon surface during the continued processing as well as to create a stress relaxation layer for the deposited silicon nitride. 50 nm LPCVD silicon nitride and 300 nm thick LPCVD silicon oxide (TEOS) is deposited, see Figure 3.14a. The thick TEOS oxide acts as a mask in the coming etch steps and protects the underlying nitride layer.

In Figure 3.14b the dielectrics are patterned by e-beam lithography and CF₄/CHF₃ RIE. The silicon etch in Figure 3.14c is a 450 nm deep Cl₂ RIE. Next a 50 nm thick LPCVD silicon nitride and a 50 nm thick TEOS oxide is deposited, Figure 3.14d. The purpose of the thin TEOS oxide is to protect the underlying silicon nitride in the following etch steps. In Figure 3.14e the silicon nitride and oxide is removed at the bottom of the trench using the same CF₄/CHF₃ RIE as previously. 450 nm of the exposed silicon at the bottom of the trench is removed by a Cl₂ RIE resulting in a total trench depth of 900 nm, Figure 3.14f. By thermally oxidizing this structure, Figure 3.14g, it is possible to form a hidden hinge when the oxide is stripped, Figure 3.14h.
This process was used in Paper C to investigate the oxidation process in narrow trenches. The original idea was that the width of the hinge would be limited by or at least show a significant reduction in oxidation rate by the closing of the trench due to diffusion limitations. However, as suggested in Paper C, the oxidation that controls the hinge width is rather reaction rate limited due to the stress dependence of the reaction rate.

By using this process hinge widths down to 20 nm have been fabricated and Figure 3.15 (a) shows a 30 nm wide hidden hinge with surrounding oxide. If the distance between the trenches is small enough the hinge will be completely oxidized, Figure 3.15 (b). This could be used to create a tunnel under the bond surface to further control the angular spring constant of the hinge as for the isotropic etch process.

Due to the stress dependent oxidation the oxidation rate is reduced the thinner the hinge gets. This increases the uniformity of the hinges fabricated by

![Figure 3.15](image1.png)

**Figure 3.15 SEM image of a 30 nm wide hinge after LOCOS for 7 hr at 900 °C (a) and complete oxidation of the hinge (b).**

![Figure 3.16](image2.png)

**Figure 3.16. a) Hinge width as a function of distance between oxidized trenches. b) Calculated angular spring constant for the hinges from graph (a).**
this process. For the smallest structures in Paper C the hinges have a 50% lower spread in hinge widths after oxidation compared to before oxidation, Figure 3.16 (a). The angular spring constant for these hinges is plotted in Figure 3.16 (b). The depth of the hinge is assumed to be 2 μm and the height of the hinge, H, and radius of the connection, R, is measured from the scanning electron microscope (SEM) images and are close to H=300 nm and R=1 μm for all of the hinges. For the EUV mirrors in the case study in Paper A the angular spring constants are lower than 4 pNm which is achieved for the three thinnest hinges in Figure 3.16 assuming a hinge that goes through the whole mirror. This shows that it is possible to fabricate monocrystalline silicon hinges with angular spring constants suitable for EUV mirrors.

### 3.5 High spatial resolution adhesion quantification

Bonding of two or more patterned wafers is one of the key enabling technologies in micromachining of silicon based MEMS. When it comes to micromirrors on top of CMOS the use of monocrystalline silicon as the structural material would be virtually impossible without bonding. For the hidden hinge mirrors the successful bonding of μm²-sized areas is crucial and one key question arouse at an early stage; *Is the adhesion affected by the size of the bond area?* How to quantify the adhesion at this scale is discussed in this section.

#### 3.5.1 Quantification methods

During fabrication and use the bonded wafers are subject to mechanical stresses that can potentially lead to failure of the bond interface. A common fracture resistance measure is the mode I fracture toughness, $K_{Ic}$. $K_{Ic}$ is a material parameter and gives the material’s resistance to crack propagation. Effective fracture toughness measurements are crucial because it is one of the most important limiting properties of the bond interface.

Here follows a short summary of common adhesion quantification methods used in wafer bonding. Special focus is given to their respective spatial resolution. A more thorough survey of adhesion quantification methods in general can be found elsewhere [61].

**Double cantilever beam method**

The double cantilever beam (DCB) method is by far the most common method to measure the strength of bonded wafers [52,61-68]. When the DCB method is used the interfacial strength is frequently presented as the specific fracture surface energy, $\gamma_f$. This is the energy required to form a new surface with unit area of the material. $\gamma_f$ can be related to $K_{Ic}$ under plane strain conditions by
where $E$ is the Young’s modulus and $\nu$ is the Poisson’s ratio.

However, the DCB method requires rather large sample sizes due to the large crack length, commonly on the order of some millimeters.

**Tensile method**

In tensile tests or pull tests the samples are glued to studs and loaded in a materials testing machine until failure occurs. In these kind of tests regardless whether the samples are plane, have etched grooves or cavities in the bonded interface the measured strength is strongly influenced by small misalignments of the studs. Because of this the specimen sizes for the tensile test ranges from millimeters and up. For example chip size of $5 \times 5 \text{ mm}^2$ [69], $10 \times 10 \text{ mm}^2$ [70,71], and $250 \text{ mm}^2$ [72] has been reported.

**Blister method**

Blister tests use the pressure required to fracture the bond interface in a cavity sealed by wafer bonding to estimate the bond strength. Typical sizes of the cavities are a few millimeters. For example square cavities $2.8 \text{ mm}$ by $2.8 \text{ mm}$ [73] and $5 \text{ mm}$ by $5 \text{ mm}$ [74-76] have been reported. Channels are sometimes used instead of squares and channel widths from $560 \mu\text{m}$ up to $2000 \mu\text{m}$ have been reported [77]. The biggest challenge when scaling down these tests is probably the connection to the externally generated pressure. For the channels the lower limit is dictated by the $300 \mu\text{m}$ diameter capillaries used for connection.

**Miscellaneous methods**

The fracture toughness of wafers bonded using sol-gel bonding has been tested on a localized scale using Vickers indentation [78]. The bonded wafers are diced and the cross section is ground and polished. The Vickers pyramid is pressed into the bonded interface with a known force and the resulting crack lengths are measured using an optical microscope. The force and the crack length can be used to calculate the fracture toughness. Typical sizes of the reported total crack length are on the order of $50 \mu\text{m}$. This technique has only been tested on unpatterned wafers. However, there should be few practical issues performing measurements on a patterned interface given that the interface can be prepared. On the other hand, if the technique is suitable for such measurements is not clear.

A quantification method based on separation of bonded wafers by introducing mesa spacers in the bond interface prior to bonding has been presented [79]. The mesas create a known separation of the bonded wafers and the result-
ing radius of the unbonded area is measured by infrared transmission imaging. These two parameters give the surface energy of the bond. A mesa height of 2 μm resulted in a radius of more than 3 mm of the unbonded area. Consequently, this method is not suitable for high spatial resolution tests.

Notch fracture toughness has been determined for anodic bonded wafers using a three point bend test [80]. The chip size used was 3 mm by 3 mm and the sizes for the bonded region ranged from 200 μm up to 1400 μm high by 3 mm wide. Scaling down this method to chip sizes below millimeters will probably be hard due to the handling and alignment issues of the chips. Further scaling to sample sizes of a few micrometers will probably be very hard due to sample fabrication issues like defining the bond interface in the middle of a bend sample.

**Chevron method**

The chevron method originates from conventional macro scale testing of brittle materials, e.g. ceramics, where a chevron notch geometry is introduced into the test sample, see Figure 3.17. During loading the chevron geometry causes the crack growth to be stable until a certain critical value of the crack length. The critical crack length is determined only by the sample geometry and loading condition. Consequently, the fracture toughness can be determined
from the maximum load only. The chevron method has been used in both bend- and tensile tests to determine the fracture toughness of bonded wafers. For example, bend tests have been reported for direct bonded wafers using chip sizes of 8 mm by 6 mm [81] and 7 mm by 4.5 mm sized chevrons have been used for anodic bonded wafers [82]. The scaling of these bend tests have the same issues as the bend test discussed above.

A chevron approach based on the tensile test has been described [68] and specimen sizes down to 1.5 by 1.5 mm have been reported [83]. This method has a practical limit for how small the samples can be since they need to be equipped with studs and mounted in a materials testing machine. Sample sizes below 100 μm are not hard to fabricate but the testing would require very high precision during the gluing of the studs.

3.5.2 Quasi three-point method

In Paper D a test method for adhesion quantification with high spatial resolution of bonded areas is presented. The method is based on a three-point-bend chevron test, see Figure 3.17, and is applicable especially for small bonded structures. The method in itself is in principle not limited to any specific sample sizes. Measurement limits arise from a combination of limits in sample preparation and limits in the measurement equipment. For example, as shown

![Figure 3.18 Illustration of measurement setup used in Paper D (not drawn to scale).](image-url)
in Paper D, using an ordinary surface profiler the method is suitable for determining the mode I fracture toughness, $K_{IC}$, of bonded areas ranging from 5 by 5 $\mu$m$^2$ to 20 by 20 $\mu$m$^2$ in size. On the other hand, replacing the surface profiler with an atomic force microscope, this method could be used to evaluate even smaller bonded structures. An illustration of the measurement setup for the quasi 3-point bend test using a surface profiler can be seen in Figure 3.18.

In Paper D the presented method is compared quantitatively to the double cantilever beam (DCB) test. Measurements show that the average $K_{IC}$ value determined using this method is in close accordance with $K_{IC}$ values measured using the DCB method but a larger spread is observed which can be attributed to a real spatial variation of $K_{IC}$ shown by the higher spatial resolution of the presented method. An overview of the measurement setup for the quasi 3-point bend test using a surface profiler can be seen in Figure 3.18.

In Paper D the presented method is compared quantitatively to the double cantilever beam (DCB) test. Measurements show that the average $K_{IC}$ value determined using this method is in close accordance with $K_{IC}$ values measured using the DCB method but a larger spread is observed which can be attributed to a real spatial variation of $K_{IC}$ shown by the higher spatial resolution of the presented method. An overview of the presented quantification methods is given in Table 3.1.

### Stress analysis of the bonded interface using the vector J-integral

The stress intensity factors at the bond interface can be investigated by using FEA. A common approach to determine the stress intensity factors is by using the so-called vector J-integral. For three-dimensional problems two components of the vector J-integral can be defined as [84]

$$J_k = \frac{1}{\Delta} \lim_{\varepsilon \to 0} \int_{A_k} \left( Wn_k - \sigma_{ij} \frac{\partial u_i}{\partial x_j} n_j \right) dA, \quad k = 1, 2$$

\[(3.2)\]
where $x_1$, $x_2$, and $x_3$ represent the local crack front coordinate system: $x_1$ is normal to the crack front and lies in the crack plane, $x_2$ is orthogonal to both $x_1$ and the crack plane, and $x_3$ is tangential to the crack front and lies in the crack plane, see Figure 3.19 (a). $\Delta$, $\varepsilon$, and $A_\varepsilon$ is the length, radius, and area of the tube, respectively. $W$ is the stress-work density, $n_k$ is the $k$th directional component of the unit normal vector on $A_\varepsilon$, $\sigma_{ij}$ is the stress tensor, and $u_i$ is the displacement vector.

In the elastic-plastic case the components $J_k$ are used directly to construct the fracture criteria. For the linear-elastic case it is more common to determine the stress intensity factors, $K_I$ (opening mode), $K_{II}$ (shearing mode), and $K_{III}$ (tearing mode), see Figure 3.19 (b). These can be related to the energy release rates for the different modes, i.e. $J_I$, $J_{II}$, $J_{III}$ by

$$J_I = \frac{K_I^2}{E'}, \quad J_{II} = \frac{K_{II}^2}{E'}, \quad J_{III} = \frac{K_{III}^2}{G},$$

where

$$E' = E, \text{ for plane stress, } \quad E' = \frac{E}{(1-\nu^2)}, \text{ for plane strain},$$

and $E$ is the modulus of elasticity, $G$ is the shear modulus, and $\nu$ is Poisson’s ratio.

The energy release rates are related to $J_I$ and $J_{II}$ by

$$J_1 = J_I + J_{II} + J_{III},$$
$$J_2 = -2\sqrt{J_I J_{II}},$$

while $J_{III}$ can be directly calculated from

![Figure 3.19 a) Illustration of the integration surface $A_\varepsilon$ near the front of a three-dimensional crack and b) the different crack modes.](image-url)
\[
J_{\text{III}} = \lim_{\Delta \rightarrow 0} \int \left( \frac{\partial u_i}{\partial x_j} n_j \right) dA, \quad (j = 1, 2).
\]

Equations (3.5) can be used to find expressions for \(J_1\) and \(J_{\text{II}}\)
\[
J_1 = \frac{1}{4} \left( \sqrt{J_1 - J_2 - J_{\text{III}}} + \sqrt{J_1 + J_2 - J_{\text{III}}} \right)^2,
\]
\[
J_{\text{II}} = \frac{1}{4} \left( \sqrt{J_1 - J_2 - J_{\text{III}}} - \sqrt{J_1 + J_2 - J_{\text{III}}} \right)^2,
\]
and \(K_1\), \(K_{\text{II}}\), and \(K_{\text{III}}\) can now be calculated from equations (3.3), (3.6), and (3.7). For a more explicit description of how this is implemented in the simulation software COMSOL Multiphysics [85] see Appendix C.

FEA has been carried out in COMSOL Multiphysics [85] to determine any introduced discrepancies from the simplification of replacing the full 3-point bend specimen, Figure 3.17, with a quasi 3-point specimen, Figure 3.18. The two simulated samples have the same size, \(B=W=15 \mu m\), and the common parameters are summarized in Table 3.2; see Figure 3.17 and Figure 3.18 for definition of parameters. For the full 3-point bend sample the load is, as depicted in Figure 3.17, evenly distributed with a value of \(P/B=100/15 \approx 6.67\) mg/\(\mu m\) and the quasi 3-point sample has a centered point load of \(P/2=50\) mg. Both samples were idealized to one half of the full specimen size and symmetry boundary conditions were applied on the \(x=0\) plane.

In the FEA the material is simulated as anisotropic and the elasticity matrix used is [86]
\[
D = \begin{bmatrix}
D_{11} & D_{12} & D_{12} & 0 & 0 & 0 \\
D_{12} & D_{11} & D_{12} & 0 & 0 & 0 \\
D_{12} & D_{12} & D_{11} & 0 & 0 & 0 \\
0 & 0 & 0 & D_{44} & 0 & 0 \\
0 & 0 & 0 & 0 & D_{44} & 0 \\
0 & 0 & 0 & 0 & 0 & D_{44}
\end{bmatrix},
\]

where \(D_{11}=166\) GPa, \(D_{12}=64\) GPa, and, \(D_{44}=80\) GPa for \(D\) given in a coordinate basis aligned to the crystal axes (i.e. (100), (010) and, (001)). The crystal
orientation of the simulated chevron samples is, using the coordinate system illustrated in Figure 3.18, z=<100> and x=<110>. If another crystal orientation is desired it is only to use the same values in the elasticity matrix and change the orientation of the coordinate basis for D.

In Paper D the Bluhm slice model was used to calculate the shape factor, $Y^*$, for the quasi 3-point method. $Y^*$ is related to the stress intensity factor by

$$K_I = \frac{P}{B\sqrt{W}} Y^*(\alpha_0, \alpha_1, \alpha),$$

and the minimum value of $Y^*$ needs to be known in order to be able to calculate the fracture toughness from the measurement data in Paper D.

Figure 3.20 shows the shape factor for the simulated samples extracted by different methods. The minimum value of the full 3-point shape factor is 1% higher than the Bluhm value and the quasi 3-point shape factor value is 2% lower than the Bluhm value. This shows that the Bluhm slice model can be used to determine the shape factor with fairly good agreement for the quasi 3-point method.

An analysis of the influence of misalignment of the stylus in the x-direction and a rotation around the z-axis has also been performed. In this analysis a full quasi sample was modeled with an off-center and tilted point load. The results are shown in Figure 3.21 where the values for the stress intensity factors are normalized to zero offset and tilt. The tilt has very little influence on the stress intensity factors and the offset increases $K_{III}$ by less than 6% and affects $K_I$ and $K_{II}$ by less than 1%.
**Sources for measurement errors**

- **Misalignment of stylus in x-direction, load not centered on pillar:**
  The accuracy of this alignment comes from the accuracy of the measurement equipment. For the surface profiler used in Paper D this accuracy is estimated to ±2 µm and the error due to this less than 1%.

- **Misalignment of pillar target wafer to sample holder due to rotation in xy-plane:**
  If the sample is mounted by hand the accuracy of this alignment depends on the operator and size of the sample chips to be mounted in the sample holder. For the sample chip lengths used in Paper D the accuracy has been estimated to be better than ±5 degrees which also introduces an error of less than 1%.

- **Specimen geometry accuracy due to fabrication artifacts:**
  Overestimation of S/2 due to target wafer thinning during etchback and chevron notch geometry error due to etching/lithography artifacts could occur. Optimizing the specimen fabrication process can minimize these errors. The influence of possible errors in the chevron notch geometry has not yet been completely analyzed but for the samples fabricated in Paper D the accuracy in S/2 measurements has been estimated to ±2 µm.

- **Friction forces from the stylus leading to an underestimation of the $K_{IC}$:**

---

**Figure 3.21** Plot of the influence of misalignment on the stress intensity factors of a quasi 3-point specimen.
The FEA shows that a coefficient of friction of 0.11 [87] between the 
<100> single crystalline silicon and the diamond tip of the stylus also 
gives an error of less than 1%.

Discussion

The fracture toughness of a bonded interface is influenced more or less by 
all processing steps and handling until the point where measurements are per-
formed. This influence is perhaps even more pronounced when testing small 
bonded interfaces since the stresses on the structures are larger due to the size 
of the structures. Hence the spread in measured values could be larger since the 
bond interface of the test structures have been exposed to large forces and 
cracks can already have been initiated before the measurement. At the same 
time it can be argued that the spread in fracture toughness should be lower 
since there is no room for defects due to the small size of the test structure.

Using shallow chevrons (small $\alpha_0$) gives a slow rise in the $Y^*(\alpha)$ curve af-
fter the minimum at $\alpha_c$. This may give an underestimation of the critical crack 
length if the material shows a rising crack-growth resistance curve [88]. Look-
ing at the samples used in Paper D this would mean a systematic overesti-
ation of $K_{IC}$ when using the samples with $B=W$ compared to samples with 
$2B=W$. However, this is not the case when comparing the data from the two 
different geometries. Hence, the tested material shows no or very little signs of 
increasing crack-growth resistance behavior.

The presented realization of the measurement method in Paper D uses a 
surface profiler to apply force and measure distance. The surface profiler is a 
very common tool that exists in most micro/nanofabrication and research facili-
ties making the presented method widely available since no additional meas-
urement equipment is necessary. However, the surface profiler is not built with 
this application in mind and for very accurate and high precision measurements 
the equipment should be custom made for the application to minimize errors 
from the measurement setup. For engineering cases a value for the fracture 
toughness may be needed to accurately design the structures. For these applica-
tions the accuracy of the surface profiler is probably enough but for research 
where for example a deeper understanding of the bond interface is in focus 
there may be a need for a custom made tool. A suitable tool would be a shear 
tester with high resolution of the applied load and the possibility to accurately 
measure the height over the substrate for the applied load. The use of such a 
tool would enable the measurements to be performed without dicing the wafer 
and consequently reduce the external influence of the bonded interface prior to 
measurement due to sample fabrication and handling. This would also greatly 
simplify the measurement procedure. However, commercially available shear 
testers are not sensitive enough for this application since they operate in a
higher force range. The typical shear force to fracture a 35 μm ball bond is 15 grams [89] which is around 30 times more than for a 15 μm by 30 μm pillar using the presented method. Hence such measurement equipment has to be custom made.

### 3.6 Bond alignment accuracy

Accurately aligned silicon-to-silicon bonding is another key enabling technology for the fabrication of the monocrystalline silicon hidden hinge micromirrors. The bond aligner used in the fabrication of the mirrors in Paper B is a Karl Süss BA6. The standard approach for this aligner is to use double sided lithography to fabricate alignment marks on the backside of one of the wafers to be bonded. These marks are then aligned to a digitally stored image of alignment marks in the bond interface. The typically achieved alignment accuracy is 3-4 μm using this approach which is not accurate enough for the hidden hinge mirrors.

#### 3.6.1 Through wafer hole aligned bonding

In Paper E the use of through wafer holes to achieve submicron alignment accuracy is presented. The basic idea for this approach is very simple and straightforward to implement as illustrated in Figure 3.22 (a). By using this approach it is possible to align the wafers using a live image of the alignment marks. This eliminates alignment errors introduced by the double sided lithography and the digitally stored image. Further it is also possible to change the
alignment gap after the wedge error compensation (WEC), see Figure 3.22 (b). This is not allowed in the BA6 when using non-transparent substrates. As shown in Paper E a reduction of the alignment gap further increases the alignment accuracy.

In Paper B through wafer holes are used during the fabrication of the mirrors using both bulk silicon wafers and SOI wafers. The bond alignment marks are defined in the same DRIE as the trench separating the mirrors; see section 3.3.1 at page 28. The through wafer holes are etched by DRIE from the backside and the marks are suspended in circular membranes with a diameter of 1.5 mm. Figure 3.23 shows a 3D surface profile of a membrane from the SOI wafer in Paper B.

For bulk silicon wafers the membrane thicknesses have ranged from around 5 μm to 30 μm. These membranes have survived repeated spin drying and blowing with a nitrogen gun without fracturing. For the SOI wafers the same is observed for 15 μm device layers and 0.6 μm BOX. Figure 3.24 shows a photograph of an aligned membrane from such an SOI wafer. However, even
if the continued processing does not destroy the membrane residual stress in
the BOX could be a problem. Marks in 10 μm device layers with 2.5 μm BOX
were not completely destroyed but clearly damaged after the through wafer
DRIE. To avoid this the BOX should be kept as thin as possible even if the
marks were not destroyed and alignment was still possible.

3.6.2 Alleviation of alignment requirements

This sub-chapter presents an approach to alleviate the requirements on
bond alignment accuracy for the hidden hinge mirrors. If the actuation elec-
trode pairs are defined on the mirror wafer, only electrical interconnects need
to be formed to the electrode wafer during the bonding. An outline of a process
to achieve this on the mirror wafer is shown in Figure 3.25 where the position
of the cross section A-A is illustrated in Figure 3.26. The bond method needs to
be revised when using this approach. (This is outside the scope of this thesis).

Assuming that the mirrors are connected to the same electrical potential as
for the current torsion mirror design and that the electrical interconnect for this
potential can be done outside the mirror’s footprint, then it is possible to design
the electrical interconnect as illustrated in Figure 3.26. The triangles illustrate
the interface of the electrical interconnects on the electrode wafer and the cir-
cles illustrate the interfaces on the mirror wafer. The isosceles triangles have
the sides 2L and the radius of the circular interface is r. In Figure 3.26 (b) the
radius of the dashed circle, R1, can be calculated by simple geometry, see Ap-
pendix D, and is

![Figure 3.25 Suggested process outline for the formation of actuation electrode pairs on the
hidden hinge mirror wafer. The process steps between a and b are the same as illustrated in
Figure 3.5a-f. c) silicon oxide deposition and chemical mechanical polishing (CMP), d) deposi-
tion and patterning of electrodes and deposition of dielectric, e) patterning of dielectric and
deposition and patterning of electrodes. f) deposition of dielectric and CMP.](image-url)
$R_1 = \frac{L\sqrt{2}}{1 + \sqrt{2}}$.  \hspace{1cm} (3.10)

$R_1$ is the maximum allowed misalignment. For the $2 \times 2 \, \mu m^2$ large EUV mirrors in Paper A a diameter of the interconnect of $0.2 \, \mu m$ gives a maximum allowed misalignment of close to $0.5 \, \mu m$. For the $16 \times 16 \, \mu m^2$ large DUV mirror in Chapter 2 a diameter of the interconnect of $2 \, \mu m$ gives a maximum allowed misalignment of $3.7 \, \mu m$.

If there is a need to incorporate an electrical interconnect to the mirror under the mirror’s footprint a similar approach is possible but instead of just two interconnects a third is also needed. This is illustrated in Figure 3.27 and a similar geometric analysis, see Appendix D, gives the maximum allowed misalignment for this layout to

Figure 3.26 Suggestion for layout of electrical interconnect to alleviate bond alignment requirements.

Figure 3.27 Suggestion for layout of electrical interconnect to alleviate bond alignment requirements.
For the EUV mirrors with interconnect diameter of 0.2 μm the allowed misalignment is 0.4 μm and for the DUV mirror with interconnect diameter of 2 μm the allowed misalignment is 3.1 μm.

Even if the diameter of the interconnect needs to be increased so that there is no alleviation of the required alignment accuracy there are still design benefits of using this approach. As discussed in section 2.6 electrode misalignment affects the crosstalk and the actuation characteristics of the mirrors. By using this approach these design constraints will in principle be removed.

### 3.7 Characterization

In Paper B monocrystalline silicon hidden hinge mirrors have been fabricated using SOI wafers. Several 16×15 mm² chips were investigated using a SEM and Figure 3.28 shows images from one of the few arrays where mirrors
were not bonded successfully. This particular chip consisted of 16 8×8 arrays and 32 4×4 arrays and this was the only array on this chip where some mirrors had come loose. As presented in Paper B mirrors were also fabricated in a simplified process using bulk silicon wafers and Figure 3.29 shows SEM images of mirrors from that process.

The deflection versus voltage characteristics of the mirrors were measured using a Wyko NT1100 optical surface profiler. As discussed in Paper B there was a problem actuating the mirrors from the SOI wafer which was blamed on the quality of the aluminum oxide on the electrode wafer. On the electrode wafers in the simplified process using bulk silicon wafers there was no aluminum oxide layer and the actuation of these mirrors was successful. Figure 3.30 shows the actuation characteristics for the mirror in Figure 3.29. The tabulated geometrical parameters are measured from SEM images and the corresponding \( k_\theta \) is calculated numerically using the method in Paper A.

![Figure 3.30 Actuation characteristics of the hidden hinge mirror in Figure 3.29. The mirror parameters to the right were used in the numeric and FEM simulations. W, D, R, and \( k_\theta \) are the width, depth, radius, and angular spring constant of the hinge while 2L is the side of the mirror and G is the electrode gap.](image)

The deflection versus voltage characteristics of the mirrors were measured using a Wyko NT1100 optical surface profiler. As discussed in Paper B there was a problem actuating the mirrors from the SOI wafer which was blamed on the quality of the aluminum oxide on the electrode wafer. On the electrode wafers in the simplified process using bulk silicon wafers there was no aluminum oxide layer and the actuation of these mirrors was successful. Figure 3.30 shows the actuation characteristics for the mirror in Figure 3.29. The tabulated geometrical parameters are measured from SEM images and the corresponding \( k_\theta \) is calculated numerically using the method in Paper A.

![Figure 3.31 a) Typical 3D data from the optical surface profiler. b) top view of the scan showing the location of the X and Y profile in Figure 3.32.](image)

---

<table>
<thead>
<tr>
<th>Mirror parameters</th>
<th>W (µm)</th>
<th>1.4</th>
</tr>
</thead>
<tbody>
<tr>
<td>D (µm)</td>
<td>2.5</td>
<td></td>
</tr>
<tr>
<td>R (µm)</td>
<td>4.2</td>
<td></td>
</tr>
<tr>
<td>( k_\theta ) (nNm)</td>
<td>38</td>
<td></td>
</tr>
<tr>
<td>L (µm)</td>
<td>16</td>
<td></td>
</tr>
<tr>
<td>G (µm)</td>
<td>0.3</td>
<td></td>
</tr>
</tbody>
</table>
Due to the etchback of the bulk silicon mirrors the mirror surface is quite rough. rms values for the surface roughness is typically larger than 50 nm. This makes it very hard to extract the deflection of the mirror since it is smaller than the rms value. This problem can however be circumvented by scanning the unactuated mirror and subtracting this data from the actuated surface profile. Figure 3.31a shows a typical 3D scan from the optical surface profiler by using this approach.

Figure 3.32 shows X and Y profiles at the locations indicated in Figure 3.31.

Figure 3.32 X and Y profiles of an actuated mirror at the locations indicated in Figure 3.31.

Due to the etchback of the bulk silicon mirrors the mirror surface is quite rough. rms values for the surface roughness is typically larger than 50 nm. This makes it very hard to extract the deflection of the mirror since it is smaller than the rms value. This problem can however be circumvented by scanning the unactuated mirror and subtracting this data from the actuated surface profile. Figure 3.31a shows a typical 3D scan from the optical surface profiler by using this approach.

Figure 3.32 shows X and Y profiles at the locations indicated in Figure 3.31 (b). Apart from the curve for the actuated mirror the X profile also shows the edges of two adjacent mirrors. Since both the left and right adjacent mirrors are equally flat there is no significant crosstalk. If there was crosstalk between the mirrors the right adjacent mirror would have been deflected.
Chapter 4

Conclusions

Planarity requirements on micromirrors used in optical maskless lithography are very tough. Increasing the resolution of future lithography system by going to shorter wavelengths further increases the planarity requirements. The next wavelength on the lithography roadmap (EUV, $\lambda = 13.5$ nm) increases mirror planarity requirements by a factor of 20. This thesis deals with the design and in particular the fabrication of a novel monocrystalline silicon micromirror structure intended to meet the planarity requirements in future optical maskless lithography systems.

The presented mirror is composed of standing flexure hinges hidden underneath the optically active surface. The stiffness of these hinges can be designed independently of the thickness of the optically active surface allowing highly planar designs. Comprehensive mechanical analysis and simulations of the mirror structure is presented and it is shown that the micromirror structure can be designed to meet EUV planarity requirements. Compared to state-of-the-art DUV mirrors the herein presented structure achieves a planarity increased by more than an order of magnitude.

The fabrication of the mirrors is based on a low temperature transfer process. Mirrors are fabricated in the device layer of an SOI wafer and then transferred by aligned low temperature bonding to the addressing electronics. The use of a low temperature process facilitates the integration of the mirrors on top of CMOS addressing electronics which will be required for large arrays.
In order to reduce fabrication related artifacts and to be able to fabricate small mirrors a high bond alignment accuracy is important. A method to increase alignment accuracy during bonding of non-transparent substrates is presented. By using this method submicron post bond alignment accuracy has been achieved with good reproducibility.

Another important challenge is the formation of the hidden hinges. This thesis presents experimental results from two different methods to fabricate monocrystalline silicon hidden hinges. The first method is based on an alternating anisotropic and isotropic etch and hinge widths down to 1 \( \mu \text{m} \) have been realized. However simulations show that hinge widths down to tens of nanometers is required to realize EUV mirrors. This can be achieved by the second investigated method. The method is based on LOCOS in closely spaced trenches and has been used to achieve hinge widths down to 20 nm. This method is interesting since it also tends to increase the uniformity of the hinges due to stress dependent oxidation.

The fabrication of large arrays with millions of individual hidden hinge mirrors requires the successful bonding of the equal number of \( \mu \text{m}^2 \)-sized areas. This is outside the scope of this thesis but a method suitable for high spatial resolution mechanical characterization of bond interfaces is presented. The method has been used to characterize areas down to 20 \( \mu \text{m}^2 \) bonded by the currently used low temperature bond method. This is more than two orders of magnitude higher resolution than previously has been reported.

Arrays of monocrystalline silicon hidden hinge mirrors have been fabricated using the presented bond alignment method and isotropic hinge etch. Down to 16\( \times \)16 \( \mu \text{m}^2 \) sized mirrors have been realized and actuation characteristics of fabricated mirrors agree with theory and simulations. This clearly shows the feasibility of using this approach for fabrication of hidden hinge micromirrors. Issues specifically related to the realization of large arrays based on the hidden hinge mirror still require attention but no fundamental obstacles have been identified.
References

REFERENCES


REFERENCES


Appendix

A. Description of the 3D FEA for the compared mirrors

The FEA was performed in COMSOL Multiphysics [85] and the dimensions and material parameters used for the mirror are summarized in Table A.1. Figure A.1 shows the geometries from the FEA and the arrows represent the modeled load. The load is modeled as a distributed load over the edge of the mirror and the magnitude is 14 mNm⁻¹ which is the load required to deflect the mirror a quarter of a wavelength to \( \frac{193}{4} = 48.25 \) nm. The whole torsion mirror structure is free to move except the outer sides of the torsion hinges which are fixed. For the hidden hinge mirror the bond area is the fixed boundary.

<table>
<thead>
<tr>
<th>Torsion mirror</th>
<th>Hidden hinge mirror</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mirror and hinge thickness (nm)</td>
<td>300</td>
</tr>
<tr>
<td>Hinge width (nm)</td>
<td>700</td>
</tr>
<tr>
<td>Hinge length (μm)</td>
<td>2.0</td>
</tr>
<tr>
<td>Mirror size (μm)</td>
<td>16×16</td>
</tr>
<tr>
<td>Young’s modulus (MPa)</td>
<td>165</td>
</tr>
<tr>
<td>Poisson’s ratio</td>
<td>0.3</td>
</tr>
<tr>
<td>Density (kg/m³)</td>
<td>2329</td>
</tr>
<tr>
<td>Young’s modulus (MPa)</td>
<td>165</td>
</tr>
<tr>
<td>Poisson’s ratio</td>
<td>0.3</td>
</tr>
</tbody>
</table>

Figure A.1 Geometry of the torsion mirror and hidden hinge mirror as modeled in the FEA showing the resulting von mises stress from the distributed load illustrated by arrows. The scale bar to the right is in MPa.
The deformation of the mirror surface presented in section 2.4 is calculated from

\[ \delta_{\text{def}} - \delta_{\text{stiff}} = \left( |\Delta_2 + \Delta_1 + 2S| \right) \]  

(A.2)

where \( \Delta_2 \) and \( \Delta_1 \) is the FEA displacement at the middle of the deflected edges and \( S \) is the sagging as illustrated in Figure A.4. The sagging presented in section 2.5 is calculated by

\[ S = (2L)^2 \int w(x,y) \, dx \, dy \]  

(A.3)

where \((2L)^2\) is the area of the mirror surface \( \Sigma \) and \( w(x,y) \) is the FEA displacement of the mirror surface. The results from the FEA are summarized for both mirrors in Table A.2.

<table>
<thead>
<tr>
<th>Torsion mirror</th>
<th>Hidden hinge mirror</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \Delta_1 ) (nm)</td>
<td>-48.9</td>
</tr>
<tr>
<td>( \Delta_2 ) (nm)</td>
<td>-61.9</td>
</tr>
<tr>
<td>( \Delta_2 + \Delta_1 ) (nm)</td>
<td>-13.0</td>
</tr>
<tr>
<td>( S ) (nm)</td>
<td>-3.5</td>
</tr>
<tr>
<td>( \delta_{\text{def}} - \delta_{\text{stiff}} ) (nm)</td>
<td>6.1</td>
</tr>
<tr>
<td>Eigenfrequency (MHz)</td>
<td>1.33</td>
</tr>
</tbody>
</table>

Figure A.4 Illustration for the calculation of the surface deformation.
B. Calculation of the moment of inertia for the hidden hinge mirror

The moment of inertia for the hidden hinge mirror can be estimated by using Steiner’s theorem and assuming a rotational axis through the center of the hinge. A simplified geometry for the mirror can be seen in Figure B.1.

The moment of inertia for the hidden hinge mirror can be estimated by using Steiner’s theorem and assuming a rotational axis through the center of the hinge as illustrated in Figure B.1. The different moment of inertias correspond to $I_0$ for the whole mirror block with dimensions $x_0, y_0$ and depth $z_0$, $I_1$ for the two holes with radius $R_1$, $I_2$ for the rectangular openings under the holes, $I_3$ for rectangular bottom part with width $x_3$ of the “mirror foot”, and $I_4$ for the top part of the “mirror foot” which is simplified to an isosceles triangle with base $x_3$ and height $R_1$. The rotational axis goes through the center of mass for the whole mirror block but the other structures have an offset that needs to be considered. Including this offset in the calculations the moment of inertia for the different structures can be written [90]

$$I_0 = \frac{m_0}{12} \left( x_0^2 + y_0^2 \right) \text{ where } m_0 = x_0y_0z_0\rho$$ \hspace{1cm} (B.1)

$$I_1 = m_1 \frac{R_1^2}{2} + m_1 \left( \frac{x_2 + x_3}{2} \right)^2 \text{ where } m_1 = \pi R_1^2 z_0 \rho$$ \hspace{1cm} (B.2)

$$I_2 = \frac{m_2}{12} \left( x_2^2 + y_2^2 \right) + m_2 \left( \frac{x_2 + x_3}{2} \right)^2 + \left( \frac{y_2}{2} \right)^2 \text{ where } m_2 = x_2y_2z_0\rho$$ \hspace{1cm} (B.3)

![Figure B.1 Geometry for moment of inertia calculation.](image)
\[ I_3 = \frac{m_3}{12} \left( x_3^2 + y_2^2 \right) + m_3 \left( R_1 + \frac{y_2}{2} \right)^2 \quad \text{where} \quad m_3 = x_3 y_2 z_0 \rho \]  
(B.4)

\[ I_4 = \frac{m_4 x_3^2}{24} + \frac{m_4 R_1^2}{2} \quad \text{where} \quad m_4 = \frac{x_3 R_1}{2} z_0 \rho \]  
(B.5)

The total moment of inertia for the hidden hinge mirror is then calculated from

\[ I_{tot} = I_0 - 2I_1 - 2I_2 - I_3 - I_4 \]  
(B.6)
C. Calculation of stress intensity factors in COMSOL Multiphysics

Here follows a description of the implementation of the vector $J$-integral in COMSOL Multiphysics for calculation of the stress intensity factors discussed in section 3.5.

First we need to find explicit expressions for the terms in equation (3.2) which is repeated here for clarity.

\[ J_k = \frac{1}{\Delta} \lim_{\varepsilon \to 0} \int \left( W n_k - \sigma_{ij} \frac{\partial u_i}{\partial x_j} n_j \right) dA, \quad k = 1, 2 \]  

(3.2)

$\Delta$, $\varepsilon$, and $A_\varepsilon$ as defined in Figure 3.19 (also repeated here for clarity) can be chosen freely. I choose to integrate over the whole crack front, i.e. $\Delta=$crack front width, in order to get the average stress intensity factor. Three different values for $\varepsilon$ were chosen in order to check the stability. The stress work density, $W$, is already predefined in COMSOL and is called $W_{s\_smsld}$ (if working in 3D solid, stress-strain).

The traction vector for the second term in the integral, i.e. $\sigma_{ij}n_j$, is also predefined in COMSOL. However, the normal vectors created by the software do not always point in the desired direction, i.e. away from the crack front. In order to get the right sign I choose to define my own normal vectors, $N_x$, $N_y$, and $N_z$. This also means defining my own traction vector which could look like this in COMSOL.

![Figure 3.19 Illustration of the integration surface $A_\varepsilon$ near the front of a three-dimensional crack.](image-url)
\[
\sigma_{ij} \frac{\partial u_i}{\partial x_j} n_j = \sigma_{i1} \frac{\partial u_i}{\partial x_k} n_1 + \sigma_{i2} \frac{\partial u_i}{\partial x_k} n_2 + \sigma_{i3} \frac{\partial u_i}{\partial x_k} n_3 = \\
= n_1 \left( \sigma_{11} \frac{\partial u_i}{\partial x_k} + \sigma_{21} \frac{\partial u_i}{\partial x_k} + \sigma_{31} \frac{\partial u_i}{\partial x_k} \right) + \ldots \\
+ n_2 \left( \sigma_{12} \frac{\partial u_i}{\partial x_k} + \sigma_{22} \frac{\partial u_i}{\partial x_k} + \sigma_{32} \frac{\partial u_i}{\partial x_k} \right) + \ldots \\
+ n_3 \left( \sigma_{13} \frac{\partial u_i}{\partial x_k} + \sigma_{23} \frac{\partial u_i}{\partial x_k} + \sigma_{33} \frac{\partial u_i}{\partial x_k} \right) = \quad (C.1)
\]

The definition for the terms in equation (3.6) is very similar and from here it is straightforward to calculate the stress intensity factors.
D. Geometrical analysis of the alignment accuracy requirements

The layout of the interface with two interconnects is illustrated in Figure D.1 (a). The radius, $R_1$, is easily described in terms of $L$ by expressing the diagonal of the square, $2\sqrt{2}L$, in terms of $R_1$

$$2\sqrt{2}L = 2R_1(1+\sqrt{2}) \Rightarrow R_1 = \frac{\sqrt{2}L}{1+\sqrt{2}} \quad (D.1)$$

For the interface with three interconnects the layout is illustrated in Figure D.1 (b). Here $R_2$ can be calculated by expressing the side of the square, $2L$, in terms of $R_2$. The angle of $15^\circ$ in the figure comes from that the angle from the line $2R_2\cos15^\circ$ to the diagonal of the square is $45^\circ$. The diagonal also cuts the $60^\circ$ angle of the equilateral triangle in half. Hence $45^\circ-30^\circ=15^\circ$ and the side of the square can be written

$$2L = 2R_2(1+\cos15^\circ) \Rightarrow R_2 = \frac{L}{1+\cos15^\circ} = \frac{4L}{4+\sqrt{2}+\sqrt{6}}$$

$$ \quad (D.2)$$

Figure D.1 Layouts of the interface with two interconnects (a) and with three interconnects (b).