Integrated Variable-Gain and CMOS Millimeter-Wave Amplifiers

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Variable Gain Amplifier finds extensive use in the high frequency demonstrators specially those operating in the millimeter-wave regions and beyond where the incoming RF signal level can have wide variations. To maintain a constant signal level an IF VGA has been designed that can offer a dynamic variation of gain as much as 45 dB together with a high maximum gain and a low noise figure. The first part of the thesis starts with theoretical as well as analytical investigations of designing a VGA based on the various possible topologies. Feasibility of implementing the Monolithic Microwave Integrated Circuit (MMIC) version of the IF VGA is then followed. Foundry based High Electron Mobility Transistors (HEMT) have been used for the realization of the circuit. Two high gain, low noise, VGA have been designed and characterized based on series feedback and parallel feedback topologies. A 45 dB of gain control and a maximum gain of 47 dB have been achieved with the series feedback VGA whereas the corresponding figures for the parallel feedback VGA are, 55 dB and 35 dB, respectively. The circuits were designed for a center frequency of 2.5 GHz. The noise figure for the series feedback VGA is 0.81 dB in the highest gain mode and for the parallel feedback VGA it is 0.86 dB. The -1 dB compression and OIP3 for the series feedback VGA are -7.2 dBm and +2 dBm, respectively. The corresponding figures for the parallel feedback VGA are -9.5 dBm and +1.3 dBm, respectively. The second part of the thesis discusses the design and characterization of small signal amplifiers using a foundry based submicron CMOS processes both with the 45 nm and the 90 nm technology. The latest state-of-the-art 45 nm CMOS process i.e the bulk CMOS and the FinFET have recently got much attention of the researchers. A brief investigation on $f_t$ for both the devices have been carried out followed by a concise overview on the technology. Maximum achievable value of $f_t$ for 45 nm bulk CMOS is of the order of 200 GHz. For FinFET this value is around 100 GHz. Two wiring options i.e. the Back-End-Of-Line (BEOL) and the post process Wafer-Level-Packaging (WLP) have been consid-
ered for transmission line as well as passive implementations and are discussed in some details. It is then followed by the MMIC implementations of the small signal amplifiers. Foundry provided models as well as in-house developed models are used in the circuit analysis. The 40 GHz amplifier designed in the back end of 90 nm CMOS gave a measured gain of 6 dB at 40 GHz. The corresponding measured noise figure is 7.8 dB. The measured -1 dB compression is -5.5 dB referred to the output. Using the same technology node, the 20 GHz amplifier gave a gain of 5.8 dB with the measured NF of 5.4 dB. The non linear measurement gave -1 dB compression of +1 dB and an IP3 of +10 dBm both referred to the output. Amplifiers designed in the latest 45 nm CMOS technology, shows promising results with an achievable gain as much as 12 dB at 90 GHz.

**Keywords:** MMIC, CMOS, LNA, VGA, GaAs, BCB, HEMT, WLP, FinFET
List of Publications

Appended papers

This thesis is based mostly on the works contained in the following papers referred to by capital letters in the text:


Other Contributions

Related papers not appended to this thesis:


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<td>$C_{gd}$</td>
<td>Gate to Drain Capacitance</td>
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<td>$C_{gs}$</td>
<td>Gate to Source Capacitance</td>
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<td>$C_{pd}$</td>
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Abbreviations

ADC      Analog to Digital Converter
ADS      Advanced Design System
BCB      BenzoCycloButene
BEOL     Back End-of-Line
BSIM     Berkeley Small Channel MOS Model
CDMA     Code Division Multiple Access
CMOS     Complementary Metal Oxide Semiconductor
CMP      Chemo Mechanical Polishing
CMRR     Common Mode Rejection Ratio
Cu       Copper
dB       Deci-Bell
DIBL     Drain Induced Barrier Lowering
FEOL     Front End-of-Line
FET      Field Effect Transistor
GaAs     Gallium Arsenide
HARVi    High Aspect Ratio Via
HBT      Heterostructure Bipolar Transistor
HEMT     High Electron Mobility Transistor
HFET     Heterosructure Field Effect Transistor
HfO₂     Hafnium Oxide
HP       Hewlett-Packard
IEEE     Institute of Electrical and Electronic Engineers
IF       Intermediate Frequency
IIP3     Input Third Order Intercept Point
IMD      Inter Metal Dielectric, Inter Modulation Distortion
LNA      Low Noise Amplifier
MESFET   Metal Semiconductor Field Effect Transistor
MIC      Microwave Integrated Circuits
MMIC     Monololithic Microwave Integrated Circuit
MOSFET   Metal Oxide Silicon Field Effect Transistor
NF       Noise Figure
OIP3     Output Third Order Intercept Point
PMD      Pre Metal Dielectric
RF       Radio Frequency
SCE      Short Channel Effects
SF       Source Follower
SFDR     Spurious Free Dynamic Range
SiC      Silicon Carbide
SiGe     Silicon Germanium
SiON     Silicon Oxynitridation
SNR      Signal to Noise Ratio
SOI      Silicon-On-Insulator
UWB      Ultra Wide Band
VGA      Variable Gain Amplifier
WLAN     Wireless Local Area Network
WLP      Wafer Level Packaging
WPAN     Wireless Personal Area Network
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Chapter 1

Introduction

1.1 Monolithic Microwave Integrated Circuits (MMICs)

A Monolithic Microwave Integrated Circuit (MMIC) is an ensemble of active and passive components required for a given circuit that is fabricated on the same substrate. Depending on the type of technology used, the operating frequency can range from 1 GHz up to several hundred GHz. In the mid of 20th century, microwave circuits were realized using waveguide components. Designs were mostly experimental, lengthy and above all expensive. With the introduction of teflon, a cheap and low dielectric material in the mid 60’s, the concept of Microwave Integrated Circuit (MIC) first came into being [1]. The technology was based on mounting discrete devices on a dielectric substrate that acts as transmission medium. Adhesive, soldering or bonding were used to incorporate the discrete devices (available in packaged form) on to the substrate. In a thin film hybrid MIC, some of the simpler components are deposited on the substrate. Soon it became obvious that fabrication of all the active and passive components of a whole microwave circuit is not far beyond the means of the researchers.

The first GaAs MMIC was reported in 1968 [2] with a simple combination of diodes and micro-strip lines. And the first transistor based MMIC (a broad band amplifier) using GaAs FET was reported in 1976 [3]. Gallium arsenide (GaAs) has been used extensively in the development of MMIC since devices and circuits processed with it can operate well beyond the microwave frequency. High electron mobility and peak drift velocity are the two unique properties that make microwave devices fabricated in GaAs more conspicuous. They give rise to higher $g_m$ and shorter carrier transit time.
CHAPTER 1. INTRODUCTION

The high carrier mobility also results in lower parasitic drain and source series resistances which are major contributors to the NF of an LNA. Moreover, the high resistivity semi-insulating GaAs substrate reduces crosstalk between devices. Passive components such as stubs and transmission lines are less lossy and the overall noise contribution is minimum compared to the conventional CMOS (complementary metal oxide semiconductor) apart from having higher $f_t$ and $f_{\text{max}}$. Therefore interest in GaAs based MMIC grew tremendously in the industry as well as in the research community in the 70’s and 80’s. The technology attained both its maturity and dominance very soon even though MMIC using other technologies like InP or SiGe was gaining popularity.

On the other hand, research based on Silicon particularly CMOS was mainly constrained to digital domain in the 70’s and the beginning of 80’s with memories and processors constituting the bulk of the semiconductor business. In the late 80’s, with the rapid expansion of wireless industries, CMOS substantiated to be a viable alternative to III-V devices with regards to high integration capabilities, lower power consumptions as well as minimum cost. The maximum operating frequency $f_{\text{max}}$, which measures how much power gain can be achieved from a device, is strongly influenced by the transistor gate resistance, output resistance and overlap capacitance. The unity-current-gain frequency, $f_t$, provides a measure of speed of the device and is proportional to its transconductance, $g_m$. Both $f_t$ and $f_{\text{max}}$ usually increase with the technology down-scaling. So, implementation of millimeter wave MMIC in silicon appeared to be more and more realistic with every generation of technology down scaling. In the last two decades CMOS has gradually embraced the analogue domain with low cost and efficient solutions to circuits in the low frequency range up to 10 GHz band. Even though III-V devices are more mature than CMOS when it comes to implementing millimeter wave MMICs, interest in the latter is growing rapidly. Making a circuit to work in CMOS at this high frequency is therefore, a real challenge for the designers.

1.2 Thesis structure

This thesis discusses the MMIC implementation of small signal low noise amplifier and IF variable gain amplifier in the submicron technology.

The first part of the thesis dwells on the MMIC implementation of
1.2. THESIS STRUCTURE

high gain, low noise variable gain IF amplifier. Investigation of existing topologies, their pros and cons have been studied and analyzed. New topology namely the series feedback based on GaAs HEMT process have been proposed, implemented and characterized. The main aim of the design is to maximize the gain variation and to achieve a high maximum gain. The work is then compared to another VGA design based on parallel feedback topology. The dynamic variation of gain in both the design is achieved by controlling the channel resistance of a HEMT device. Finally a comparative investigation is carried out based on the published works on the above topic.

Work on submicron CMOS was carried out in the second part of the thesis. The main aim was to investigate the feasibility to designing CMOS based amplifier specially in the millimeter-wave region. The investigation is initiated by studying the unity current gain frequency, $f_t$ and maximum oscillation frequency, $f_{\text{max}}$ of the MOS devices and then proceeded towards circuit implementation. Several small signal amplifiers have been designed and characterized. Two wiring options have been considered for circuit implementation i.e. the Back-End-Of-Line (BEOL) and the Wafer-Level-Packaging (WLP). These were discussed in some detail together with the process and technology as well as passive device implementations. Finally a comparative investigations have been carried out based on the result of the state-of-the-art amplifiers to that of the reported works.
Chapter 2

Variable Gain Amplifier

Variable gain amplifiers are used in the radio communication systems in order to regulate the RF/IF power to desired levels [4]. The transmitted and received signals can have a wide range of amplitude variations depending on the instantaneous signal path and other obstructions. The signal processing ability of a receiver is governed by the noise level as its lower limit and by the signal distortion by the upper limit. This range is usually called the dynamic range. Achieving high dynamic range involves trade off between the input signal level with respect to the noise level and the output distortion level. In cellular communication system VGA’s are used [5], [6], [7], in the handset to ensure equal power level received at the base station. Other applications of VGA are: temperature compensation in satellite communication systems [8], design of active phase shifter [9], [10].

![Figure 2.1: Simplified receiver unit with the variable gain amplifier in the IF block.](image)

The gradual down scaling of existing technologies makes the high data rate transmission more promising at high frequency particularly in the millimeter wave regions and beyond. Successful implementation of demonstrator operating in the V band has already been reported [11], [12], [13]. In such microwave systems, a variable gain amplifier, at the IF block, plays an essential role of providing the Analog to Digital Converter (ADC) with constant IF signal for effi-
efficient sampling. Figure 2.1 shows the simplified schematic of an IF sampling receiver architecture where the variable gain is applied to the IF block to effectively adjust the sensitivity of the ADC and the overall detection limit of the receiver chain. Controlling the gain enables the IF signal to remain in an optimal level for digital demodulation. In such an architecture, noise figure and linearity are the two important optimizable parameters for successful operation of a variable gain amplifier.

2.1 Methods to Achieve Gain Variation

This section discusses four methods of achieving gain variations, the Gilbert Cell, the Cascode cell, Cascaded ”Π” and ”T” network and transistors with feedback.

2.1.1 The Gilbert Cell

The small signal gain of a differential pair is a function of the tail current. The two transistors in a differential pair steer the tail current to one of the two destinations [Fig. 2.2]. The control voltage, \( V_{\text{con}} \), governs the tail current and so does the gain. If \( I_{QA} = 0 \) then \( V_{\text{OUT}} = +g_{m}R_{D}V_{\text{IN}} \) and If \( I_{QB} = 0 \) then \( V_{\text{OUT}} = -g_{m}R_{D}V_{\text{IN}} \). But for
2.1. METHODS TO ACHIEVE GAIN VARIATION

2.1.2 Cascode Configuration

Fig. 2.3(a) shows the schematic of a cascode configuration with the control voltage applied to the gate of the cascode transistor. Gain variation is achieved by controlling the effective transconductance, $G_m$, of the cascode configuration. Variation of the $G_m$ with the control voltage, $V_{con}$, for two different gate bias is shown in Fig. 2.3(b). The higher the gate voltage, the greater the $G_m$ variation range. The

Figure 2.3: (a) Schematic representation of cascode configuration (b) Simulated variation of transconductance with the control voltage. Simulation was carried out using 100 µm ($2\times50$) transistor provided by the WIN Semiconductor of Taiwan. Model of the transistor was provided by the same foundry.

$I_{QA}=I_{QB}$, the gain drops to zero [14].

The main advantages of this topology is higher gain control range compared to cascode or feedback topology discussed in the following sections. It is popular with CMOS process due to the high integration capability of SI technology and the lossy nature of silicon. Main disadvantages are the layout complications and the integration complexity. Presence of more than one device in the circuit imposes extra constraints to the power consumptions, a crucial parameter for systems operating in the high frequency regions. Added with this is the MMIC implementation of the matching network or baluns which, if realized with passive elements, can result in substantial layout enlargement. Active balun may help save die area but imposes further limitations to the DC power requirements of the system. Most of the reported works [15] based on this topology are for the WCDMA applications.
main disadvantage of this topology is the poor linearity under compressed gain condition [16]. In the presence of a strong signal, the gain ($G_m$ in turn) is reduced by the control voltage applied to the gate of the control transistor. IP3, a parameter of linearity measure and a function of $G_m$, is affected in the same order. This dependence of linearity on gain makes this topology less popular where the incoming signals can be rather strong. The main advantage is its capability to selectively obtain low DC power dissipation and low noise figure. Some recent works up to X band based on this topology can be found in [17], [18]. Reports of working MMIC VGA up to W based on dual gate topology can be found in the literature [19], [20], [21], [22].

A dual-gate can be used to control the gain as shown in Fig. 2.4. This is virtually a representation of the cascode configuration above. It is operated normally in common source configuration with the input signal applied to the first gate while the second gate is RF grounded. This is equivalent to a common source and a common gate configurations connected in cascade as shown in Fig. 2.4(b). A general investigation on control strategy of the second gate on RF performance (gain, NF etc.) of a dual gate GaAs FET can be found in [23], [24], [25], [26].

### 2.1.3 Cascaded "Π" and "T" network

This topology is based on the cascaded combination of an attenuator and an amplifier. An attenuator is a network that reduces the input RF power by a predetermined ratio. The most common forms are the "T", the "Π" and the "bridged-T" networks as shown in Fig. 2.5.

Each of the networks in the figure can be used to implement a vari-
2.1. METHODS TO ACHIEVE GAIN VARIATION

Figure 2.5: Schematic of network configurations (a) T network (b) Π network and (c) bridged-T network.

able attenuator by using a variable resistor in the arms [27]. As opposed to two other attenuator configurations, the bridge-T attenuator uses two arms namely, R1 and R2 as variable resistors to realize the variable attenuators [28]. $Z_0$ is the characteristic impedance here. Use of FETs in zero bias mode, arranged in PI, Tee, and Bridged-T configuration for achieving variable resistance is quite common in the design of voltage controlled variable attenuators [29], [30], [31], [32]. Any of the above networks (Fig. 2.5) cascaded with conventional amplifiers can result in a variable gain amplifier with varying degrees of gain margin. The half "T" is the other possible arrangement to realize the desired variable attenuator in where a series FET (in zero bias mode) is followed by a shunt FET [33].

The main disadvantage is the degradation of the noise figure. The overall NF is the product of the NF of the amplifier and the loss factor of the attenuator (absolute numbers). This causes excessive degradation of the SNR affecting signal integrity to the subsequent blocks of the receiver.

2.1.4 Feedback Topologies

Based on the type of feedback, the dependance of gain variation can either be linearly proportional or inversely proportional to the variation of the control element. There are two possible ways to connect the feedback component between the terminals of the active device.

◇ Series feedback
◇ Parallel feedback

For a common source configuration, the feedback component is connected between the gate (input) and the drain (output) terminal. This arrangement is called the shunt or parallel feedback topology. In the series or source feedback VGA, the control resistor is con-
CHAPTER 2. VARIABLE GAIN AMPLIFIER

Figure 2.6: Common source configuration (a) Series feedback VGA (b) Parallel feedback VGA.

Connected between the gate (input) and the source (common) terminal. Fig. 2.6 shows the general circuit schematic of the feedback VGA in the common source configuration.

Most of the reported works on feedback VGA are based on either shunt feedback topology [16], [34] of common source configuration [Fig. 2.6(b)] or using the topologies described in sections 2.1.1-2.1.3. The investigation of source feedback VGA [35] based on the proposed topology of Fig. 2.6(a) lays the foundation of this part of the thesis.

2.2 Motivation: Topology and design structure

There were three main issues that were given due considerations among others while designing the variable gain amplifier:

- High range of gain variation
- High value of maximum gain
- Low Noise Figure

A high maximum gain is desired in order to detect a weak signal which is typical of a receiver operating in the high frequency regions specially in and around the millimeterwave regions. Most of the reported works of VGA strive to achieve high range of gain variations
without giving much effort on keeping the minimum gain near unity and goes far down to zero dB (loss). This ultimately results in excessive NF while compressing a strong signal. The resulting high value of gain variation also gives rise to a large variations in NF.

Another important parameter is the stability factor which becomes crucial when requirements for maximum gain is high. For instance, in radio astronomy applications, the incoming signal is rather weak and usually lie close to the noise floor. For optimum detection of the signal, the required gain could be as much as 60 dB. To ensure stability the gain stages are usually, implemented in the IF block. Though feedback topologies are well known for giving better results in this respect, simultaneous attainment of high maximum gain coupled with high range of gain variation still remains a challenging design task. This thesis therefore, targets these issues in greater detail. Since linearity plays an important role on the performance of the subsequent blocks specially ADC, relevant investigations on this matter have also been carried out where feasible.

In order to achieve high range of gain variation, more than one stages of VGAs are cascaded together. To address the issue of stringent demand on noise, a low noise amplifier has been used in front of the VGA. The output of the VGA is taken from a source follower. It is designed in constant current self bias mode. The main aim of using a source follower at the output is to achieve an active load match [36]. In addition, the source follower prevents the output from loading the last amplifier stage. Fig. 2.7 shows the arrangement of the subcircuits of the multistage VGA.

As part of the proposition of the series feedback variable gain amplifier, a single stage VGA has first been implemented and characterized. This is then followed by a multistage implementation. A two stage parallel feedback VGA (with an LNA at the input and the output taken from a source follower) has also been implemented and characterized. The aim is to perform a comparative investigation between the two designed topologies based on their performances.
To realize the variable resistor in the feedback VGA’s, the channel resistance of a zero biased FET has been used. Fig. 2.8 shows the measured $R_{ds}$ of commercial HEMTs in zero bias mode i.e. with $V_{dd} = 0.05$ V. The channel resistance shows an exponential dependence on the gate voltage in the reverse order. Analytical approach to explain the validity of using a zero biased FET as variable attenuator can be found elsewhere [28]. In this work, an equivalent circuit approach has been proposed with relevant mathematical reasoning.

2.2.1 Technology

Realization of the MMIC circuits were made available from WIN foundry [37] using GaAs HEMT technology. Both the pseudomorphic and the metamorphic versions have been used. Foundry provided models were used for circuit simulation. A 0.15 µm pHEMT has been used for series feedback VGA. The device has an extrinsic $g_m$ of 495 mS/mm, gives a drain current of 650 mA/mm and has a mean $f_t$ of 85 GHz. The parallel feedback VGA on the other hand, was realized with a 0.15 µm mHEMT process. The device has a $g_m$ of 730 mS/mm, gives a drain current of 650 mA/mm and has a mean $f_t$ of 110 GHz.
2.3 Series Feedback VGA: Theoretical Investigation

Based on the basic circuit configuration depicted in Fig. 2.6(a), the control resistance is replaced by a zero biased FET and is connected to the source resistance $R_s$ through a high value of coupling capacitor, $C_{cc}$ as shown in Fig. 2.9. The gain is varied by the equivalent control impedance, $Z_X$ and is given by:

$$Z_X = \frac{R_s + sR_{ds}R_s (C_{eq} + C_{cc})}{1 + s \left[ R_s C_{cc} + R_{ds} (C_{eq} + C_{cc}) \right] + s^2 \left( R_s R_{ds} C_{eq} C_{cc} \right)} \quad (2.1)$$

where $R_s$ is the source resistance, $C_{cc}$ is the coupling capacitor, $R_{ds}$ is drain to source resistance of the control transistor, and $C_{eq}$ is the equivalent capacitor across the source and drain. If the control transistor is driven from a low impedance source, $C_{eq}$ is approximately equal to the sum of $C_{ds}$ and $C_{gd}$. $R_{ds}$, $C_{gs}$, and $C_{gd}$ are dependent

**Figure 2.9:** Basic circuit configuration of series feedback VGA.

**Figure 2.10:** Equivalent circuit model for the control transistor of Fig. 2.9.
on the gate to source voltage, although the latter two can be approximated as constant for this small signal application.

\[ Z_X \text{ with values of } R_s \text{ and } C_{cc} \text{ according to Table 2.2 is plotted in a Smith-chart in Fig. 2.11 for a 200 } \mu\text{m (4 fingers) gate width pHEMT using the foundry model. } V_{con} \text{ was swept from -1.2 V to -0.5 V with a step of 0.1 V to illustrate the change of } Z_X. \text{ The frequency was also swept from 2 to 3 GHz. This plot shows that } Z_X \text{ is not purely resistive and the capacitive part needs to be considered also.} \]

The gain variation of this amplifier relies on the variation of \( R_{ds} \) and so it is interesting to investigate \( R_{ds} \) versus \( V_{gs} \). In Fig. 2.12, \( R_{ds} \) versus \( V_{gs} \) \([V_{con}]\) is plotted together with the real part of \( Z_X \). \( R_{ds} \) for a 100 } \mu\text{m (2 fingers) pHEMT was measured with an HP 4145A parameter analyzer. The measured data is scaled to a 200 } \mu\text{m device (4 fingers) assuming that } R_{ds} \text{ is inversely proportional to the total gate width. At low } V_{con} \text{ values, close to pinch-off for the control transistor, the influence of } R_{ds} \text{ is small, and } R_s \text{ (to some extent also } C_{eq}) \text{ determines the minimum gain. At higher } V_{con} \text{ values, the control transistor is conducting and the gain is increasing. The gain is now mainly determined by } R_{ds} \text{ and } C_{cc}. \text{ The coupling capacitor } C_{cc}, \text{ should be sufficiently large in order not to significantly influence the maximum gain.} \]

Fig. 2.13 shows the simplified equivalent small signal model for the series feedback VGA together with \( Z_X \), a variable quantity given by
2.3 SERIES FEEDBACK VGA: THEORETICAL INVESTIGATION

Figure 2.12: Simulated plot of $R_{ds}$ (solid triangle) and real value of $Z_X$ (star) versus the control voltage, $V_{con}$ (X axis). Foundry model of 200 $\mu$m (4 fingers) pHEMT has been used in the simulation. The measured $R_{ds}$ (square) is superimposed on the plot. The drain voltage was set at 0.05 V during the measurement.

Figure 2.13: Simplified equivalent small signal model of SF VGA. Equivalent circuit of $Z_X$ is depicted in Fig. 2.10 and is quantified by equation (2.1).

The voltage gain for a load impedance of $Z_L$, is given by:

$$A_V = \frac{V_{out}}{V_{in}} = \frac{g_m Y_X(s) - s \zeta - s^2 \xi}{g_{ds} Y_X(s) + Y_L [g_m + g_{ds} + Y_X(s)] + s \eta + s^2 \xi}$$  \hspace{1cm} (2.2)$$

Where, $Y_X(s) = 1/Z_X(s)$; $Y_L = 1/Z_L$.
\[ \xi = C_{gd}C_{gs} + C_{gs}C_{ds} + C_{ds}C_{gd} \]
\[ \zeta = g_{ds}(C_{gs} + C_{gd}) + C_{gd}(Y_X(s) + g_m) \]
\[ \eta = C_{gs}(g_{ds} + Y_L) + C_{ds}(Y_X(s) + Y_L) + C_{gd}(Y_X(s) + g_m + g_{ds}) \]

The analytic expression of equation (2.2) is verified by comparing the simulated gain. This is shown in Fig. 2.14. In principle, any realistic numbers can be considered for the intrinsic elements and we chose some typical values as mentioned in Table 2.1.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
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<td>$C_{gs}$</td>
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<tr>
<td>$C_{gd}$</td>
<td>20 fF</td>
</tr>
<tr>
<td>$g_m$</td>
<td>150 mS</td>
</tr>
<tr>
<td>$\tau$</td>
<td>0.15 ps</td>
</tr>
<tr>
<td>$R_{ds}$</td>
<td>250 Ω</td>
</tr>
<tr>
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<td>$Y_L$</td>
<td>10 pF</td>
</tr>
<tr>
<td>$R_L$</td>
<td>50 Ω</td>
</tr>
</tbody>
</table>

**Figure 2.14:** Calculated (circled) and simulated (solid) variation of voltage gain for sweeping $R_{ds}$ at 2.5 GHz verifying the accuracy of the expression of equation (2.2).
2.4 Circuit Implementation

2.4.1 Single Stage VGA

The schematic depicted in Fig. 2.9 is used as the foundation block for the single stage VGA implementation. The modified design is shown in Fig. 2.15. An active load (Q₁) has been used in the drain instead of a conventional passive components. This saves circuit area, give good stability margin, increases the gain and overall is suitable for implementation in the IF block.

The output of the VGA is taken from a source follower, Q₃. The source follower is designed in constant current source self-bias mode. By proper scaling of Q₃, it is possible to match the load to a reasonable degree and to make it independent of gain variation. The control voltage $V_{con}$, which is applied to the gate of the control transistor (Q_c), governs the variation of $R_{ds}$ of Q_c and in turn vary the gain.

![Circuit schematic of a single stage VGA.](image)

**Figure 2.15:** Circuit schematic of a single stage VGA.

<table>
<thead>
<tr>
<th>Device</th>
<th>Q₁</th>
<th>Q₂</th>
<th>Q₃</th>
<th>Q₄</th>
<th>Q_C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Size ($\mu$m)</td>
<td>2X15</td>
<td>4X50</td>
<td>2X25</td>
<td>2X15</td>
<td>4X50</td>
</tr>
<tr>
<td>Comp.</td>
<td>$R_S$</td>
<td>$C_C$</td>
<td>$C_{cc}$</td>
<td>$C_{IN}$</td>
<td>$C_{OUT}$</td>
</tr>
<tr>
<td>Value</td>
<td>150 $\Omega$</td>
<td>5.25 pF</td>
<td>6 pF</td>
<td>6 pF</td>
<td>4.5 pF</td>
</tr>
</tbody>
</table>
Table 2.2 summarizes the size and type of the major components used in the design. Fig. 2.16 shows the micro-photograph of the circuit. The combined occupied area is around 1.2×1.4 mm². Necessary decoupling networks has been used in the drain bias to suppress unwanted oscillations. This is usually done with a high value of decoupling capacitor and a small resistor in the bias line. A 6.7 nH spiral inductor together with a 100 Ω resistor used at the gate network of the VGA serves the purpose of providing DC supply as well as to improve the input matching. A small rectangular inductor (0.636 nH) has also been used at the gate as part of the matching network. The total DC power consumption is 75 mW out of which 10 mW is consumed by the source follower.

Results and analysis: Single stage VGA

Parameters of interest are the scattering matrix, both as a function of frequency and control voltage, $V_{\text{con}}$. Compression characteristics, on the other hand, is analyzed to study the power response and its influence on gain variation. Investigation is also carried out about the dependence of IP3 on gain variation.

Figure 2.17 shows the measured gain with $V_{\text{con}}$ as parameter. Variation of gain is achieved by the gate voltage ($V_{\text{con}}$) applied to the gate of the control transistor. The gain is almost flat in a bandwidth (BW) greater than 4 GHz. The curves with different control voltages are parallel to each other which is a sign that the control
voltage is not influencing the bandwidth much. For a lower value of \( V_{\text{con}} \), a higher source resistance is induced to the source network of the VGA. The smaller the control voltage, the higher the channel resistance, \( R_{ds} \). This, when coupled to the source resistance \( R_s \), gives a high equivalent impedance, \( Z_X \). The ultimate consequence is the reduction in gain. This is evident from equation (2.2) and Fig. 2.14.

Fig. 2.18(a) shows a gain variation range of 13 dB measured at the center frequency for various control voltage. The strongest variation lies in the region of -1.25 to -0.75 V. Gain sensitivity of the VGA

**Figure 2.17:** Measured \(|S_{21}|\) as a function of frequency with \( V_{\text{con}} \) as parameter.

**Figure 2.18:** (a) Variation of \(|S_{21}|\) with \( V_{\text{con}} \) (b) Rate of change of gain variation with \( V_{\text{con}} \).
i.e. the rate of change of gain variation with respect to the control voltage is plotted in Fig. 2.18(b). A maximum value of 61 dB/V is achieved at a $V_{\text{con}}$ value around -1 V. Linearity is a parameter to measure the suppression of the unwanted signals. If a weak RF signal is accompanied by two closely spaced strong interferers, its highly likely that the IM products of the interferers will fall in the pass band of the desired RF signal at the output of the amplifier. The ratio (in dB) of the RF signal to the IM product is given by [38]:

$$ IR = RF + 2 \cdot IIP3 - 3 \cdot INT $$

(2.3)

Where RF is the wanted signal strength in dBm at a certain frequency, IIP3 is the input referred IP3 of an amplifier in dBm at that frequency, INT is the signal strength of two closely spaced interferers expressed in dBm. Since at the receiver end, we don’t have enough freedom to strengthen the receiving RF signal or suppressing the adjoining interferers, the most effective way to maximize IR is to maximize the input IP3 of the concerned amplifier. For instance, if a weak signal of -60 dBm is accompanied by two strong interferers with a strength of -30 dBm each and if they are passed through an amplifier having an IIP3 of -10 dBm, the output RF signal will be 10 dB stronger than the IM products. A flat profile of IIP3 with respect to gain variation is always deserved. Fig. 2.19 shows the dependance of IP3 on the control voltage and the gain variation. Maximum deviation of measured IIP3 is less than 2 dB for a 10 dB gain variation.

Finally, the port reflections are shown in Fig. 2.20. Use of source follower ensures an unaffected (with gain) and well matched (better than -15 dB) output profile. However, the circuit is not well matched at the input. In reality an LNA will be used at the input of the
2.4. CIRCUIT IMPLEMENTATION

Figure 2.20: Port reflections versus frequency for various control voltage (a) $|S_{22}|$ and (b) $|S_{11}|$.

VGA which will give an optimized input match as well as low NF. This feature has been investigated in the subsequent sections while implementing the multistage VGA.

2.4.2 Multistage VGA

Based on the topology discussed in section 2.3 and the corresponding single stage VGA implementation in section 2.4.1, the multistage VGA has been realized by cascading three single stages together. Fig. 2.21 shows the circuit schematic. It is virtually a composition of three single VGA units together with an LNA at the input and a source follower at the output. Each of the VGA units has the same design structure as described in section 2.4.1. Contribution from the transmission line, together with the coupling capacitor and the gate networks, provided the interstage match.

Table 2.3: Major comp. used in Fig. 2.21

<p>| | | | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>$Q_L$</td>
<td>2X15 $\mu$m</td>
<td>$L_{cl}$</td>
<td>5.3 nH</td>
<td>$C_{p3}$</td>
</tr>
<tr>
<td>$Q_A$</td>
<td>4X50 $\mu$m</td>
<td>$L_{cg}$</td>
<td>6.7 nH</td>
<td>$R_w$</td>
</tr>
<tr>
<td>$Q_S$</td>
<td>2X25 $\mu$m</td>
<td>$L_{g}$</td>
<td>1.2 nH</td>
<td>$C_{cc}$</td>
</tr>
<tr>
<td>$Q_N$</td>
<td>4X100 $\mu$m</td>
<td>$L_{gg}$</td>
<td>0.67 nH</td>
<td>$C_{out}$</td>
</tr>
<tr>
<td>$Q_W$</td>
<td>2X15 $\mu$m</td>
<td>$C_{p1}$</td>
<td>5.46 pF</td>
<td>$C_{in}$</td>
</tr>
<tr>
<td>$Q_C$</td>
<td>4X50 $\mu$m</td>
<td>$C_{p2}$</td>
<td>6 pF</td>
<td></td>
</tr>
</tbody>
</table>

Table 2.3 summarizes the major components used in the circuit schematic of Fig. 2.21. In many applications, for an IF-amplifier following a receiver mixer, low noise figure is of utmost importance. This demand of low noise figure intensifies further if the gain becomes a varying quantity. For a feedback VGA, variation of the control element influences the input port reflections which ultimately affects
the NF. A 12 dB gain variation from a single stage VGA (coupled with a source follower at the output) can give as much as as 10 dB variation in NF [39] when designed without considering the noise factor into account. With a number of stages cascaded together and with the increase of range of gain variation, this scenario deteriorates even further, specially when the gain becomes negative.

A high noise, can substantially reduce Spurious Free Dynamic Range (SFDR) to a minimum level. SFDR is defined as the ratio of the maximum input signal level that a circuit can tolerate to the minimum input signal level at which the circuit provides a reasonable signal quality. As far as VGA is concerned, it gives an estimation of the maximum relative level of interferers that the VGA can handle while producing an acceptable signal quality for a weak input signal [38].

Mathematically:

$$SFDR(dB) = \frac{2}{3} [IIP_3 - NF + P_{kT} - 10\log_{10}(BW)] - SNR_{min} \tag{2.4}$$

Where $IIP_3$ is the input third order intercept point expressed in dBm, $NF$ is the noise figure expressed in dB, $P_{kT}$ is the thermal noise power expressed in dBm (-174 dBm/Hz) and $BW$ is the system bandwidth in Hz. It is seen from the above equation that NF and IP3 exercise substantial contribution to maintain the SFDR level. This demand on NF and IP3 becomes even more critical with the increase of number of cascaded stages. With a low level of SFDR due to the noise contributed by the VGA, overall detection of the weak signal by the ADC becomes almost impossible. One effective solution is to use a low noise amplifier at the input of the VGA. The overall NF, though
not remains constant as required by the equation, improves considerably with a lower minimum value and a lower NF variation.

Table 2.3 shows the size of both the active and passive elements used to realize the LNA. The NF is optimized by trade-off with the input matching for a given device size, associated gain and the bias. Source degeneration technique has been used for simultaneous input match and noise optimization [40]. Fig. 2.22 explains the dependence of associated gain, noise resistance ($R_n$) and DC power consumption on device width ($W$) of a pHEMT for a low noise biased at 2.5 GHz. The noise figure of a two-port system is linearly proportional to the noise resistance and therefore has inverse relationship with the gate width [Fig.2.22(b)]. For a proposed limit of NF and DC power consumption, a 400 $\mu$m (4\cdot100) pHEMT was chosen for the LNA. Once the device size has been chosen, the inductors at the gate, drain and source terminals were determined by optimization for a lowest possible NF.

The output of the multistage VGA is coupled with a source follower having the same device size, component values and power consumption as used for implementing the single stage VGA as described in section 2.4.1. The main aim of using SF at the output is to achieve active load match by proper scaling of the transistors. In addition, the source follower prevents the output from loading the drain of the last amplifier stage. Fig. 2.23 shows the microphotograph of the multistage VGA. The total occupied area by the circuit containing
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Figure 2.23: Microphotograph of a three stage VGA (enclosed by the dotted line) coupled with an LNA. To save the die area, two circuits are placed on the same chip.

the multistage and the single stage VGA is $3.5 \cdot 3 \text{ mm}^2$.

Results and analysis-Multistage VGA

$S_{21}$, noise figures, power compression, third order intercept point (IP3) are the most interesting parameters to look into. An Agilent PNA (E8361A) has been used to measure the S-Parameters while the noise figure (NF) was measured with an Agilent 8974 noise figure analyzer. To measure the Power compression and IP3, an Agilent 4419B power meter and Agilent 8565 E spectrum analyzer have been used. Fig. 2.24 shows the measured gain ($S_{21}$) with the control voltage as parameter. Legend shows the corresponding control voltage for each of the gain curve. The -3 dB bandwidth is approximately 800 MHz. The simulated $S_{21}$ based on the foundry model is superimposed on the measured plots (dotted lines) and can be seen to have a good correspondence.

Figure 2.25(a) shows the gain variation plotted against the control voltage, $V_{con}$ at 2.5 GHz. The gain variation is more than 45 dB with a maximum value of 47 dB. A gradual variation of gain with a lower slope is always expected. A high sensitive gain profile gives a
sharp transition between the maximum and the minimum gain making the gain control very much sensitive to $V_{\text{con}}$. To study the gain control sensitivity, the rate of change of gain variation with respect to the control signal is plotted in Fig. 2.25(b). The maximum gain control sensitivity is approximately 152 dB/V.

Reflection coefficients in the highest and lowest gain modes are plotted in Fig. 2.26(a) and in Fig. 2.26(b). Use of source follower ensures a good match at the output port. Some variations at the input port can be seen, though. This is expected, since the variation of the feedback element at the source of each of the VGA units causes the input impedance to be affected in the same manner.

The main aim of the IF VGA is to maintain a minimum signal level for detection by the ADC. One way of investigating this necessity is to study SFDR and its influence on gain variation. A flat profile is always desired and it is expected to have minimum influence on gain variation. From mathematical formulation given in equation (2.4), it is seen that SFDR depends on input IP3 and NF. It is therefore important to study their behavior and to estimate their dependence on gain variation. The plot of the experimental NF is shown in Fig. 2.27. A minimum value of 0.82 dB is obtained in the
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Figure 2.25: (a) Variation of $|S_{21}|$ with $V_{\text{con}}$ (b) Rate of change of gain variation with the control voltage.

Figure 2.26: Variation of port reflections with $V_{\text{con}}$ (a) $|S_{11}|$ (b) $|S_{22}|$.

Figure 2.27: (a) NF with sweeping frequency for various control voltage (b) NF vs. control voltage measured at 2.5 GHz.
highest gain mode. In the lowest gain mode this value is 5.5 dB. The total variation is less than 5 dB making the NF less prone to high gain variation. The influence of IP3 on the control voltage and gain variation is shown in Fig. 2.28. The input IP3 is shown to have influenced by the gain variation in the reverse order. This is expected since IIP3 of a multistage configuration (Fig. 2.29) is given by:

\[
IIP3_{\text{tot}} = \frac{1}{IIP3_1} + \frac{1}{IIP3_2 + \text{Gain}_1 \cdot IIP3_3 + \text{Gain}_2} + \ldots = \frac{1}{\sum_{i=1}^{N} \prod_{j=i+1}^{N-1} \text{Gain}_j IIP3_i}
\]  

(2.5)

\[\text{Figure 2.29: Input IP3 of cascaded systems.}\]

Quantities used in the equation are in absolute numbers and \(G_0 = 1\) for \(j=0\). Thus with each stage in a cascade configuration with a gain greater than unity, the nonlinearity of the latter stages becomes increasingly more critical because the IP3 of each stage is effectively scaled down by the total gain preceding that stage. Fig. 2.30 shows the calculated variation of IIP3 for a two stage VGA. Each of the gain stages has an IIP3 of -5 dBm and the first stage offers a gain
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Figure 2.30: Calculated variation of IIP3 with gain based on equation (2.5) for a typical two stage VGA (a) VGA block (b) IIP3 variation with gain.

Figure 2.31: Variation of SFDR with (a) $V_{\text{con}}$ and (b) Gain.

variation of 15 dB. The corresponding IIP3 variation is around 12 dBm.

In order to fully comprehend the impact of IP3 on the VGA performance, we study the dependence of SFDR on the gain variation considering the VGA having a minimum SNR of 10 dB. Fig. 2.31 shows the calculated SFDR based on equation (2.4). Measured values of NF and IIP3 shown in Fig. 2.27-2.28 are used in the calculation. The VGA has a bandwidth of 0.8 GHz centered at 2.5 GHz. The minimum output SFDR, in the highest gain mode, is 14 dB, approximately. So for a small IF input level, the VGA gives a tolerance margin of 14 dB from the interferers while producing an acceptable signal level for the ADC.
2.5 Parallel feedback VGA

This section represents the design and characterization of a parallel feedback VGA. The aim is to maximize the gain, range of gain variation with minimizing the NF as well as IIP3 variation. A comparative investigation will also be carried out with the series feedback VGA together with some of the published works based on this topology.

2.5.1 Theory

Fig. 2.6(b) shows the basic circuit topology for implementing the parallel feedback VGA. The modified schematic replacing the variable component with a control transistor, is shown in Fig. 2.32(a). From the corresponding small signal model of Fig. 2.32(b) it is seen that the variable impedance, $Z_X$ is similar to the one given in equation (2.1) except the source resistance $R_s$. The modified $Z_X$ is given by:

$$Z_{eq} = \frac{1 + sR_{dsc}(C_{eq} + C_{cc})}{sC_{cc} + s^2R_{dsc}C_{eq}C_{cc}}$$

(2.6)

$C_{cc}$ is the coupling capacitor which should be rather large and $C_{eq}$ is the equivalent capacitor as explained in equation (2.1). The corresponding voltage gain for a load of $Z_L(=1/Y_L)$:
\[
AV = \frac{V_{out}}{V_{in}} = \frac{-g_m + s\delta + s^2\beta}{g_{ds} + Y_L + s\lambda + s^2\psi}
\]  

(2.7)

where,
\[
\delta = -g_m R_{dsc} (C_{eq} + C_{cc}) + C_{gd} + C_{cc}
\]
\[
\beta = R_{dsc} [C_{eq} C_{cc} + C_{gd} C_{eq} + C_{cc}]
\]
\[
\psi = R_{dsc} [C_{eq} C_{cc} + (C_{gd} + C_{ds}) (C_{eq} + C_{cc})]
\]
\[
\lambda = R_{dsc} (Y_L + g_{ds}) (C_{eq} + C_{cc}) + C_{gd} + C_{ds} + C_{cc}
\]

The voltage gain for the circuit configuration of Fig. 2.32 has been plotted in Fig. 2.33 considering the parasitic elements mentioned in Table 2.1. A 50 Ω load has been considered.

![Graph showing calculated and simulated voltage gain for sweeping R_{dsc}](image)

**Figure 2.33:** Calculated (circled) and simulated (solid) variation of voltage gain for sweeping \(R_{ds}\) at 2.5 GHz verifying the accuracy of the expression of equation (2.7). Component used in the calculation and simulation have been tabulated in Table 2.1.

### 2.5.2 Design

Fig. 2.34 shows the schematic of the multistage parallel feedback VGA. The corresponding micro-photograph is shown in Fig. 2.35.
The circuit has two VGA units with a low noise amplifier (LNA) at the input and a source follower at the output. As described in section 2.4.2, the LNA is designed with inductive source degeneration technique. A 400 μm, 4 fingers mHEMT has been used with a drain supply of 1.6 V that consumes around 107 mW of DC power. Of the total DC power (140 mW) consumption, the bulk is consumed by the LNA. The two VGA units consume a total 30 mW from a 1.3 V drain supply. Table 2.4 summarizes some of the major component values used to realize the circuit.

Table 2.4: Major comp. used for PF VGA [Fig. 2.34]

<table>
<thead>
<tr>
<th>Component</th>
<th>Value</th>
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<tbody>
<tr>
<td>Q1</td>
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<tr>
<td>Q2</td>
<td>4X50 μm</td>
</tr>
<tr>
<td>Q3</td>
<td>2X50 μm</td>
</tr>
<tr>
<td>Qc</td>
<td>2X25 μm</td>
</tr>
<tr>
<td>Ld</td>
<td>9 nH</td>
</tr>
<tr>
<td>Lg</td>
<td>6 nH</td>
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<tr>
<td>Cc</td>
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<td>Lx</td>
<td>5 nH</td>
</tr>
<tr>
<td>Ccc</td>
<td>10 nH</td>
</tr>
<tr>
<td>C1</td>
<td>0.6 nH</td>
</tr>
<tr>
<td>Lv</td>
<td>6 nH</td>
</tr>
<tr>
<td>Rg</td>
<td>1.5 kΩ</td>
</tr>
<tr>
<td>Crf</td>
<td>5 pF</td>
</tr>
</tbody>
</table>

Figure 2.34: Schematic of the parallel feedback VGA.

2.5.3 Result: Comparative investigation with the series feedback VGA

Fig. 2.36 shows the measured variation of gain with V_con as parameter. The dotted lines show the simulated values. The control voltage is varied from -1 to -0.45 V with a step of +0.05 V. The gain
CHAPTER 2. VARIABLE GAIN AMPLIFIER

Figure 2.35: Microphotograph of the parallel feedback VGA. The circuit area is 4.5 mm x 2.5 mm.

varies from 36 to -15 dB. The measured bandwidth is 0.7 GHz, approximately. The circuit remains stable for all applied gate (control) voltage in the measured frequency band in concern. For the series feedback VGA, $V_{con}$ varies from -1.7 to -0.75 V with the same resolution of +0.05 V. The per-stage gain of both the VGA’s is comparable i.e. about 12 dB/stg. The series feedback topology has three gain control units whereas the parallel feedback VGA has two. Overall gain control range is better for the parallel feedback VGA.

Fig. 2.37(a) shows the gain variation of the VGA’s at the center frequency with respect to the control voltage. When compared to the corresponding plot of series feedback VGA of Fig. 2.25(a), it gives higher gain variation range though the series feedback VGA offers higher maximum gain. To study the dependence of gain variation with the control signal, the rate of change of gain variation with $V_{con}$ is plotted in Fig. 2.37(b). It is a measure of sensitivity of the gain variation with the control signal. The lower the values, the less is the sensitivity. When compared to the concerned plot of series feedback VGA of Fig. 2.25(b), the higher maximum value (187 dB/V) obtained by the parallel feedback VGA confirms its greater sensitivity to the control signal than its counterpart.

Plots of reflection coefficients are shown in Fig. 2.38. When compared to Fig. 2.26, the series feedback VGA gives better performance. The source follower in the series feedback VGA is designed in self-bias mode with a current source at the source terminal. The
same design procedure is however, not followed for the source follower of the parallel feedback VGA. Some variations at the input port ($S_{11}$) can be noticed as well. Variation of the control voltage causes the feedback element to vary which ultimately affects both the NF and the input reflections. Use of a second stage of LNA preceding the VGA will minimize this effect but at the cost of area, power and linearity.

The NF performance is shown in Fig. 2.39. For the highest gain mode, the measured NF at 2.5 GHz is 0.86 dB. This value is higher than the series feedback VGA under similar gain condition. The total NF variation is around 23 dB for a gain variation of 55 dB. This is shown in Fig. 2.39(b) where the measured NF is plotted against the sweeping control voltage, $V_{con}$. This excessive variation of NF is mainly due to the negative gain swing. The minimum achievable gain is lower than -20 dB (20 dB loss). This causes excessive noise contribution when compressing a strong signal. The series feedback VGA is, however, immune to this problem. The maximum NF variation is less than 6 dB for a gain variation of 45 dB. In the whole range of gain variation, the minimum gain offered by the series feedback VGA is close to unity. This has the advantage of gaining low NF under compressed gain condition. Sensitivity profile with regards to frequency is better for the series feedback VGA. It has flatter fre-
Figure 2.37: (a) Variation of $|S_{21}|$ with $V_{\text{con}}$ (b) Rate of change of gain variation with $V_{\text{con}}$.

Figure 2.38: Variation of port reflections with $V_{\text{con}}$ (a) $|S_{11}|$ and (b) $|S_{22}|$.

Figure 2.39: (a) NF versus frequency for various control voltage (b) Variation of NF with the control voltage at 2.5 GHz.
2.5. PARALLEL FEEDBACK VGA

Figure 2.40: (a) Variation of IP3 with $V_{\text{con}}$ (b) Dependence of IP3 with gain.

Figure 2.41: (a) Variation of NF with gain (positive gains only) for both the VGAs (b) IIP3 variation with gain.

quency response [Fig. 2.27(a)] than that of the parallel feedback VGA. To compare the NF variation with gain, it is plotted against the gain variation and is shown in Fig. 2.41(a) for both the VGAs. In the highest gain mode, the series feedback VGA shows better result. For moderate positive gain range, the parallel feedback VGA gives a slight better performance. Fig. 2.40 shows the IIP3 variation with the control voltage and gain. A 35 dB of gain variation introduces an IIP3 variation of 25 dBm. However the IIP3 values for a certain gain is higher for parallel feedback VGA than that of the series feedback VGA.

To fully comprehend the linearity of the proposed VGAs based on the two topologies, we study the impact of nonlinearity on SFDR for each of them. Using the measured data of IP3 and NF as described above, SFDR for both the VGA is calculated based on equation (2.4)
Figure 2.42: SFDR variation with gain and control voltage for both the VGAs. (a) SFDR versus gain (b) SFDR versus $V_{\text{con}}$. Plot with triangle $[\Psi]$ shows the work from [15].

considering a 10 dB SNRmin. The bandwidth for the series feedback VGA is 0.8 GHz whereas for the parallel feedback VGA it is 0.7 GHz. Considering an IF bandwidth of 0.7 GHz, the SFDR for both the designs are plotted again the gain variation and the control signal. Fig. 2.42(b) shows the variation of SFDR with respect to the control voltage $V_{\text{con}}$. Higher SFDR is achieved for the parallel feedback VGA for a certain control voltage. The same figure is plotted with respect to sweeping gain in Fig. 2.42(a). SFDR for the parallel feedback VGA is better in the low gain region. For high gain its value is comparable for both the topologies. To compare the work with the published literature, SFDR for the work from [15] has been plotted. This will be discussed in further details in section to follow.

Virtually it is the weak signal that needs high gain from the VGA. A low value of SFDR of the VGA means its vulnerability to the interferers of the adjacent channels or unwanted signals. This is particularly critical for systems that operate in the low frequency regions. The parallel feedback VGA gives better performance in this scenario. On the other hand, systems operating in the high frequency regions particularly in the millimeter wave or beyond, usually, are less prone to adjacent channel suppression and therefore, the series feedback VGA can be a good choice. Table 2.5 shows a comparative summary between the two designs. To clearly distinguish between the two VGAs, both the weak as well as the strong signals are considered in Table 2.6.
Table 2.5: Comparative summary between the Series Feedback (SF) VGA and the Parallel Feedback (PF) VGA

<table>
<thead>
<tr>
<th>Parameter</th>
<th>SF</th>
<th>PF</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain/stg.</td>
<td>≈</td>
<td>≈</td>
</tr>
<tr>
<td>Gain variation range</td>
<td>-</td>
<td>+</td>
</tr>
<tr>
<td>Max. gain</td>
<td>+</td>
<td>-</td>
</tr>
<tr>
<td>Max. variation rate</td>
<td>-</td>
<td>+</td>
</tr>
<tr>
<td>Input matching</td>
<td>≈</td>
<td>≈</td>
</tr>
<tr>
<td>Output matching</td>
<td>+</td>
<td>-</td>
</tr>
<tr>
<td>BW</td>
<td>+</td>
<td>-</td>
</tr>
<tr>
<td>DC power/stg</td>
<td>+</td>
<td>-</td>
</tr>
<tr>
<td>Area</td>
<td>-</td>
<td>+</td>
</tr>
</tbody>
</table>

Table 2.6: Comparison on RF properties between the two VGA in the strong signal and weak signal conditions

<table>
<thead>
<tr>
<th></th>
<th>Strong signal</th>
<th>Weak Signal</th>
</tr>
</thead>
<tbody>
<tr>
<td>NF</td>
<td>SF</td>
<td>≈</td>
</tr>
<tr>
<td>$P_{-1dBmix}$</td>
<td>PF</td>
<td>PF</td>
</tr>
<tr>
<td>$P_{-1dBout}$</td>
<td>SF</td>
<td>SF</td>
</tr>
<tr>
<td>IIP3</td>
<td>PF</td>
<td>PF</td>
</tr>
<tr>
<td>OIP3</td>
<td>PF</td>
<td>PF</td>
</tr>
<tr>
<td>SFDR</td>
<td>PF</td>
<td>PF</td>
</tr>
</tbody>
</table>

2.6 Comparison with the published works

Most of the design works done on VGA, are aimed at attaining high range of gain variation without giving much attention to achieving high value of maximum gain. For a V band receiver with an IF block working at S band, attaining a high gain is as much important as that of high range of gain variation. In this respect, the series feedback VGA stands out of the contemporary works published so far in the literature. Table 2.7 summarizes some of the works worth mentioning on variable gain amplifier operating in the S band. Work based on utilizing FET as an attenuator in a half T arrangement in front of a small signal amplifier reported by Detratti [33] claimed a gain variation range of 40 dB from three cascaded stages with a maximum gain of 18 dB. Variation of IP3 with the control parameter is evident from the gain plots. Though noticeable deviation around the pinch-off voltage of the control FETs have been acknowledged, no clear explanation is given in this regard. The measured NF is 6.3 dB in the highest gain mode (18.8 dB) which is rather large for a pHEMT device.

Work proposed by Wang [17] based on cascode arrangement (section
### Table 2.7: Comparison with the published literature

<table>
<thead>
<tr>
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<th></th>
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<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>[33]</td>
<td>1.95</td>
<td>2</td>
<td>0.4</td>
<td>40</td>
<td>18.8</td>
<td>22.1</td>
<td>0.2µm pHEMT</td>
</tr>
<tr>
<td>[15]</td>
<td>2.5</td>
<td>3</td>
<td>4.3</td>
<td>35</td>
<td>24</td>
<td>18</td>
<td>GaAs HBT</td>
</tr>
<tr>
<td>[17]</td>
<td>5.7</td>
<td>1</td>
<td>0.6</td>
<td>8</td>
<td>16.4</td>
<td>—</td>
<td>0.18µm CMOS</td>
</tr>
<tr>
<td>[41]</td>
<td>5.2</td>
<td>3</td>
<td>1.5</td>
<td>20</td>
<td>20</td>
<td>—</td>
<td>0.18µm CMOS</td>
</tr>
<tr>
<td>[34]</td>
<td>3.5</td>
<td>1</td>
<td>&lt;1</td>
<td>15</td>
<td>7</td>
<td>—</td>
<td>0.3µm GaAs</td>
</tr>
<tr>
<td>Φ&lt;sup&gt;a&lt;/sup&gt;</td>
<td>2.5</td>
<td>3</td>
<td>0.7</td>
<td>55</td>
<td>35</td>
<td>14</td>
<td>0.15µm pHEMT</td>
</tr>
<tr>
<td>Ψ&lt;sup&gt;b&lt;/sup&gt;</td>
<td>2.5</td>
<td>4</td>
<td>0.8</td>
<td>45</td>
<td>47</td>
<td>3</td>
<td>0.15µm pHEMT</td>
</tr>
</tbody>
</table>

<sup>a</sup> This work: Three gain stages parallel feedback VGA

<sup>b</sup> Ψ This work: Four gain stages series feedback VGA

2.1.2) using 0.18 µm CMOS at 5.7 GHz claimed a gain variation of 8 dB from a single stage with highest gain 16.8 dB and lowest NF of 3.5 dB. No information on compression characteristics was provided. Work by Ming Da [41] utilizes a folded cascode topology to design the VGA. Of the three gain stages, the one in the middle contributes to gain variation by controlling the gate supply to the pMOS. The achieved gain variation range is 40 dB with the maximum gain of 20 dB from three cascaded stages. The minimum NF is 3.5 dB in the highest gain mode. No information is provided on the linearity performance on gain variation. Work reported by Yong [42] claims to have a gain variation of 28 dB at 2.4 GHz with maximum gain of 19 from two gain stages. The first stage is the LNA and second stage is the parallel feedback VGA. Maximum NF is 2.1 dB in the highest gain mode. The figures are, however, based on simulations and have not been verified by measurements.

Among some early works from the mid 90’s the one by Kobayashi [15] is worth mentioning. He based his work of VGA on current steering technique. The work systematically outlines some possible topologies with their merits and demerits. Table 2.7 highlights the main features of the work. Based on the provided information, SFDR of the work is plotted against the gain variation considering an IF bandwidth of 0.7 GHz and is plotted in Fig. 2.42(a). The proposed work of the parallel feedback VGA shows better result with flatter profile for the given gain variation.

### 2.7 Investigation with other technology

As part of the investigation with different technology, the variable gain amplifier is studied with 45 nm CMOS. The source feedback
topology discussed in section 2.1.4 has been used to implement the single stage VGA. As measurement data is not available during the time of writing this thesis, investigation is carried out based on simulations only. Detailed about the technology and the model are discussed in Chapter two.

![Detailed schematic of the 45 nm CMOS VGA.](image)

**Figure 2.43:** Detailed schematic of the 45 nm CMOS VGA.

The circuits consumes around 9 mW and gives a gain variation around 9 dB at 2.5 GHz. The high Q value of the above IC (WLP) Inductors are suitable for terminal matching. The occupied area, on the contrary, becomes larger. The big decoupling capacitor (10 pF), $C_{cc}$, is also responsible for area enlargement.

### 2.7.1 Simulated Performances

From the simulated plots of Fig. 2.44-2.46, it can be seen that a gain variation of 9 dB is achieved at 2.5 GHz with a maximum gain of around 13 dB. Both The input and the output gives good matching irrespective of the gain variation and remains below -15 dB in all the whole gain swing. NF variation with the gain is also minimum i.e. around 1.5 dB for a 9 dB gain variation. Since, SFDR is a function of NF, this small dependence of NF on gain ensures an SFDR almost independent of gain variation.

The main disadvantages is the area occupied by the circuit. Given the freedom of the die area, the main effort was given to achieve a
CHAPTER 2. VARIABLE GAIN AMPLIFIER

Figure 2.44: (a) $S_{21}$ versus frequency (b) $S_{21}$ versus $V_{\text{con}}$.

Figure 2.45: (a) $S_{11}$ versus frequency (b) $S_{22}$ versus frequency.

Figure 2.46: Simulated NF and gain sensitivity (a) NF versus $V_{\text{con}}$ (b) $dS_{21}/dV_{\text{con}}$ versus $V_{\text{con}}$. 
working design with the port matched to 50 Ω and minimum NF variation. The main idea was to study the feasibility of the series feedback topology in 45 nm CMOS. Virtually, its the passives and the above IC inductors that occupy the bulk of the area which is around 3.2 mm². If however, the inductors are designed in the back end, a size reduction as much as 50% can be achieved. This comes with the trade-off with the noise and gain performance of the amplifier.

2.8 Discussion and Future Work

The thesis discusses the performances of two high controllable gain VGA with high maximum gain and low noise figure. Two approach of feedback topology namely, the series feedback and parallel feedback have been investigated. Detailed comparison between the working circuits are outlined in section 2.5.3 and summarized in Table 2.5-2.6. Also, a brief comparison with the published work has also been carried out in section 2.6 and is summarized in Table 2.7.

The following points are worth summarizing:

1. Series feedback VGA gives the best performance when it comes to achieving high controllable gain together with high maximum gain.

2. Variation of input IP3 with gain should be kept as minimum as possible. Its inevitably inherent in a multistage configuration as explained by eqn. 2.5.

3. The same is true for NF for a multistage VGA. In a cascaded amplifier, the NF in each of the stages is scaled down by the gain of the previous stage before being added to the NF of that stage. So, a variation in gain in one of the stages causes the NF to vary but in the inverse order. And, if instead of gain, the VGA introduces attenuation (loss), the overall NF becomes excessively high. This is evident from Fig. 2.39(b) of the parallel feedback VGA.

4. Linearity degradation can be attributed to other reasons apart from eqn. 2.5 specially for a feedback amplifier. In a crude approximation, with the simplest amplifier configuration, IP3 is related to the shape of the $g_m$ curve of the active device [43]. This dependence on $g_m$ makes IP3 susceptible to vary with gain. In a feedback amplifier, the effective $g_m$ has functional dependence on the feedback element. For instance in a commons source, series feedback amplifier, the effective transconductance at dc is given by:
\[ G_m = \frac{g_m}{1 + g_m R_s} \]  

(2.8)

Variation of \( R_s \) causes \( G_m \) to vary in the same manner which in essence, implies a functional dependance of IP3 on feedback component. This can be a possible explanation for the IP3 variation with gain in a series feedback VGA.

5. NF variation has been minimized by using an LNA stage in front of the VGA. This variation can further be reduced i.e. the NF can be made almost independent of gain variation if there is an isolation between the VGA and the LNA. A carefully designed source follower may serve the purpose of an isolation stage. IP3 will still remain dependent on the gain variation. This parameter, however, will have less significant effect on SFDR if the linearity of the VGA can be improved considerably. Though numerous techniques to enhance IP3 of an amplifier can be found in the literature [44], [45], [46], [47], none has been investigated for a feedback VGA.

2.9 Conclusion

The thesis demonstrates the implementation of two high gain, low noise variable gain amplifiers based on two distinct topologies with possible merits and de-merits between the two. Each of the designed VGA described in the thesis, is preceded by an LNA. Excellent NF has been obtained in both the circuits specially with the series feedback VGA. A NF variation of 5 dB has been measured for a 45 dB gain variation in case of the series feedback VGA. Comparable performance can be noticed [2.41(a)] as long as the gain of the parallel feedback VGA remains positive. The series feedback (SF) VGA is suitable for use in the high frequency receivers where the signals can be rather weak. Linearity on the other hand, is better achieved by the parallel feedback VGA. Systems requiring better demand on linearity for suppression of interferers or unwanted signals may find parallel feedback VGA more suitable.
Chapter 3

CMOS Millimeter-Wave Amplifiers

3.1 Background

Silicon based technologies particularly CMOS substantiated to be a viable choice for implementing high speed or low power wireless and wire line applications both from technical as well as economical point of view. Initially the applications were mainly limited to digital domain but with the increasing demand of wireless industries, CMOS has successfully proven its competence by implementing necessary RF circuitry and system operating below 10 GHz. The widely used low frequency spectrum, up to X band, is getting congested and it is likely to reach its saturation limit in the near future. Moving to the largely unused spectrum in the millimeter wave frequencies (and beyond) is the only effective solutions to avoid this channel congestion and interference. Applications in millimeter-wave frequencies for instance, at 60 GHz is gaining popularity because of the high absorption coefficient of $\text{O}_2$ molecule. The unlicensed 7 GHz contiguous bandwidth offered at 60 GHz has applications of point-to-point communications, wireless local area network (WLAN), short range high data rate wireless personal area networks (WPANS). Moving up the frequency in W band, interest in vehicular radar at 77 GHz has huge economic potential.

To meet the marketplace demands any solution has to be optimized with regards to cost, size and power. Operation in these frequency bands was once considered the exclusive domain of III-V-compounds due to their superior electron mobility, higher breakdown voltage and semi-insulating substrate. CMOS on the other hand, benefits from faster technology evolutions, higher integration and can offer
overall cost reductions in the volume productions specially when the already invested billion-dollar business is taken into account. In spite of these promising features, implementing CMOS based sub-circuits or a full fledged demonstrator in and around the millimeter-wave regions remains a topic of hectic research in the academia as well as in the industry. Some working CMOS circuits in the W band or V band [48], [49], [50], [51], [52] can be seen though. One of the key reasons may be attributed to unavailability of accurate modelling. The III-V devices are fabricated on semi-insulated substrate which makes it comparatively easy to eliminate the parasitics for proper modelling. CMOS on the other hand, is fabricated on conductive substrate and is prone to high parasitics. The passives suffer from low Q. Making a functional circuit in CMOS in high frequency is therefore, considered a big challenge for the researchers.

3.2 Device Structure

The simplest CMOS structure is fabricated on a silicon p-type substrate. For the nMOS, two heavily doped n-regions form the drain and the source terminal of the device. They are buried in a low doped p-well. A conductive piece of poly-silicon (poly) forms the gate contact and is insulated to the P-well by a thin layer of Silicon Di-Oxide (SiO$_2$). A high doped p-region builds the bulk connection. Shallow Trench Isolation is used to isolate the transistor from each other. This remains to be the very basic CMOS structures based on which new process are evolved with every generation of technology down-scaling.

The concept or the process of scaling down the gate of a transistor substantiated to be the most effective way of integrating high volume, low power and low cost CMOS digital circuitry. Historically device scaling remains the primary method by which the semiconductor industry has improved the productivity and performance. As far as RF applications are concerned, scaling defines one of the most important figure of merit of a transistor.

The unity current gain frequency $f_t$, reveals the ability of a transistor to work at high frequency. For a MOS device, $f_t$ is inversely proportional to the square of the gate length. So the possibility of making a high frequency RF/MMIC circuit becoming more and more realistic with the gradual down sizing of gate length. However, this continuous push of device dimension comes up with some of the new challenges and demands which necessitates introducing relevant pro-
cess modifications as well as coming up with new device structures. The multi gate fin shaped FET i.e. FinFET attracted much of the attention of the researchers of late. It offered a great relief to some of the most crucial issues pertaining to short channel effects (SCE) \[53\], an unavoidable phenomena resulting from gate shrinkage. Fig. 3.1 shows the simplified layout structure of a FinFET device.

The most prominent of the SCE i.e. the gate leakage is minimized in a FinFET device since the channel is no longer controlled by one side of the gate as with a planar bulk. It uses undoped channels \[54\], have no halo implants and therefore do not suffer from doping fluctuations. This minimizes threshold voltage (\(V_t\)) variation between the two adjacent but otherwise identical transistors, an important parameter for analog building blocks and ADC.

In the backdrop of above developments, the simple MOS structure no longer remained simple, rather became one of the most complicated processes with the introduction of the latest 45 nm technology node and beyond. The new architectures with new materials introduced new complexities with regards to modelling and circuit designs. Therefore, it turns out to be a challenging issue to make functional RFIC/MMIC circuitry using such a process. This second part of the thesis is therefore devoted to studying the matters pertaining to implementing high frequency MMIC small signal amplifiers utilizing 45 nm and 90 nm CMOS technology nodes. The study is carried out under the auspices of recently concluded IMPACT \[55\] project and the currently running NanoRF project. The Belgium based research foundry IMEC was responsible for processing the circuits and providing the device models. Some models were developed in -house as well and were used in the circuit analysis. In order to have a clear understanding about the technology, the following section is devoted to describing the technology in some detail.
3.3 Technology

Fig. 3.2 shows the 3D prototype of a cubic CMOS Process containing the Front-End-Of-Line (FEOL), the Back-End-of-Line (BEOL) and the Post Process (Wafer-Level Packaging, WLP) Layers. The process uses a p-type 20 Ω-cm silicon substrate as the bulk. FEOL houses the active device while the passives are implemented in the BEOL or the WLP layers.

In the 45 nm CMOS technology node, BEOL has only one wiring option available. It houses five metal layers each having a thickness of 0.5 µm except the first metal layer (M-I) which has a thickness of 300 nm. Contacts are made of tungsten. Each of the metal layers is buried inside a thick oxide layer with a theoretical permittivity ($\epsilon_r$) of 3.9. The tan$\delta$ of the dielectric is approximately equal to 0.07. The MIM capacitors and the thin film TaN resistors are fabricated between the second Metal layer and the third metal layer of BEOL. Fig. 3.3 shows the cross sectional view of the back end. The total BEOL thickness is around 4.3 µm.

WLP Cross section is shown in Fig. 3.4. It houses two metalization layers each having a thickness of 5 µm. The first metalization layer, WLP-M1 (Cu) is buried inside a thick layer of Benzo Cyclo Butane (BCB, $\epsilon_r$=2.65). BCB1 isolates WLP-M1 from the back end while a comparatively thinner layer of BCB2 protects the WLP-M1 from oxidation at the top. The electrical contacts to the underlying BEOL are connected using a high aspect ratio via (HARVi), with the via height-diameter ratio up to 1:1. The top metal (WLP-M2) makes the flow compatible with the standard wire bonding technology [56].

The thick above-IC dielectrics (BCB) lower the parasitic capacitance to the patterned ground shields and increase the inductor resonance frequency while thick Cu (transmission line) yields low series resistance [56], [57]. In essence WLP technology offers an opportunity of improving performances and functionalities of MMICs and RFICs by introducing high Q inductors and low loss transmission lines at high frequencies.

With the 90 nm CMOS technology node, BEOL, however, has two wiring options: one with WLP and the other without WLP. In the former case with WLP, BEOL has three metal layers each having a thickness of 0.625 µm separated by thick oxide layers. The WLP layer houses two metal layers (WLP-M1 and WLP-M2) each having
Figure 3.2: A 3D prototype of a 90nm CMOS with the Front End, Back End and the Post Process Layers. The figure is not drawn to scale.

WLP-M1 constitutes the signal line whereas WLP-M2, Cu/Ni/Au, creates the overpass. In the second wiring option, BEOL has five metal layers with the same thickness i.e. 0.625 µm.

The front-end shown in Fig. 3.2 contains the active structure i.e. the transistor. IMEC’s 45 nm CMOS process offers a minimum gate length of 45 nm for the active device. It is made on 20 Ω-cm p-type Si wafer. To electrically isolate the device from each other, Shallow Trench Isolation (STI) is used. In order to minimize the gate leakage, a common phenomenon of Short Channel Effect (SCE), the conventional silicon dioxide as dielectric is no longer used. Rather, a 1.4 nm Hafnium Oxide (HfO₂) or Silicon Oxynitridation (SiON) is used as the gate dielectric. The TaN/Poly stack is used as the gate electrode. Halos are implanted to locally increase the channel doping near the extension region. This minimizes the DIBL (Drain Induced
CHAPTER 3. CMOS MILLIMETER-WAVE AMPLIFIERS

Figure 3.3: Cross sectional view of the Back-End-of-Line (BEOL).

Figure 3.4: Cross sectional view of the Post Process (Wafer-Level Packaging, WLP) Layer.

Barrier Lowering) effect however, affects the gain due to lowering of the output conductance ($g_{ds}$) [58].
FinFETs were fabricated on Silicon-On-Insulator (SOI) wafer with 145 nm buried oxide thickness. Fin patterning resulted in fin heights of 60 nm and fin width of 20 nm. A high-k dielectric, HfO$_2$ with an effective oxide thickness of 1.9 nm has been used as gate dielectric. The gate consists of a thin layer of TiN.

Similar processing flows were adopted for the 90 nm CMOS with an effective gate length of 70 nm and oxide thickness of 1.5 nm. The TaN/Poly stack is used as the gate electrode and Silicon Oxynitridation (SiON) is used as gate dielectric.

### 3.4 Device Models

For circuit simulation and analysis the latest industry standard compact model, PSP [59], [60] has been used. The model includes gate resistance and the four substrate networks as shown in Fig. 3.5 for RF applications.

The scalability (i.e. number of cells, number of fingers, number of gate contacts—single or double, etc.) of the gate and the substrate network which are strongly layout dependant is not imbedded in the original model. This, however, does not pose a serious threat to the model accuracies at low frequencies. For high frequency applications specially in the millimeter-wave regions, introducing scalability to the substrate networks is a must. It has been incorporated in the original model and the modified version was used in circuit analysis. A detail study on standard CMOS model modifications with scalable substrate network can be found in [61] for further reference.

For FinFET, the compact model MM1 by NXP has been used as a core model (an empirical version of the physics based MM11 model).
with the introduction of extrinsic elements i.e. overlap capacitance, gate resistance and parasitic capacitance. Since scalability issues were not introduced to the extrinsic parasitics in the core model, a fixed device dimension \((W_f = 20 \text{ nm} \text{ and } h_f = 60 \text{ nm})\) was used for circuit implementation as well as analysis.

The non availability of device models from the processing foundry during the time of working with the 90 nm CMOS amplifiers, led to the development of an in-house model [62]. Its a scalable, empirical based model taking both the nonlinear and the small signal conditions (i.e. RF noise) into account. Further details on the models and the concerned applications can be found in [63] [64], [65].

### 3.5 Device Performance

#### 45 nm CMOS

One of the key parameter of interest is to study \(f_t\) and \(f_{\text{max}}\) [66], [67], [68], [69] of a transistor as far as RF applications are concerned. Both the parameters are considered a figure of merit for the device and give an estimation of the maximum operating frequency of the working circuits. In the subsequent sections of LNA designs, information of \(f_t\) will help in the estimation of the required current density for an optimum NF at a certain frequency. It is therefore, studied for the devices against the drain current. Fig 3.6 shows the extracted \(f_t\) of a 192 \(\mu\text{m}\) width bulk CMOS with an effective gate length of 45 nm. The device consists of 8 cells in total. Each of the cells has 8 fingers with gate width of 3 \(\mu\text{m}\). The current gain \(|h_{21}|\) of the devices is calculated from the measured S-parameters (de-embedded), and \(f_t\) is determined by extrapolating \(|h_{21}|\) using a slope of -20 dB/decade to the unity gain point. The maximum achieved \(f_t\) is about 210 GHz. The plots of Fig. 3.6 shows the potential of the 45 nm bulk CMOS for millimeter-wave functional circuits well above 100 GHz. Fig. 3.7 shows the extraction procedures.

\(f_{\text{max}}\) is defined as the frequency where the power amplification of a transistor becomes unity under consideration of an optimum matching both at the input as well as at the output. Extraction of \(f_{\text{max}}\) by extrapolation is rather cumbersome due to very small log scale above 200 GHz.
3.5. DEVICE PERFORMANCE

Figure 3.6: Extracted $f_t$ for 45 nm bulk CMOS for various drain voltage.

Figure 3.7: Extraction of $f_t$ from the measured data of 45 nm bulk CMOS.

FinFET

It is interesting to study $f_t$ of a FinFET when compared to that of a bulk of the same technology node. FinFET offers a high series resistance from the S/D extensions of the fins (of the order of hundreds of nanometer). The effective transconductance, $G_m$ is inversely proportional to the source resistance, $R_s$ [70]. This ultimately lowers the unity current gain frequency since $f_t$ of a device which is linearly proportional to its effective transconductance. Mobility degradation
along the side walls of the fins and additional fringing capacitance are also responsible for lowering the $f_t$ [58].

Fig. 3.8 shows the extracted $f_t$ of the FinFET. The maximum achievable value is around 70 GHz. It's interesting to see the ratio of $f_t$ between the bulk CMOS and FinFET. Fig. 3.9 shows the ratio against the drain current (mA/µm) for a drain voltage of 0.6 V. Several methods have been investigated [71] to increase $f_t$ of a FinFET. Since $R_s$ and $R_d$ are two of the main reasons, one way of lowering their values is to increase the fin width, $W_f$ [72]. However there
is a penalty of doing that since for an efficient suppression of the short channel effects, the fin width has to be decreased when the gate length is shrunk.

90 nm Bulk CMOS

Fig. 3.10 shows $f_t$ of the 90 nm bulk CMOS. The maximum achievable $f_t$ can be as much as 90 GHz. Based on this value of, it is therefore feasible to design a 40 GHz LNA which has been dwelt at length in section 3.7.1.

3.6 Passive structures

Passives play a vital role in defining the occupied area as well as RF performance while designing MMIC circuits. They are used in impedance matching, biasing, phase shifting, filtering and many other functions. Applications of passives and their use in MMICs are mostly governed by their sizes, RF performance and material properties. Extensive investigation on various passive structures and their RF properties can be found in the literature [29], [73], [74]. There are two types of passives that merit considerations: the distributed elements where the size are comparable to the wavelength of the center frequency and the lumped elements which are compact in size and are preferred for low frequency applications. Since the working frequencies of the designed amplifiers remain within or in the close
proximity to the millimeter-wave regions, distributed elements are given due precedence.

3.6.1 Microstrip Transmission Lines

Among the various types of transmission lines, the microstrip transmission line is widely used in the MMICs. Given the material and the thickness of a substrate, the transmission line loss and impedance depends on the geometry i.e. the width and the thickness. In the sub-micron CMOS process with several conducting layers in the back end as well as in the above-IC, substrate loss is minimized by shielding the thick Si bulk by the ground layer. In the current works of amplifier designs with the 45 nm and the 90 nm CMOS FET, both the back end and the WLP layers were used alike to implement the microstrip transmission lines. Fig. 3.11 shows the cross sectional view of micro-strip transmission lines. It has been shown that the measured line loss per unit length in the above IC is less than that in the back end. At 35 GHz the measured value is around 0.25 dB/mm for the WLP transmission line whereas in the back end, it is around -1.5 dB/mm at the same frequency [75].
3.6. PASSIVE STRUCTURES

3.6.2 Capacitors

Capacitors are one of the important elements in the MMIC/RFIC building block. They are widely used in the matching network or as a coupling or decoupling capacitor. In many of these applications, capacitor consume a large portion of the active circuit area. Therefore a high density capacitor is always preferred. For analog applications linearity and matching (between two adjacent capacitors) are considered the most important parameters while choosing a capacitor. For RF applications, on the other hand, high Q and high self resonance frequency (well above the operating frequency) are the two important parameters of interest. Given the guidelines above, the MIM cap were considered to be the right candidate for the amplifiers implementation in the 45 nm and 90 nm CMOS process.

MIM Cap

In the development of mm-wave amplifiers with the 45 nm CMOS, only the MIM capacitors were used whereas amplifiers with 90 nm CMOS used the multi-layer capacitor together with the MIM caps. The MIM capacitor is well known for its high density (higher capacitance per unit area) and compact layout structure. Fig. 3.12 shows the simplified cross section of a MIM structure. The MIM electrodes consists of two thin (∼50 nm) TaN layers which are placed between the second metal and the third metal separated by a short distance (∼35 nm). Silicon-Di-Oxide works as the dielectric.

The Q factor of the MIM structure is low (around 10 at 20 GHz for an area of 100 µm² [75]) and therefore is not very promising for
MMIC circuits. It also affects the yield factor since the thin dielectric is very susceptible to mechanical strain and prone to developing pinholes during process run. The multi finger structure though gives better Q factor (15 for the same area and frequency), still remains vulnerable to mechanical ruptures [65].

**Multilayer Capacitor**

The multi-layer structure has higher Q value compared to the MIM structure but due to occupying larger area, parasitic effect becomes prominent in the high frequency applications. A general investigations on equivalent circuit based modelling approach was carried out based on the data from the EM simulations of the multi-layer structures. Further details are available in Appendix B. Different combinations of metal layers have been investigated for the multi layer capacitors and the one forming with metal three (M3) to metal five (M5) has been found to have given the best performance with regards to Q value (around 22 at 20 GHz for an area of 100 $\mu m^2$). Figure 3.13 shows the cross section of the used multilayer capacitor.

**3.7 Small Signal amplifiers**

The main aim of this second part of the thesis is to investigate the feasibility of designing millimeter wave small signal amplifiers, using submicron CMOS processes. Starting with the amplifiers designed with the 90 nm CMOS process, the thesis discusses the general approach adopted to designing the amplifiers and the way of analyzing them. The measured data for the 45 nm CMOS amplifiers are however, not available during the time of writing the thesis.
To keep the layout area to a reasonable limit, the transmission lines were meandered where necessary. The distributed elements were used for implementing the passive elements and the matching networks. A decoupling network in the bias line has been used to stabilize the amplifier and to block the RF-signal in the DC bias path. A 10 Ω resistance (20 Ω for 90 nm process) coupled with a 1 pF MIM capacitor (multilayer cap for 90 nm process) was used in the decoupling network. The distributed resistance was formed from TaN metal sheet.

![Typical layout schematic of a single stage amplifier with the meandered transmission lines.](image)

Fig. 3.14 shows a typical layout of a single stage amplifier with meandered transmission lines. For a double stage implementation, two such stages are cascaded by maintaining optimum power transfer between the stages. The die photo of 90 nm CMOS amplifiers operating at 40 and 20 GHz, respectively are shown in Fig. 3.15.

### 3.7.1 90 nm CMOS amplifiers

Two amplifiers have been designed at 40 GHz and 20 GHz based on 90 nm bulk CMOS. The back end consists of five metal layers with the signal line at the fifth metal layer and the grounding at the first metal layer. This is described in detail in section 3.3 and Fig. 3.3.
CHAPTER 3. CMOS MILLIMETER-WAVE AMPLIFIERS

Figure 3.15: Micro-photograph of (a) 40 GHz small signal amplifier with an effective circuit area including pad: 0.7 mm$^2$ (b) 20 GHz small signal amplifier with an effective circuit area including pad: 0.56 mm$^2$.

Figure 3.16: Noise parameters versus current density for the 90 nm bulk CMOS. The data is measured at three different frequencies for a drain voltage of 1.5 V.[courtesy data: Mattias Ferndahl]
40 GHz small signal amplifier

The size of the transistor used in the design has a width of 2 $\mu$m with 20 fingers giving a total width of 40 $\mu$m. In order to have a sound understanding of the noise profile, the measured noise parameters of the device are plotted against the device’s current density at three different frequencies namely, at 18 GHz, at 20 GHz and at 24 GHz. This is shown in Fig. 3.16.

It is interesting to note that a current density within the range of 0.1 mA/$\mu$m to 0.2 mA/$\mu$m ensures the minimum NF for the device. A recent paper [76] reveals that a current density of $\sim$0.15 mA/$\mu$m gives the minimum noise figure irrespective of CMOS technology node and foundry. Within this limit, $F_{\text{min}}$ ranges from 2.75 dB to 3.25 dB for a frequency span of 6 GHz (18-24 GHz). With 50 $\Omega$ terminations, NF remains around 4.5 dB and the noise resistance $R_n$ remains close to 75 $\Omega$.

To see the impact of drain supply on the noise profile, the above parameters are plotted for a different drain voltage with $V_{dd}$ at 1.0 V. The resulting plots are shown in Fig. 3.17. It can be seen that $F_{\text{min}}$ increases by as much as 0.3 dB for the same minimum current density at different frequencies. Similar variations can be observed for NF.

Fig. 3.18 shows the device’s IV curve and the corresponding unity gain frequency for a $V_{dd}$ of 1.5 V. To trade-off between the gain [Fig. 3.19] and the noise figure, a current density of 0.225 mA/$\mu$m has been chosen corresponding to gate voltage of 0.65 V. The chosen current density remains close to the range for minimum noise figure. An estimated $f_t$ of 80 GHz (approx.) is obtained as shown in Fig. 3.18(b). Implementation of the 40 GHz amplifier therefore, proves realistic with an operating frequency near $f_t/2$.

The matching network has been implemented with the distributed elements. It has been designed in such a way that $\Gamma_{\text{opt}}$ remains close to $S_{11}$ at the target frequency. Transmission lines in the back end have been used to implement the matching network. Simulations have been carried out with the built-in model in ADS. This was verified by field simulations in HFSS and showed almost identical characteristics. Based on the theory of stub matching networks for simultaneous gain and NF optimization [77], an estimation of the stub geometry have been determined which were latter optimized by the simulator. The final line length became rather lengthy and have
Figure 3.17: Noise parameters versus current density for the 90 nm bulk CMOS. The data is measured at three different frequencies for a drain voltage of 1.0 V.[courtesy data: Mattias Ferndahl]

Figure 3.18: (a) IV curve for 90 nm bulk CMOS (W = 2 µm, f = 20) (b) $f_t$ for $V_{dd} = 1.5$ V.
Figure 3.19: Available gains for different frequencies at a drain supply of 1.5 V

been meandered to save the overall occupied area.

In order to avoid cross coupling between the two adjacent lines while meandering, as a thumb rule, a minimum separation of more than three times the width of the corresponding line have always been maintained. The layout architecture looks similar to the one shown in Fig. 3.14. The drain and the gate shunt stubs have been used to supply the bias. In order to suppress unwanted RF oscillations, a decoupling network (RC PI netowrk) has been used in the bias lines.

Considering the performance of the amplifier, capacitors in the decoupling network can be allowed to have greater variations (greater tolerance margin due to over/under estimations or process/temp/aging related variations) compared to the one used as coupling capacitors. The multi-layer (M5-M1) capacitor has therefore been used in the decoupling network. The total area occupied by each of the capacitor is around $65 \cdot 65 \, \mu m^2$. A 1 pF MIM Cap was chosen to be used as coupling capacitors. The occupied area is about $\approx 45 \cdot 35 \mu m^2$ and was implemented by scaling up the single cell capacitor worth 0.1 pF each. Two such stages are cascaded by the high value MIM capacitor. Corresponding circuit photo is shown in Fig. 3.15(a).

Characterizations of the 40 GHz amplifiers have been done by studying the scattering parameters, NF and power compression. Fig. 3.20 shows the measured and the simulated small signal response. The measured gain at 40 GHz is 6 dB. Matching at both the ports re-
Figure 3.20: Measured and simulated s-parameter of the 40 GHz amplifier.

mains broad band with a value lower than -10 dB. However, the center frequency is seen to have shifted down to 35 GHz giving a gain of 7.25 dB. The measured -3 dB bandwidth is 12 GHz, approximately. Downshifting of $S_{11}$ has also been noticed. The reason is not very obvious though, but may be due to the lossy nature of the silicon. The DC losses in the transmission line was found to be 5.6 $\Omega$/mm [65] which is quite substantial to cause considerable deviations in the circuit performance.

Fig. 3.21 shows the schematic set up for the measurement. To measure the NF above 26.5 GHz, a signal generator 83650B, a source module HP 83555A and a mixer was used to down-convert the LO. A Microwave amplifier 8349B has been used to amplify the LO signal. Figure 3.22(a) shows the simulated and the measured NF of the given amplifier. Measurement gave a value around 7.6 dB whereas the simulated value is 7.24 dB. Good agreement between the measured and the simulated data can be observed. Its also evident from the simulation that the circuit is noise matched at the center frequency. NF sensitivity on bias is shown in Fig. 3.23. The minimum noise
3.7. SMALL SIGNAL AMPLIFIERS

Figure 3.21: Schematic for instrumentation set up for NF measurement above 26.5 GHz using Agilent 8974A analyzer.

Figure 3.22: Noise figure of the 40 GHz amplifier (a) Measured (circled), Simulation (solid) (b) Simulated.

The figure is found to be at a bias of 0.65 V at the gate and 1.75 V at the drain. This is the same bias for which the NF was optimized. The drain voltage, however, is slightly higher. This is due to the small voltage drop across the 20 Ω resistor of the decoupling network used in the bias line.

Finally, the nonlinear characterization of the amplifier was performed by measuring the 1 dB power compression which is -5.5 dBm referred to the output port. This is shown in Figure 3.24. This is a reasonable value specially when the gate supply is optimized for low noise figure. In a double stage LNA, the second stage could be optimized for high linearity to maximize the overall linearity of the LNA. This feature, however, has not been investigated with the current design.

Table 3.1 shows a comparison of the reported work with other similar published works in the literature. The amplifier is considered to be working with maximum gain at 35 GHz. However, the noise is
**CHAPTER 3. CMOS MILLIMETER-WAVE AMPLIFIERS**

**Figure 3.23:** Bias sensitivity on the measured NF (a) NF versus $V_{gg}$ with $V_{dd}$ as a parameter (b) 3D variation.

**Figure 3.24:** Measured compression characteristics of the 40 GHz amplifier.

**Table 3.1:** Comparison with other published work

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<td>90 nm SOI</td>
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φ This work

optimized at 40 GHz and therefore its worthwhile to conduct the comparative investigations at 40 GHz also. This is shown in Table
3.7. SMALL SIGNAL AMPLIFIERS

Figure 3.25: Measured and simulated s-parameter of the 20 GHz amplifier.

3.2. Even after comparing with some of the most recent works, the reported work in the thesis stands out with regards to measured NF (not available in other works) and power consumption.

Table 3.2: Comparison with other published work

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<td>0.386</td>
<td>43.2</td>
<td>65 nm CMOS</td>
</tr>
</tbody>
</table>

Ψ This work

20 GHz small signal amplifier

The same device has been used to design a single stage 20 GHz amplifier. A single ended topology with stub matching techniques have been adopted to design the circuit. The device size and the supply remained the same. Based on the investigation of the device’s RF
and noise characteristics, similar design procedures as that of the 40 GHz amplifier have been followed. Fig. 3.25 shows the measured and the simulated performance of the amplifier. Measurement gave a value of 5.8 dB at 20 GHz. This is roughly 2 dB higher than the simulated value at the same frequency. Measured $S_{11}$ and $S_{12}$ shows very good matching both at the input and at the output ports. A slight shift in the frequency can be noticed with the input matching network. The reason, as already mentioned, could be due to lossy nature (RC parasitics) of silicon which was not properly taken into considerations during the simulations.

Fig. 3.26 shows the bias sensitivity of the amplifier on gain performance. Variation of $S_{21}$ (max.) has been plotted for various gate voltage [Fig. 3.26(a)]. The plot confirms the chosen gate bias as the optimum gate supply for the maximum gain. Corresponding gain variation with the drain and gate bias is shown in the adjacent figure.

![Figure 3.26](image)

**Figure 3.26:** Measured $S_{21}$ sensitivity on bias of the 20 GHz amplifier (a) $S_{21}$ vs. frequency with the gate voltage as parameter. $V_{dd}$ was set at 1.5 V (b) Variation of $S_{21}$ for the gate and drain bias.

Characterization of NF of the amplifier was done with Agilent NF analyzer, 8974 A. Figure 3.27 shows the measured NF versus the frequency. The amplifier gave a NF of 6.4 dB measured at 20 GHz. This is 1 dB higher than the simulated value at the same frequency. Virtually, the optimum noise match occurs several GHz above the designed frequency. This is evident from the downward slope of the measured noise curve. Simulated curves plotted in Fig. 3.27(b) shows that the optimum noise match occurs at 24 GHz with a value of 4.6 dB at 24 GHz whereas from measurement it is approximately
5.2 dB.

![Graphs](image_url)

Figure 3.27: Noise figure of the 20 GHz small signal amplifier (a) Measurement (b) Simulation.

![Graphs](image_url)

Figure 3.28: Measured compression characteristics of the 20 GHz amplifier. (a) -1 dB compression (b) IP3.

Compression characteristics for the amplifier is shown in Fig. 3.28. The measured 1 dB compression point is +1 dBm (referred to the output) and the IP3 (third order intercept point) is +10 dBm (referred to the output).

### 3.7.2 45 nm CMOS amplifiers

This section discusses the design of 90 GHz LNA in 45 nm CMOS process. Since the measured data is not available, the analysis is based on simulations. Foundry provided device models have been used for circuit analysis. From Fig. 3.16-3.16 in the earlier section, it has been shown that a current density in the range of 0.1 mA/µm-0.2 mA/µm ensures low noise figure. If we allow ~5 mA drain current
to minimize the overall power consumption, the device width lies in the range of 20 µm-40 µm.

![Graph](image)

**Figure 3.29:** (a) Simulated IV characteristics (b) Extracted $f_t$ [re-drawing Fig. 3.6] for a drain voltage of 0.6 V.

![Circuit Schematic](image)

**Figure 3.30:** Circuit schematic of the 90 GHz low noise amplifier.

Based on a trade-off between the gain and the noise figure, a device width of 24 µm has been chosen. Fig. 3.29(a) shows the IV plot for a two finger, 12 µm width device. For the chosen current of 5 mA/µm, the gate requires a supply of 0.65 V. The corresponding drain supply is approximately 0.6 V. From Fig. 3.29(b) it can be seen that the above current density incorporates a unity current gain frequency $f_t$, of about 170 GHz. This is almost double the center frequency which
3.7. SMALL SIGNAL AMPLIFIERS

Figure 3.31: Simulated noise and Associated Gain of the cascode 45 nm bulk CMOS.

clearly confirms the feasibility of designing the amplifier at 90 GHz.

One of the critical parameters liable to degrade the performance of submicron CMOS devices at high frequency specially in the millimeter wave regions is the gate-to-drain capacitance or the Miller Capacitance [66]. For an efficient high frequency performance, the device should have better isolation between the input and the output. One possible solution is to consider a cascode topology. It gives better isolation, has better stability margin, has higher MSG figure of merit and above all provides higher gain.

However the noise performance is worse than that of the common source topology. Cascode, in principle, is the cascade of a common source and a common gate configuration. The channel noise contributed by the common gate configuration degrades the overall noise performance. Careful choice of the device dimension and the drain current play a crucial role in optimizing the gain and the noise figure. Fig. 3.31 shows the noise profile of the cascode configuration versus drain current for various gate voltage. Both the transistors have the same device width i.e. 24 ${\mu}$m.
One possible problem with the cascode topology is the introduction of the pole at the drain-source node. The parasitic capacitance at the drain-source junction shunts an RF current to ground thereby decreasing the gain and degrading the noise performance. The problem becomes acute for circuits operating in the upper extreme of $f_t$ specially above $f_t/2$ [84]. One possible solution is to tune out the deleterious capacitance by an inductor [78]. However Q factor of the inductor at this frequency on the lossy Si substrate is rather poor. Moreover, the inductor needs comparatively a large decoupling capacitor to block the DC. This affects the required circuit area to some extent. The treatment was therefore, not considered in the design.

The procedures discussed in the earlier section was adopted here to design the matching network with the micro-strip lines in the above IC layer (Fig. 3.4). This gives lower line loss and less parasitics effects [section 3.6.1]. The main aim of using the above IC layer is to overcome or minimize the constraints encountered earlier by the circuits designed in the back end. Specially it gives better shielding to the RF signal from the lossy silicon substrate. Further investigations of transmission line properties in the post process layers can be found in [56], [57] [85], [86], [87].

![Figure 3.32: Layout of the 90 GHz low noise amplifier.](image)

Given the freedom of ample die area, the transmission lines were preferred not to be meandered considering such high operating fre-
Figure 3.33: Simulated noise and gain for the 45 nm bulk CMOS.

Figure 3.33 shows a 12 dB simulated gain with -3dB bandwidth greater than 20 GHz. Simulations show good isolation between the input and the output port with the reverse transmission coefficient less than -27 dB at 90 GHz. Good matching can also be noticed. The simulated noise figure is around 2.75 dB at the center frequency. When compared to a recent LNA work on 65 nm CMOS with a NF of 5.7 dB at 80 GHz [88], a ∼3 dB noise figure at 90 GHz in 45 nm CMOS is rather realistic. The K and Mu factor are plotted in Fig. 3.34(b) verifying the amplifier’s stability in the frequency band of operation.

To compare the proposed amplifier with other similar works published in the literatures, the following figure of merit was introduced [78]. Since very few CMOS LNA can be found at 90 GHz, the frequency requirement is relaxed and the LNA’s working in the whole W band spectrum is considered in the following investigation:

\[
FOM = \frac{S_{21} \cdot BW[GHz]}{(NF - 1) \cdot P_{DC}}
\] (3.1)

Where S21 and NF are expressed in magnitudes, P_{DC} is the dissipated power in mW and BW is the -3dB bandwidth in GHz. Since
Figure 3.34: (a) Simulated NF (b) Simulated stability factors.

the circuit area is always an important parameter of consideration, the above expression is normalized with the corresponding circuit area. The modified equation becomes:

\[
\text{FOM} = \frac{S_{21} \cdot \text{BW}[\text{GHz}]}{(\text{NF} - 1) \cdot \text{P}_{\text{DC}}[\text{mW}] \cdot \text{Area}[\text{mm}^2]}
\]  

Based on the expression above, FOM is calculated for some of the recently published LNAs in the W-Band and compared to that of the LNA proposed in this thesis. The gray solid bar shows the resulting FOM numbers. It's evident that the reported work outperforms the contemporary LNAs by a considerable margin except the one reported in [89]. Since FOM depends inversely on the area, it could be improved further by reducing the overall circuit size. As pointed out earlier, there was no restrictions on the die area, no effort was spared to make it smaller. With the transmission lines meandered and some re-arrangement of the bias network, its possible to squeeze the area by as much as 50%. Taking this change into account, re-calculating and redrawing the FOM bar (non-shaded), it is seen that a comparable (to [89] ) Figure Of Merit can be credited to the designed LNA. This observation gives us the feeling of bright prospects of CMOS based circuits in the millimeter and submillimeter-wave regions in the near future.

3.8 Discussion, Conclusion and Future work

Table 3.3 summarizes some of the best reported State-Of-the-Art amplifiers on various technologies. Most of the reported millimeter wave and sub millimeter-wave amplifiers belong to the III-V group. As pointed out earlier, the electron mobility as well as the higher
3.8. DISCUSSION, CONCLUSION AND FUTURE WORK

Figure 3.35: Figure of Merit for the recent State-of-The art LNA in W-Band. The reported work is presented by [*]

Drift velocity enables the III-V technologies to have comparatively higher $f_t$ and $f_{\text{max}}$. CMOS based devices, on the other hand, suffer from higher sheet resistance of the polysilicon gates and lower substrate resistance consequences of which become severe around millimeter wave region. A higher gate resistance can lower the transistor $f_{\text{max}}$, power gain and increase the noise. However, adopting different layout techniques of the gate could minimize some of the problems above. Whereas a GaAs FET can be treated as a three terminal device, the existence of bulk terminal and body effect complicate matters for CMOS. When first explored for RFICs in the mid 80’s, CMOS was the worst available process for noise performance, passive component integration, electrostatic discharge (ESD), and device modelling. Concentrated research efforts have dramatically reduced the performance gap between CMOS and other popular processes.

Interest in millimeter-wave CMOS circuits are therefore, increasing with the gradual down scaling of the gate length. Table 3.3 shows the performance summary of the State-Of-Art LNA’s where substantial number of works can be seen in the V-W band. The per-stage gain is comparable to other technologies. However, most of the designs are lagging behind in the noise performance. Another point
worth noting is the total power consumed by most of the CMOS amplifiers which is considerably high except the one reported in [89]. Since one of the goals of using the submicron CMOS is to pare down the power consumption to a bare minimum, the above circuits fail in that perspective. Keeping this in mind, the proposed work in the thesis strives to achieve that goal other than attaining high gain and low NF.

The thesis outlines the design and characterization of small signal amplifiers based on 90 CMOS technology and proposes two amplifier designs (based on simulations) on 45 nm CMOS. The extracted $f_t$ was as much as 200 GHz which shows its promising feature to designs circuits i.e. LNA well above 100 GHz. On the part of the 90 nm CMOS amplifiers, the measured results showed satisfactory performances with regards to gain, NF, power consumption. The slight shift in the center frequency for the 40 GHz amplifier can be attributed to the dispersion effect [104] by the passives or the transmission lines. Proper modelling of the loss phenomenon in the passive components may bridge the gap to a considerable extent.

### Table 3.3: State-Of-The-Art LNA’s

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$^a$InAlAs/InGaAs
$^b$Φ This work: Simulated results
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Appendix A

Small Signal Voltage Gain

This section deals with the derivation of small signal voltage gain of feedback amplifiers.

A.1 Source Equivalent Impedance

\[ Z_X(s) = \left[ \left( \frac{1}{R_{dsC}} + \frac{1}{sC_{eq}} \right) \right] \frac{1}{R_s} \]

If the control transistor is driven from a low impedance source, \( C_{eq} \) is approximately equal to the sum of \( C_{ds} \) and \( C_{gd} \).

\[ Z_X(s) = \left[ \left( \frac{R_{ds}}{1 + sR_{dsC_{eq}}} \right) + \frac{1}{sC_{cc}} \right] \frac{1}{R_s} \]

\[ Z_X(s) = \frac{1 + sR_{dsC_{eq}C_{cc}}}{sC_{cc} + \frac{1}{R_s} + s^2R_{dsC_{eq}C_{cc}}} \frac{1}{R_s} \]  \( \text{(A.1)} \)

\[ Z_X(s) = \frac{R_s + sR_{dsC_{eq}C_{cc}}}{1 + s \left( R_sC_{cc} + R_{dsC_{eq}C_{cc}} \right) + s^2 \left( R_sR_{dsC_{eq}}C_{cc} \right)} \]  \( \text{(A.2)} \)
A.2 Series Feedback VGA

The intrinsic small signal model with the source impedance $Z_X(s)$, of a common source configuration is shown in Figure A.2.

Applying KCL at the ‘Source’ Node;
\[ sC_{gs}V_{gs} + g_mV_{gs} + V_{ds}g_{ds} + sC_{ds}V_{ds} = \frac{V_s}{Z_X(s)} \]  
(A.3)

And, applying KCL at the output;
\[ s(V_{out} - V_{in})C_{gd} + g_mV_{gs} + V_{ds}g_{ds} + sC_{ds}V_{ds} = -\frac{V_{out}}{Z_L} \]  
(A.4)

subtracting equation (A.4) from equation (A.3);
\[ sC_{gs}V_{gs} - s(V_{out} - V_{in})C_{gd} = \frac{V_s}{Z_X(s)} + \frac{V_{out}}{Z_L} \]  
(A.5)

\[ \Rightarrow sC_{gs}(V_{in} - V_s) + s(V_{in} - V_{out})C_{gd} = \frac{V_s}{Z_X(s)} + \frac{V_{out}}{Z_L} \]  
(A.6)

\[ \Rightarrow V_s = \frac{sV_{in}(C_{gs} + C_{gd}) - V_{out}(sC_{gd} + Y_L)}{Y_X(s) + sC_{gs}} \]  
(A.7)

Where $Y_X(s) = \frac{1}{Z_X(s)}$ and $Y_L = \frac{1}{Z_L}$, From equation (A.3);

\[ V_{gs}(sC_{gs} + g_m) + (g_{ds} + sC_{ds})V_{ds} = V_sY_X(s) \]  
(A.8)

\[ \Rightarrow (V_{in} - V_s)(sC_{gs} + g_m) + (g_{ds} + sC_{ds})(V_{out} - V_s) = V_sY_X(s) \]  
(A.9)

\[ \Rightarrow V_{in}(sC_{gs} + g_m) + (g_{ds} + sC_{ds})V_{out} = (g_m + g_{ds} + Y_X(s))V_s \]  
\[ + s(C_{gs} + C_{ds})V_s \]  
(A.10)
Using equation (A.7) into equation (A.10) and simplifying:

\[
V_{\text{in}} \left( g_m Y_X(s) - s\zeta - s^2\xi \right) + V_{\text{out}} \left[ Y_X(s) g_{ds} + Y_L (Y_X(s) + g_m + g_{ds}) + \eta + s^2\xi \right] = 0
\]

\[
\Rightarrow A_v = \frac{V_{\text{out}}}{V_{\text{in}}} = \frac{g_m Y_X(s) - s\zeta - s^2\xi}{Y_X(s) g_{ds} + Y_L (Y_X(s) + g_m + g_{ds}) + \eta + s^2\xi}
\]

(A.11)

Where

\[
\xi = C_{gd} C_{gs} + C_{gs} C_{ds} + C_{ds} C_{gd}
\]

\[
\zeta = g_{ds} (C_{gs} + C_{gd}) + C_{gd} (Y_X(s) + g_m)
\]

\[
\eta = C_{gs} (g_{ds} + Y_L) + C_{ds} (Y_X(s) + Y_L) + C_{gd} (Y_X(s) + g_m + g_{ds})
\]

### A.3 Parallel Feedback VGA

\(Z_{\text{eq}}\) is given by the series combination of \(Z_Y\) and \(C_{cc}\). From A.1,

\[
Z_{\text{eq}}(s) = \left[ 1 + sR_{dc} \frac{(C_{eq} + C_{cc})}{sC_{cc} + s^2R_{dc}C_{cc}C_{eq}} \right]
\]

(A.12)

**Figure A.3:** Simplified equivalent small signal model of parallel feedback VGA.

Considering \(Y_{eq}(s) = \frac{1}{Z_{eq}(s)}\) and \(Y_L = \frac{1}{Z_L}\), Applying KCL at the output node,

\[-V_{\text{out}} Y_L = sC_{ds} V_{\text{out}} + g_{ds} V_{\text{out}} + g_m V_{\text{in}} + Y_{eq}(s) (V_{\text{out}} - V_{\text{in}}) + sC_{gd} (V_{\text{out}} - V_{\text{in}})\]

\[
A_v = \frac{V_{\text{out}}}{V_{\text{in}}} = \frac{-g_m + Y_{eq}(s) + sC_{gd}}{Y_L + g_{ds} + Y_{eq}(s) + s(C_{ds} + C_{gd})}
\]

(A.13)
APPENDIX A. SMALL SIGNAL VOLTAGE GAIN

\[ A_v = \frac{V_{out}}{V_{in}} = -g_m + \frac{1 + sR_{ds} (C_{eq} + C_{cc})}{sC_{cc} + s^2R_{ds}C_{ce}C_{eq}} + sC_{gd} \]
\[ Y_L + g_{ds} + \frac{1 + sR_{ds} (C_{eq} + C_{cc})}{sC_{cc} + s^2R_{ds}C_{ce}C_{eq}} + s (C_{ds} + C_{gd}) \]  

(A.14)

Re-arranging and simplifying,

\[ A_v = \frac{V_{out}}{V_{in}} = \frac{-g_m + s\delta + s^2\beta}{g_{ds} + Y_L + s\lambda + s^2\psi} \]  

(A.15)

where,

\[ \delta = -g_mR_{ds} (C_{eq} + C_{cc}) + C_{gd} + C_{cc} \]
\[ \beta = R_{ds} [C_{eq}C_{cc} + C_{gd} (C_{eq} + C_{cc})] \]
\[ \psi = R_{ds} [C_{eq}C_{cc} + (C_{gd} + C_{ds}) (C_{eq} + C_{cc})] \]
\[ \lambda = R_{ds} (Y_L + g_{ds}) (C_{eq} + C_{cc}) + C_{gd} + C_{ds} + C_{cc} \]
Appendix B

Multi-Layer Capacitor Modelling Flow

![Flow chart](Image)

**Figure B.1:** Flow chart
**Figure B.2:** Geometry and Substrate definitions

**Figure B.3:** ADS circuit set up for parameter optimization. Cs: Capacitance between the metal layers, Rs: Series Resistance offered by the metal layer, Rx: Substrate leakage resistance, Ls: Inductance due to the length of the metal layer Cp1, Cp2, Rp1, Rp2: Parasitics between the metal layers and the substrate

### B.1 Optimization Objective

To attain the Model S-Parameter as close match as possible with the S-Parameter obtained from EM simulation of the device struc-
B.1. Optimization Objective

Figure B.4: Curve fitting between the modelled and the EM simulated data. Lines with star are from the field simulations.

Optimizing Expression: Minimization of $\delta, \beta, \psi, \lambda$ in the frequency range: 2 GHz to 50 GHz.

$$\delta = \frac{|S_{44} - S_{12}|}{|S_{34}|}$$
$$\beta = \frac{|S_{13} - S_{11}|}{|S_{33}|}$$
$$\psi = \frac{|S_{44} - S_{22}|}{|S_{44}|}$$
$$\lambda = \frac{|S_{43} - S_{21}|}{|S_{43}|}$$

Table B.1: Model Parameter extraction.

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<th>$R_s$</th>
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$^a$Area: $\mu m^2$
Figure B.5: Frq. 2 GHz to 50 GHz. Lines with star are from EM simulation.
Appendix C

Appended Papers
Paper A

A 45 dB Variable Gain Low Noise MMIC Amplifier
M. Anowar Masud, Herbert Zirath, Matthew Kelly

*IEEE Transactions on Microwave Theory and Techniques*,
Paper B

MMIC implementation of High Gain Low Noise IF VGA based on feedback topology
M. Anowar Masud, Herbert Zirath

Submitted to IEEE Journal of Solid State Circuits
Paper C

Comparative investigation between a single ended and a balanced IF VGA

M. Anowar Masud, Herbert Zirath

90 nm CMOS MMIC amplifier

M. Anowar Masud, Herbert Zirath, Mattias Ferndahl, Hans Olof Vickes

Paper E

A Variable gain MMIC amplifier

M. Anowar Masud, Mattias Ferndahl, Herbert Zirath
