Characterization and Analysis of Surface Passivations and Gate Insulators for AlGaN/GaN Microwave HFETs

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Abstract

The large bandgap of gallium nitride (GaN) and aluminum gallium nitride (AlGaN) offers an inherently high intrinsic breakdown field. When the materials are joined into the AlGaN/GaN heterostructure a 2-dimensional electron gas (2DEG) with a high electron density as well as high electron mobility is generated. The combination of high electron density with high mobility and high breakdown field results in excellent power handling capability at high frequencies. These inherently virtuous physical properties are utilized by the GaN-based heterostructure field effect transistor (HFET) technology.

This thesis deals with developing appropriate fabrication processes for AlGaN/GaN HFETs by basic material characterization methods. The main focus is on the passivation of the heterostructure surface, which is notorious for its effect on device performance. Several examples of the effect of the passivation process on the electrical properties of the heterostructure are presented. For example, it is shown that passivating a heterostructure using a non-optimized plasma based deposition method may redistribute more than 90% of the channel electrons to a barrier accumulation layer.

The use of metal-insulator-semiconducting-heterostructure (MISH) capacitor analysis for extracting interface states is described in detail. Based on a comparison of different passivation methods the low pressure chemical vapor deposition (LPCVD) silicon nitride (SiN\textsubscript{x}) emerges as a suitable candidate for passivation of AlGaN/GaN heterostructures. In this thesis the effects of different LPCVD SiN\textsubscript{x} deposition parameters are investigated. Furthermore, LPCVD SiN\textsubscript{x} passivation will produce devices that are less sensitive to illumination. The illumination sensitivity is reduced to less than 3% compared to 15% to 130% for other passivated and non-passivated heterostructures.

This thesis also reports on the fabrication and DC characterization of insulated gate HFETs. A 5 nm thick layer of LPCVD silicon nitride is deposited below the gate which reduces the gate current by one to two orders of magnitude. This type of device is a promising candidate for reliable HFETs with applications in microwave and power electronics.

**Keywords:** AlGaN/GaN heterostructure, HFET, passivation, passivation characterization
List of publications

Appended publications

This thesis is based on work contained in the following papers:


[E] M. Fagerlind, and N. Rorsman ”Illumination effects on electrical characteristics of GaN/AlGaN/GaN heterostructures and HFETs and their elimination by LPCVD silicon nitride passivation,” *Submitted to Journal of Applied Physics.*

Other publications

The following papers have been published but are not included in this thesis since the content is out of the scope of this thesis.


## Notations and abbreviations

### Notations

- $d_{B0}$: barrier thickness
- $d_{RE}$: recess etch depth
- $\mu_H$: Electron Hall mobility
- $\mu_{\text{meas}}$: Measured electron mobility
- $\omega$: Angular frequency
- $C_{\text{barr}}$: Barrier capacitance
- $C_{\text{pass}}$: Passivation capacitance
- $C_{\text{tot}}$: Total capacitance
- $f_{\text{max}}$: maximum frequency of oscillation
- $f_T$: current gain cut-off frequency
- $n_{C(V)}$: $C(V)$ integrated charge
- $n_{\text{meas}}$: Measured electron density
- $n_s$: Electron density
- $n_{\text{tot}}$: Total sheet density
- $q$: Electron charge
- $r_c$: Contact resistivity
- $R_{\text{sh}}$: Sheet resistance
- $t_{RE}$: Recess etch time
- $V_{2A}$: 2DEG accumulation voltage
- $V_{BA}$: Barrier accumulation voltage
- $V_{DS}$: Drain to source voltage
- $V_{GS}$: Gate to source voltage
- $V_{PO}$: Pinch-off voltage
### Abbreviations

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
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<tbody>
<tr>
<td>2DEG</td>
<td>Two Dimensional Electron Gas</td>
</tr>
<tr>
<td>AlGaN</td>
<td>Aluminium-Gallium-Nitride</td>
</tr>
<tr>
<td>AlN</td>
<td>Aluminum-Nitride</td>
</tr>
<tr>
<td>C(V)</td>
<td>Capacitance-Voltage</td>
</tr>
<tr>
<td>DC</td>
<td>Direct Current</td>
</tr>
<tr>
<td>HFET</td>
<td>Heterostructure Field Effect Transistor</td>
</tr>
<tr>
<td>HSD</td>
<td>Heterostructure Schottky Diode</td>
</tr>
<tr>
<td>GaN</td>
<td>Gallium-Nitride</td>
</tr>
<tr>
<td>I(V)</td>
<td>Current-Voltage</td>
</tr>
<tr>
<td>LCR meter</td>
<td>Inductance-Capacitance-Resistance meter</td>
</tr>
<tr>
<td>MISH</td>
<td>Metal Insulator Semiconducting Heterostructure</td>
</tr>
<tr>
<td>MISHFET</td>
<td>Metal Insulator Semiconducting HFET</td>
</tr>
<tr>
<td>MMIC</td>
<td>Monolithic Microwave Integrated Circuit</td>
</tr>
<tr>
<td>MSMH</td>
<td>Metal Semiconducting-Heterostructure Metal</td>
</tr>
<tr>
<td>OSP</td>
<td>Optical Surface Profiler</td>
</tr>
<tr>
<td>PECVD</td>
<td>Plasma Enhanced Chemical Vapor Deposition</td>
</tr>
<tr>
<td>PPC</td>
<td>Persistent Photoconductivity</td>
</tr>
<tr>
<td>RS</td>
<td>Reactively Sputtered</td>
</tr>
<tr>
<td>SO</td>
<td>Surface orientation</td>
</tr>
<tr>
<td>TCAD</td>
<td>Technology Computer Aided Design</td>
</tr>
<tr>
<td>TLM</td>
<td>Transfer Length Method</td>
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</table>
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Chapter 1

Introduction

Transistors based on the AlGaN/GaN heterostructure have been researched during the last 20 years [1]. The wide bandgap of the materials in the AlGaN/GaN heterostructure implies an inherently high electric breakdown field. Furthermore, a 2-dimensional electron gas (2DEG) with a large electron sheet density that have a high mobility and a high saturation velocity is formed in the structure. The electrical properties of the 2DEG enable fabrication of devices with low resistance and high current densities. The combination of all these characteristics makes the AlGaN/GaN heterostructure material an excellent candidate for power and high frequency applications [2,3]. Furthermore, the possibility to grow the heterostructure on SiC substrates, which have high thermal conductivity, makes the material system even more suitable from power management perspective. However, there is still a need for research and development of transistor fabrication processes that will fully and reliably utilize the inherently virtuous electrical properties of the AlGaN/GaN heterostructure.

Compared to other heterostructure device technologies the AlGaN/GaN heterostructure has some features that can be considered both advantageous or disadvantageous, all depending on application. For example, the heterostructure is strongly polarized, resulting in large charge densities at the surface and at internal heterointerfaces. The polarization also results in high internal electric fields [4]. Furthermore, the 2DEG will be generated without any intentional doping [5].

There are several reports on AlGaN/GaN based devices that are affected by lag- and frequency dispersion effects [6, 7]. The lag and dispersion affect the devices in different ways but can be shortly summarized as differences in device output depending on the dynamics of the input signal. The cause of these effects is commonly accepted to be due to trapping of electrons. The charge trapping gives rise to virtual gating, resulting in increased device resistance during certain operation conditions. The traps causing the dispersion has been identified to be located at the surface of the heterostructure [8]. In order to reduce trapping the most commonly employed method is to passivate the surface by deposition of a passivation dielectric [9]. However, the passivation may also degraded device performance, predominately by increasing gate leakage and lowering breakdown voltage [10,11].
Reliability of GaN HFETs is an increasingly more researched area [12], which is a natural consequence of a maturing technology. A recurring reliability/stability issue for the GaN HFET is the large gate current. More stable devices showing a higher reliability can be obtained by introducing a gate insulator between the gate and the heterostructure surface [13]. The devices are then referred to as MISHFETs or MOSHFETs (metal-insulator/oxide-semiconducting-heterostructure-field-effect-transistors) depending of which gate dielectric is used.

1.1 Thesis motivation

To fully take advantage of the potential of AlGaN/GaN HFET technologies, a reliable passivation, yielding dispersion-free operation is required. The dispersions is closely linked to states at the surface of the heterostructure.

1.2 Thesis contribution

In this work methods of characterizing and evaluating passivations are developed. Hall and metal insulator semiconducting heterostructure (MISH) capacitor capacitance-voltage (C(V)) characteristics have simultaneously been analyzed to provide a more complete picture of the interaction between surface passivation and the electrical properties of the heterostructure.

With the aid of MISH analysis the passivation using a low pressure chemical vapor deposition (LPCVD) silicon nitride (SiN$_x$) is identified to be a potential candidate for providing a surface passivation with low densities of states at the passivation interface.

In this thesis the potential of the LPCVD silicon nitride is further explored also in the role as gate dielectric for MISHFETs. The devices have not been fully characterized but preliminary results are presented to exemplify the use of fabrication methods described in this thesis.

1.3 Outline

In addition to this introductory chapter the thesis is divided into six additional chapters. Chapter 2 offers a summarized description of the AlGaN/GaN heterostructure and the current state of AlGaN/GaN HFETs, MISHFETs and monolithic microwave integrated circuits (MMICs). Chapter 3 presents different methods for heterostructure and passivation characterization. Chapter 4 applies the methods to different SiN$_x$ passivation methods, with focus on the LPCVD SiN$_x$. Chapter 5 includes a discussion around the fabrication and characterization of HFETs and MISHFETs, with a large focus on the most critical fabrication steps, ohmic contacts and surface passivation. Chapter 6 is a summary of the appended papers. Finally, chapter 7 concludes this thesis as well as presents some suggestions for future work.
Chapter 2

AlGaN/GaN heterostructure electronics

The binary alloys AlN and GaN are part of the III-N group of materials, i.e. they are made up of one atom from group III in the periodic table and Nitrogen. AlN and GaN have some properties that make them different from most other semiconductor materials. The materials have large bandgaps and they have a polarized crystal structures. In Table 2.1 some of the most basic properties of AlN, GaN, and some other commonly used semiconductors are reported. The larger bandgap of AlN and GaN put these materials in a group which are collectively referred to as wide bandgap semiconductors. The properties of the AlGaN alloy can to first order approximation be obtained by linearly interpolating between the values of AlN and GaN (for more accurate parameter determination different bowing parameters have to be accounted for [14]).

In general terms, a heterostructure is a single crystal material that is the result of joining two (or more) different crystalline materials. To first order approximation, each entity of the heterostructure maintains the physical characteristics of the pure material. At the same time the heterostructure material may have some additional properties that would not be found in either of the constituent materials. This aspect has opened up an entire field of research called heterostructure engineering where heterostructures may be tailored for specific applications. An indication of the significance of heterostructures was when the year 2000 Nobel physics prize was awarded in part to Herbert Kroemer and Zhores Alferov for their pioneering work on heterostructures [15].

| Table 2.1: A comparison of material properties for different semiconductor materials | H=hexagonal crystal structure [16]. |
|-----------------------------|-------------------|-------------------|-------------------|-------------------|-------------------|
|                            | Si                | GaAs              | 4H-SiC            | 2H-GaN            | 2H-AlN            |
| $E_g$ [eV]                 | 1.1               | 1.4               | 3.2               | 3.4               | 6.2               |
| $\mu_n$ [cm²/Vs]           | 1400              | 8500              | 900               | 1000              | 300               |
| $v_{sat}$ [1·10⁵ cm/s]     | 1.0               | 1.2               | 1.2               | 2.5               | -                 |
| $E_{crit}$ [MV/cm]         | 0.3               | 0.4               | 4                 | 5                 | 1.5               |
| $k$ [W/cmK]                | 1.3               | 0.56              | 3.7               | 1.3               | 2.9               |
Table 2.2: Material parameters of III-nitrides that are relevant for the discussion in this section, the values are taken from [17].

<table>
<thead>
<tr>
<th></th>
<th>AlN</th>
<th>GaN</th>
<th>InN</th>
</tr>
</thead>
<tbody>
<tr>
<td>$a_0$ [Å]</td>
<td>3.11</td>
<td>3.19</td>
<td>2.54</td>
</tr>
<tr>
<td>$c_0$ [Å]</td>
<td>4.982</td>
<td>5.185</td>
<td>5.703</td>
</tr>
<tr>
<td>$P_{sp}$ [C/m$^2$]</td>
<td>0.081</td>
<td>0.029</td>
<td>0.032</td>
</tr>
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</table>

2.1 AlGaN/GaN heterostructure

At epitaxial growth of the AlGaN/GaN heterostructure, a highly conductive layer is formed at the interface of the two materials. The conductive layer is partly a consequence of the polarization of the III-N alloys. In the AlGaN/GaN heterostructure the crystals are polarized in a direction perpendicular to the heterointerface. The polarization is due to the hexagonal crystal structure of the III-N materials. The crystal structure of GaN is schematically shown in Fig. 2.1. The polarization is a result of the nitrogen atom having higher electro-negativity than the group-III atom. The N atom will pull the electron closer to its core and become negatively charged, leaving the group III-atom positively charged. The atom to atom dipole moments, $p$, shown in the figure will sum up to the total crystal polarization, called spontaneous polarization $P_{sp}$. Hence, the material will be polarized along the $c$-axis, while the symmetry of the crystal makes it non-polarized in a plane parallel to the heterointerface. Large surface/interface charge densities and large internal electric fields are generated [4] as a consequence of the polarization. The most basic crystal structure parameters for AlN, GaN and indium nitride (InN) are presented in Table 2.2.

If a crystal with a clear polar axis is compressed or elongated along a direction perpendicular to the axis, the distances separating each N-III pair will increase or decrease and hence change the polarization. Since the lattice con-

![Figure 2.1](attachment:figure2.png)
stants of AlN and GaN are different, a heterostructure formed between the materials will be strained. The polarization due to strain is designated piezoelectric polarization. In an AlGaN/GaN heterostructure the total polarization will become a combination of spontaneous and piezoelectric polarization.

Fig. 2.2 shows a schematic overview of a typical GaN epitaxial wafer (epi-wafer). The left part is a magnified drawing of the epitaxial structure while the right drawing is more true to the relative thicknesses of each layer. The surface passivation is included in this figure even though it is not part of the epitaxial structure. The passivation is usually deposited at a later point, but it is included here since it is an integral part of the AlGaN/GaN HFET technology. The drawing also defines the passivation interface and the channel interface as the interfaces between passivation/barrier and barrier/channel, respectively. The drawing represents the most simple GaN heterostructure i.e. a thin AlGaN layer grown on top of a thicker GaN layer. Towards the end of this section more advanced heterostructures are discussed.

AlGaN/GaN can be been epitaxially grown on different substrates. Sapphire was used as growth template for the first experiments [18], and is still used for research purposes. SiC is often used due to both: better lattice match for epitaxial growth, and to higher thermal conductivity [19]. Growth on silicon substrates is driven by the inexpensive substrates and compatibility with existing microelectronic fabrication processes [20]. There are also efforts to base the epitaxial growth on free-standing GaN wafers [21] or to transfer the epitaxial layer to diamond substrates [22].

The band diagram of a typical AlGaN/GaN heterostructure is plotted in Fig. 2.3. The conduction band minima and valence band maxima are plotted versus the distance from the channel interface (negative distances are closer to the surface). The wider bandgap of AlGaN and the more narrow bandgap of GaN will align at the heterointerface. Due to the difference in polarization a fixed positive charge will create an energetically favorable potential well just below the channel interface. The electron distribution has a distinguishable peak just below the channel interface. There is also a part of the electron distribution that penetrates into the barrier and a tail of the distribution that extends into the buffer. The band diagrams and electron distributions reported in this thesis have been calculated using the technology computer aided design (TCAD) software Sentaurus (by Synopsys). The simulation solves the

Figure 2.2: Passivated AlGaN/GaN epi-wafer.
Schrödinger equation for a material structure [23]. The electron distribution is referred to as a two-dimensional electron gas (2DEG) and its existence in the AlGaN/GaN heterostructure was experimentally demonstrated about 20 years ago [18]. Electrons located in the 2DEG are confined to the potential well in the direction perpendicular to the channel interface, but are free to move in the plane parallel to the channel interface. Electrons in the 2DEG are frequently reported to have room temperature mobilities above 2000 cm$^2$/Vs with a reported record mobility of 3200 cm$^2$/Vs [24]. These mobilities are several times higher than the mobility for electron conduction in GaN bulk crystals as reported in Table 2.1.

In the first AlGaN/GaN 2DEG demonstrations the AlGaN layer was doped in order to generate the conductive layer [18], which is understandable since doping of the barrier is how the 2DEGs are generated in AlGaAs/GaAs [25] and InAlAs/InGaAs [26] heterostructures. However, it was shortly thereafter realized that the 2DEG will be generated without doping [5] and most current publications relating to AlGaN/GaN 2DEGs do not dope the materials. Several theories concerning the source of the 2DEG has been presented; piezoelectric doping [27], impurity doping [28], and the more widely accepted theory of surface donors [29].

Through the process of heterostructure engineering, several improvements to the AlGaN/GaN heterostructure have been proposed. Two illustrative examples are methods to increase the channel confinement of the 2DEG. The first method is aimed at reducing the number of electrons penetrating into the barrier. This is accomplished by introducing a thin AlN exclusion layer between the AlGaN and the GaN [30]. The second method is aimed at reducing the magnitude of the electron density tail extending deeper into the buffer. This is accomplished by replacing the GaN buffer with an AlGaN back-barrier [31]. Fig. 2.4 schematically presents the heterostructures with a) AlN exclusion layer and b) Al$_{0.07}$Ga$_{0.93}$N back-barrier. The simulations have been simplified by not changing the polarization charge density at the channel interface and omitting the polarization charge densities at the additional heterointerfaces. Another suggestion for improving the heterostructure has been the growth of a GaN cap layer which can be used to reduce the
2.2. GAN HFETs

2.2.1 Dispersion Effect and Surface Passivation

Effect of dispersion without deposition of a surface passivation [32]. Other approaches constitute increasing the fraction of Al in the AlGaN barrier layer, which will increase carrier concentrations and mobility by increasing carrier confinement [33]. The extreme is to have a pure AlN barrier [30, 34].

A more fundamental modification of the heterostructure is the growth of N-polar heterostructures, basically turning the whole structure up-side-down. The concept is old [35] but it is only during the last couple of years that the growth technology has improved to a level where competitive device materials can be grown [36]. The growth is performed in such a way that the polarization vector of the materials is pointing in the opposite direction to what has previously been discussed. Instead of growing an AlGaN layer on top of a GaN layer the growth order is reversed; a GaN layer is grown on top of an AlGaN layer. The 2DEG will be formed on top of the AlGaN bulk and will automatically have a very good confinement against the bulk of the heterostructure (compare with the concept of back-barriers). Yet another type of heterostructure was the proposal to replace the AlGaN barrier with an InAlN barrier, which would provide a heterostructure with higher 2DEG sheet densities and with lower stress in the barrier layer [37]. InAlN/GaN heterostructures has been demonstrated with 2DEG sheet density as high as $2.7 \times 10^{13} \text{cm}^{-2}$ [38].

Regardless of utilized heterostructure, operation of devices have been reported to be affected by traps [39, 40].

2.2.2 GaN HFETs

It is the conductive 2DEG formed just below the channel interface that makes the AlGaN/GaN heterostructure an excellent template for field effect transistors. The first AlGaN/GaN HFET was demonstrated just a short period after the 2DEG was demonstrated [1]. Fig. 2.5 presents schematic images of an HFET in on- and off-state. The HFET utilizes the 2DEG as a channel for current conduction in on-state. The device is switched to off-state when the 2DEG below the gate is depleted due to a negative voltage at the gate.

The terminology used to describe the heterostructure field effect transistor deserves a short comment. In this thesis and most of the papers the term...
HFET is used. There are several other terms used to describe the same kind of device: High Electron Mobility Transistor (HEMT), Heterojunction FET (HJFET), Modulation Doped FET (MODFET), and Two Dimensional Electron Gas FET (TEGFET). In this thesis the term GaN HFET will be used to describe HFETs utilizing any type of heterostructure mentioned in the previous section, the exact epitaxial layer structure will only be specified when of importance.

Due to favorable electrical transport properties the GaN HFET can be used for both high power devices and high frequency devices. The state of the art GaN HFET power density is 40 W/mm at 4 GHz [41]. The high frequency performance is continuously improving. AlN/GaN HFETs with AlGaN back-barrier showing current gain cut-off frequency/maximum frequency of oscillation ($f_T/f_{\text{max}}$) values of 260/394 GHz [42] and 220/400 GHz [43] have been demonstrated. An even higher $f_T$ of 300 GHz has been reported for an InAlN/GaN type HFET with InAlN back-barrier [44] but with a quite modest $f_{\text{max}}$ of around 30 GHz. The GaN HFET does not only offer high power and high frequency performance. Quite good low-noise performance has been demonstrated as well. An AlGaN/GaN HFET with a noise figure of 0.98 dB at 18 GHz has been demonstrated [45]. Furthermore, HFETs with a combination of excellent noise performance and power performance have been reported [46].

There is an increasing number of companies offering GaN HFET technology commercially: Cree, Inc [47]; Nitronex Corporation [48]; Sumitomo Electric Device Innovations, Inc [49]; and TriQuint Semiconductor [50].

## 2.3 GaN MISHFETs

The introduction of an insulation layer below the gate of the HFET can be seen as the next step to proceed with development of the GaN HFET transistor technology. Several advantages related to the introduction of a gate dielectric has been discussed by Marso et al. [51]. MISHFETs have been fabricated with a large number of different gate insulation layers: SiO$_2$ [51], GaN [52], SiN$_x$ [53], Al$_2$O$_3$ [54], HfAlO [55].

Excellent high frequency MISHFET performance has been demonstrated using a SiN$_x$ gate dielectric with $f_T/f_{\text{max}}$ of 163/184 GHz [53], and record $f_T$ of 180 GHz has been reported [56].
2.4 GaN HFET MMICs

Interest from both commercial and military sources drives the development of AlGaN/GaN HFET based monolithic microwave integrated circuits (MMIC). The power density by itself implicates that GaN HFET technology can be utilized to reduce size of critical systems. Furthermore, the robustness and low noise figure of the GaN HFET technology may allow for removing limiter circuits in receivers [57].

A large number of demonstrators of GaN HFET based MMIC circuits have been reported: Power amplifiers from X-band [58,59] up to W-band [60], low noise amplifiers [61], oscillators [62], and receiver front-end [57] with design proposals existing for complete transceiver front-ends [63].

Even though this thesis does not specifically deal with MMIC technology, all the process development is performed with the intent to be easily integrated in the existing "in-house" MMIC process.
Chapter 3

Heterostructure and Passivation characterization

The most important characteristics for an AlGaN/GaN HFET material are high conductivity and a 2DEG that is well confined to the channel of the heterostructure. The conductivity requirement is easily evaluated by I(V) measurements. However, a more complete picture can be obtained by Hall characterization from which the magnitude of the 2DEG sheet density ($n_s$) and the 2DEG Hall mobility ($\mu_H$) can be extracted. The confinement is most effectively characterized by capacitance-voltage (C(V)) extraction [4].

A combination of Hall measurements and C(V) characterization of MISH-capacitors is used to characterize interface states and evaluate different passivation methods. The MISH C(V) method was described in paper [D] where it was used to compare different passivation deposition methods. Other reports concerning MISH C(V) have been published both before [64] and after [65] paper [D]. In the report by Mizek et al. [64] the influence of interface states is analyzed in a different interval of the C(V) sweep. In the report by Mizue et al. [65] the C(V) of Al2O3 passivated AlGaN/GaN is analyzed in a similar manner to the analysis paper [D].

3.1 Hall

Hall characterization is one of the most fundamental semiconductor characterization methods [66]. The Hall characteristics in this thesis is performed using a Biorad/Nanonmetrics Hall measurement system. The resistivity ($R_{sh}$) of the material is measured and then the Hall voltage is extracted by measurements during application of a magnetic field. $n_s$ and $\mu_H$ are then extracted from the measured Hall voltage. Hall characterization is an excellent way to monitor the effects of fabrication steps in an HFET process. This is especially true for AlGaN/GaN type heterostructures since a change of the properties at the surface may have a profound effect on properties of the 2DEG [67].
3.1.1 As-grown heterostructures

Since the research effort of our group does not include material growth the heterostructure materials have either been supplied by partners in joint research projects (Linköping University) or bought from commercial vendors (Cree, NTT-AT, EpiGaN). All materials investigated in this thesis are of depletion type, which means that the as-grown material should be conductive. Hence, after a simple material resistivity screening the materials with uncharacteristically high resistivity can be scrapped. Different material suppliers employ different methods of characterizing the materials before shipping them. Most commonly utilized methods are resistivity measurements by non-destructive eddy-current measurements and mercury probe C(V) measurements for extracting sheet densities, barrier thickness and electron distribution [68].

The electrical properties of a HFET processed heterostructure material always differ significantly from the measurements supplied by the material supplier. It is difficult to determine to which degree the change is caused by processing related material degradation, material non-uniformity, or uncertainties related to using different characterization techniques. For the purpose of eliminating these unknowns a "quick and dirty" characterization process was developed to evaluate AlGaN/GaN heterostructure materials. The method is described in paper [A] and relies on ohmic contacts of gallium metal and a Schottky contact of silver glue. The choice of these metalizations facilitates room-temperature processing of material characterization structures. The method offers evaluation of "as-grown" materials with the same characterization equipment as is used for the processed samples, thus eliminating one uncertainty. Furthermore the effect of a single processing step can be isolated and investigated.

As an example, the Ga&Ag process was used for investigating a heterostructure with InAlN barrier. After processing the first HFET samples the resistivity was seen to be huge compared to the data supplied by the epi-wafer supplier. Hall measurements revealed that the high resistivity was due to a very low $n_s$. Ga&Ag measurements showed that the as-grown material had a normal sheet density that was confined to the channel. The reduction of $n_s$ was identified to be due to a combination of incompatible cleaning process and the ohmic contact annealing. In this way a problematic processing step may be identified. More accurate characterization methods can then be used to quantify the effect the specific process step.

The gallium contacts alone have been used frequently to obtain the Hall characteristics of as-grown materials. These are used as reference values in order to trace the effect of different processing steps. Fig. 3.1 shows a collection of Hall measurements on ten different AlGaN/GaN heterostructure materials. Three types of heterostructures are characterized: AlGaN/GaN, GaN/AlGaN/GaN, and AlGaN/AlN/GaN. The heterostructures that have almost the same epitaxial specification are: two GaN/AlGaN/GaN wafers (blue); two AlGaN/GaN wafers (red); and three AlGaN/AlN/GaN heterostructures which have almost identical Hall characteristics. For all materials the Hall characteristics have been measured as a function of time after suspending illumination. The open symbols are measured with the sample continuously illuminated, the semi-closed symbols are measured about 1 minute after the illu-
3.1. HALL

Figure 3.1: Hall characteristics extracted from ten as-grown epi-materials with different epitaxial layer specification. Each material has been measured as a function of duration in darkness. The inset shows $n_{\text{meas}}$ as a function of time in darkness.

mination was suspended and the closed symbols are measured after even longer duration in darkness. The relation between different types of heterostructures conforms with what can be expected: materials with AlN exclusion layers have higher $n_s$ and $\mu_H$.

3.1.2 Two layer conduction and persistent photoconductivity

As discussed in paper [F] interpretation of the Hall results are not always trivial since conduction may be confined to more than one layer. The Hall measurements reported in Fig. 3.1 were all extracted assuming a uniform material, which seems to provide accurate results for most as-grown materials (with GaN/Al$_{0.14}$Ga$_{0.86}$N/GaN heterostructure as an exception). Processing, in particular deposition of surface passivation, may result in severe conduction in the barrier/cap layer as reported in paper [E] and paper [F]. A second conductivity layer with a different mobility will perturb the $n_s$ and $\mu_H$ extracted by Hall measurements. The measured $\mu_H$ and $n_s$ values are then weighted averages of the mobilities and sheet densities of the different layers, and hence no longer represent physical quantities [66, 69, 70].
\[ \mu_{\text{meas}} = \frac{n_b \mu_b^2 + n_c \mu_c^2}{n_b \mu_b + n_c \mu_c}, \]  
(3.1)

\[ n_{\text{meas}} = \frac{(n_b \mu_b + n_c \mu_c)^2}{n_b \mu_b^2 + n_c \mu_c^2}. \]  
(3.2)

\( n_b, n_c, \mu_b, \mu_c \) are the electron sheet densities and mobilities in the barrier and channel, respectively. If the mobility in each layer can be assumed to be constant equation (3.2) may be simplified by introducing the channel confinement ratio \((CCR=n_c/n_{\text{tot}})\).

\[ \mu_{\text{meas}} = (1 - CCR) \mu_b^2 + CCR \mu_c^2 \]  
(1 - CCR) \mu_b + CCR \mu_c, \]  
(3.3)

i.e. the measured mobility is completely independent of the total sheet density. It is determined entirely by the relative distribution of electrons between the channel and the barrier.

**Simple model**

The effect of two layer conduction on measured Hall parameters will first be demonstrated by an example assuming a simple model. In the model the channel and barrier both have constant mobilities of \( \mu_c = 1600 \text{ cm}^2/\text{Vs} \) and \( \mu_b = 300 \text{ cm}^2/\text{Vs} \), respectively. The effect on the measured parameters are plotted in Fig. 3.2. Each of the three curves in each plot represent a different total sheet density: \( n_{\text{tot}} = 4 \times 10^{12}, 5 \times 10^{12}, \text{ and } 6 \times 10^{12} \text{ cm}^{-2} \), respectively. In each plot CCR is assumed to vary between pure channel conduction \((CCR=1)\) to pure barrier conduction \((CCR=0)\).

Fig. 3.2a) reflects equation (3.3) where the mobility only depends on the relative distribution of electrons between the barrier and the channel, i.e. the curves for different \( n_{\text{tot}} \) are superposed. Fig. 3.2b) plots \( n_{\text{meas}} \) according to equation (3.2). A correct extraction of a specific \( n_{\text{tot}} \) is only measured for pure channel or pure barrier conduction. For all other CCRs the \( n_{\text{meas}} \) is lower than \( n_{\text{tot}} \). At \( CCR=0.18 \) the difference between \( n_{\text{tot}} \) and \( n_{\text{meas}} \) is almost 50%.

Fig. 3.2c) plots \( R_{\text{sh}} \) which is inversely proportional to the product of \( n_{\text{meas}} \) and \( \mu_{\text{meas}} \). Fig. 3.2d) plots a trajectory for each \( n_{\text{tot}} \) in the \( R_{\text{sh}} \) versus \( n_{\text{meas}} \) plane. Where the dotted contour lines in the background represent different \( \mu_{\text{meas}} \). The trajectory for a constant \( n_{\text{tot}} \) can be seen to start and end at the previously defined channel and barrier mobilities. The figure illustrates the ambiguity of the Hall measurement for a material with two-layer conduction.

**Sheet density dependent mobility model**

As discussed in both paper [E] and paper [F], the assumption of mobilities independent of sheet density is not correct. This is predominately due to the influence of Coulomb and interface scattering. Both scattering processes are related to the channel interface, and as a result the mobility in the low and high \( n_s \) regions will be reduced. The Coulomb scattering is dominating when the electrons are few compared to the large positive polarization charge density at the channel interface [71]. At high sheet densities the dominating scattering
3.1. HALL

![Hall Effect Diagram]

**Figure 3.2:** The effect of two layer conduction on measured Hall parameters:
a) the mobility versus CCR, b) n_{meas} versus CCR c) R_{sh} versus CCR, and d) n_{meas} versus R_{sh}

process is the interface scattering [72], which is due to a larger portion of the charge densities being pushed closer to the interface. The drift mobility (\(\mu_D\)) is determined from the relation \(I = qn_s \mu_D E\) [73], where \(I\) is the current density extracted at a low electric field \(E\). The sheet density is extracted by integration of the C(V), which is then related to the current measured at low electric field.

Fig. 3.3a) shows the measured capacitance and current used to extract the mobility versus sheet density. The extracted \(\mu_H\) versus \(n_s\) is plotted in Fig. 3.3b) where \(\mu_D\) has been transformed to \(\mu_H\) by multiplying it with 1.17 (which will result in a peak channel mobility comparable to the simple model). The model for channel mobility versus channel sheet density (\(\mu_c(n_c)\)) is obtained by interpolating the experimental data around the peak and then linearly extrapolating the experimental data for high and low \(n_c\). The model has a peak mobility of 1600 cm\(^2\)/Vs at \(n_s\) approximately \(4 \times 10^{12}\) cm\(^{-2}\). The model for barrier conduction (\(\mu_b(n_b)\)) is then constructed by rescaling \(\mu_c(n_c)\) to provide a peak mobility of 300 cm\(^2\)/Vs.

**Advanced model**

Fig. 3.4 is the equivalent plot of Fig. 3.2 but for two layer conduction modified with \(\mu_c(n_c)\) and \(\mu_b(n_b)\). Fig. 3.4a) shows that the mobility is no longer independent of \(n_{tot}\). For \(n_{tot}\) below \(4 \times 10^{12}\) cm\(^{-2}\) the \(\mu_c(n_c)\) and \(\mu_b(n_b)\) are on the left sides of their peak values in Fig. 3.3b), hence the \(\mu_{meas}\) is a single-valued function of CCR. However for larger \(n_{tot}\) there are sometimes two possible...
CHAPTER 3. HETEROSTRUCTURE AND PASSIVATION CHARACTERIZATION

Figure 3.3: a) The I(V) and C(V) measurements used for extracting the drift mobility versus different \( n_s \). b) Hall mobility models versus sheet densities in the channel and barrier.

\( CCRs \) that will provide a specific \( \mu_{\text{meas}} \). Fig. 3.4b) does not change dramatically from that of the simple model, but the difference between \( n_{\text{meas}} \) and \( n_{\text{tot}} \) is generally lower. For this specific case the largest deviation between \( n_{\text{tot}} \) and \( n_{\text{meas}} \) is approximately 30-40\%, which is 10-20\% smaller than for the simple model.

The Hall characteristics in combination with a two layer conduction model was used in paper [F] to explain the large resistivity increase experienced for heterostructures that had been passivated using a high plasma strike power.

Figure 3.4: The effect of two layer conduction, using the advanced mobility models, on measured Hall parameters: a) the mobility versus \( CCR \), b) \( n_{\text{meas}} \) versus \( CCR \) c) \( R_{\text{sh}} \) versus \( CCR \), and d) \( n_{\text{meas}} \) versus \( R_{\text{sh}} \)
The extremely large increase of $R_{sh}$ was found to be due to redistribution of electrons from the channel to an accumulation layer in the barrier. In a similar manner the two-layer Hall analysis was used in paper [E] to investigate the effect of illumination. Where large differences in photon-generated electron recombination dynamics was explained by difference in $CCR$.

**PPC**

It was shown in Fig. 3.1 that all as-grown samples show the same general effect of illumination, $R_{sh}$ is seen to increase due to an apparent decrease of $n_{meas}$. The difference in $n_{meas}$ for these as-grown materials is seen to be around $1 \times 10^{12} \text{ cm}^{-2}$. This behavior is designated persistent photoconductivity (PPC) [74–78]. The PPC and its effect on HFET devices was investigated in paper [E]. The PPC was explained to be predominately due to photo generation of electrons from surface states and DX-centers in the AlGaN barrier.

Fig. 3.5 plots an example of the magnitude of the illumination effect. The plot shows the resistance between two contacts measured in: darkness, with illumination, and with partial spectrum illumination. The measurement of the contact pair is more sensitive than the measurement using the Hall setup utilized for the plot in paper [E]. It can be seen that there is a small effect already for a filter with $\lambda_C = 475 \text{ nm}$. The PPC then increases slightly for filters with shorter $\lambda_C = 455$ and $395 \text{ nm}$ but is very small until the $\lambda_C = 335 \text{ nm}$ filter is used (the $\lambda_C = 375 \text{ nm}$ filter was not used in this measurement series).

### 3.2 MSHM characterization

MSHM characterization was used in paper [B] to extract electrical barrier thicknesses for development of an etch recipe for shallow barrier etches. In that specific report the recess etch was used to reduce the contact resistance of ohmic contacts. Furthermore, the MSHM process is also a convenient method

![Figure 3.5: Resistance for a series of different measurements where the sample is either non-illuminated, full spectrum illuminated or illuminated through different long-pass filters.](image-url)
to evaluate material uniformity, and to some extent material quality and/or process quality. The processing is simple, with only one metalization. In paper [B] the method was evaluated by characterizing an evaluation structure which is schematically shown in Fig. 3.6. The evaluation structure has two Schottky metal contacts and one ohmic contact. The ohmic contact is not required for the characterization method but it is fabricated for this test structure in order to be able to characterize each heterostructure Schottky diode (HSD) individually. Fig. 3.7a) plots the 100 kHz and 1 MHz MSHM C(V) characteristic measured between the two Schottky contacts and Fig. 3.7b) is the C(V) measurement for each individual HSD. The 100 kHz characteristic of the MSHM has a typical ”batman” curve characteristic where small capacitance ”ears” are visible in a small voltage region where the forward biased diode is conductive (only for the lower frequency) and the reversely biased diode is still accumulated.

Fig. 3.8 shows an example of MSHM characteristic when one of the HSDs is not a good rectifier (the diode still maintains some rectification). By measuring a few contacts the uniformity in barrier thickness (i.e. electrical thickness) and the uniformity of the Schottky contact can be evaluated.

**Figure 3.6:** Test structure with two Schottky contacts and one ohmic contact.

**Figure 3.7:** a) C(V) characteristics of a typical MSHM structure measured at 100 kHz (solid) and 1 MHz (dashed). b) 100 kHz characteristics of individual Schottky diodes.
3.3 MISH Capacitor analysis

The typical structure of the investigated MISH capacitors is a circular metal contact placed inside a circular opening of the ohmic contact (Fig. 3.9). Every layer has a capacitance related to the dielectric constant and the thickness of the layer. $C_{\text{pass}}$ is the capacitance of the passivation layer and $C_{\text{barr}}$ is the capacitance of the barrier layer. The total capacitance ($C_{\text{tot}}$) is the capacitance between the gate and the 2DEG which is electrically equivalent to a series connection of $C_{\text{barr}}$ and $C_{\text{pass}}$.

$$C_{\text{tot}} = \frac{C_{\text{pass}} C_{\text{barr}}}{C_{\text{pass}} + C_{\text{barr}}}. \quad (3.4)$$

The C(V) characteristics in this thesis have been extracted using HP4284A and HP4285A LCR meters. These tools measure the admittance response of a small signal voltage excitation at different test signal frequencies ($f_{TS}$) [79]. The capacitance values plotted in this thesis have been extracted from the measured admittance by assuming a model with an ideal capacitor in parallel with a conductance element, i.e. the $C_p$-G model. The conductance element has not been analyzed further in this thesis since a large response of the interface states is detected when studying the capacitance. The capacitance is more straightforward to analyze because the capacitance can be directly

Figure 3.9: Schematic drawing of a typical MISH capacitor evaluated in this thesis.
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transformed to an electrical thickness and be related to the physical location of charge fluctuations.

Fig. 3.10 plots the extracted C(V) for an LPCVD SiN$_x$ passivated Al-GaN/GaN heterostructure (the deposition details will be presented in section 4.1.1). Fig. 3.10a) plots the parallel capacitance extracted from the forward sweep (sweep from depletion at -30 V to barrier accumulation at 20 V). At -30 V the 2DEG below the gate is completely depleted and the capacitance is zero. The first step-like increase of the capacitance, at voltage $V_{2A}$, is where electrons are starting to accumulate in the channel 2DEG. The flat capacitance region with capacitance $C_{\text{tot}}$ is the filling of the channel 2DEG and represents the capacitance of the passivation layer in series with the barrier layer. At $V_{BA}$ the capacitance starts to increase since electrons are starting to accumulate in the barrier of the heterostructure. The passivation capacitance ($C_{\text{pass}}$) is extracted when the curve starts to level out at $V_{PIA}$. In this flat capacitance region an accumulation layer has formed inside the barrier and the passivation interface can be assumed to be fully accumulated. Fig. 3.10b) plots the forward sweep characteristics for three additional $f_{TS}$. The $f_{TS}$ are 1 k, 10 k, 100 k, and 1 MHz where the lowest test signal frequency provides the highest capacitance. Fig. 3.10c) plots the reverse sweep (the sweep from barrier accumulation back to depletion) along with the forward sweep for $f_{TS}=1$ kHz. The hysteresis between the forward and reverse sweeps indicates that there is trapping of electrons during barrier and passivation interface accumulation. Two different hysteresis voltages are extracted, $\Delta V_{BA}$ and $\Delta V_{2A}$ which are the difference between forward and reverse sweep $V_{BA}$ and $V_{2A}$, respectively. Fig. 3.10d) plots the complete measurement with both forward and reverse sweeps for all four $f_{TS}$.

From the definition of capacitance as the relation between charge and voltage an equivalent charge can be extracted from the C(V). An equivalent electron density at a gate bias $V_x$ can be calculated by the integration,

$$n_{C(V_x)} = \frac{1}{q} \int_{V_x}^{\infty} C \, dV,$$

where $q$ is the elementary charge and the integration is performed from a voltage where the 2DEG is deplete. The equations as reported in paper [D] for extracting the state distributions are presented by equations (3.6) to (3.10).

$$N_{\text{fix}} = \left( -\frac{q n_{\text{ref}}}{C_{\text{tot}}} - V_{2A} \right) \frac{C_{\text{pass}}}{q}.$$  

(3.6)

$$N_{\text{slow}} = \left( V_{BA,lf} - \left( V_{2A} + \frac{q n_{\text{ref}}}{C_{\text{tot}}} \right) \right) \frac{C_{\text{pass}}}{q}.$$  

(3.7)

$$N_{\text{disp}} = (V_{BA,hf} - V_{BA,lf}) \frac{C_{\text{pass}}}{q}.$$  

(3.8)

$$N_{\text{hystBA}} = (\Delta V_{BA} - \Delta V_{2A}) \frac{C_{\text{pass}}}{q}.$$  

(3.9)

$$N_{\text{hyst2A}} = \Delta V_{2A} \frac{C_{\text{pass}}}{q}.$$  

(3.10)
Figure 3.10: MISH C(V) characteristics. a) Forward sweep for $f_{TS}=1\,\text{kHz}$ b) Forward sweep for $f_{TS}=1\,\text{k, 10 k, 100 k, and 1 MHz}$. c) Forward and reverse (dashed) sweeps for $f_{TS}=1\,\text{kHz}$. d) Complete characteristics, the inset presents MSHM characteristics.

$C_{\text{barr}}$ of a material is usually known from previous MSHM measurements, as shown in the inset of Fig. 3.10d). When calculating $C_{\text{tot}}$ using (3.4) the result is usually smaller than the measured $C_{\text{tot}}$. The difference is attributed to states at the passivation interface. This can be assumed since: $C_{\text{pass}}$ extracted at different $f_{TS}$ for the same passivation are different; and $C_{\text{pass}}$ extracted using the same $f_{TS}$ for different passivation methods of the same material are different. An accurate value of the passivation capacitance is crucial for accurate extraction of passivation interface state densities. Therefore, the measured $C_{\text{pass}}$ is replaced with the calculated $C_{\text{pass,c}}$ extracted using (3.11).

$$C_{\text{pass,c}} = \frac{C_{\text{barr}}}{C_{\text{barr}} - C_{\text{tot}}}.$$  

(3.11)

A few general comments are necessary concerning MISH C(V) characterization. A characteristic similar to that in Fig. 3.10d) is necessary in order to claim that a somewhat complete picture of the states at the passivation interface has been obtained. Both forward and reverse sweeps have to be measured in order to detect hysteresis due to trapping. There also has to be a clear step in capacitance in the barrier accumulation region to make sure that there has been sufficient barrier accumulation to allow for sufficient trapping of electrons at the passivation interface. Furthermore, extraction at several frequencies are necessary to evaluate the existence of traps with different time constants. For this reason the sweep of the reactively passivated and PECVD passivated samples in paper [D] are not complete since a flat $C_{\text{pass}}$ is not observed in the barrier accumulation region (for RS there was not even an
indication of barrier accumulation at all). The incompleteness of the sweep will prohibit extraction of some interface state densities and will underestimate $\Delta V_{BA}$ and $\Delta V_{2A}$ densities since there is no guarantee that all states at the passivation interface were filled. The completeness of the sweep, in combination with relatively low interface state densities, was the primary reason why the LPCVD passivation was considered to be most promising for surface passivation.

In paper [D] it was also shown how to relate characteristic time of the sweep to activation energies of the traps. This will not be employed in the experiments presented in this thesis since the extraction is based on assumptions regarding trap capture cross-section. It will be satisfactory just to compare magnitudes of the values extracted from equations (3.6) to (3.10).

### 3.3.1 MISH capacitor simulation

The MISH structure has been implemented in the same TCAD software as was used for extracting the band diagrams presented earlier (Sentarus by Synopsys). The ACCoupled solver is used which solves the Poisson equation coupled with the current continuity equations for the large gate voltage sweep as well as an AC signal measurement at each sweep bias, i.e. after finding the steady state solution at each defined gate bias the complex small signal admittance is extracted from the current response of a small signal voltage [23]. The simulation mimics how a LCR meter operates with the exception that the LCR meter does not, necessarily, “wait” for thermal equilibrium before the admittance parameters are measured. Hence, hysteresis type dynamics detected in the experimental measurements are not possible to reproduce using the simulator.

A very simplified model is used for the examples in this thesis. The difference in polarization between AlGaN and GaN is modeled with a positive interface charge at the channel interface. The simulator, which is constrained by the Poisson equation and electron and hole continuity equations, will ”automatically” create a 2DEG with a density of electrons equal to the positive channel interface charge. The model is far from physically complete but will be shown to provide results that are remarkably similar to what is observed experimentally. As a note, the model is simplified but not far fetched since it can be thought to describe a case where the negative polarization charge at the AlGaN surface is neutralized by surface donors that will be positively charged when they have donated their electron to the 2DEG [29]. Fig. 3.11 presents four different simulations where four different quantities have been varied, $f_{TS}$ is 1 kHz if not otherwise stated.

In the simulation presented in Fig. 3.11a) the positive charge at the passivation interface is varied, which is equivalent to varying $n_s$ when using this simplified model. $V_{BA}$ is the same for all three different channel interface charge densities, which is where electrons start to accumulate in the barrier. The channel interface charge is obtained when integrating the C(V) curve. In Fig. 3.11b) the influence of a fixed positive or negative charge at the passivation interface is investigated. The charge is seen to shift the characteristics in positive voltage direction for negative charge and in the negative voltage direction for positive charge. Fig. 3.11c) plots C(V) simulated with differ-
3.3. MISH CAPACITOR ANALYSIS

Figure 3.11: TCAD simulations where a parameter of the simulation is varied: a) the positive charge at the channel interface, b) a fixed charge at the passivation interface c) different densities of an acceptor trap with emission rate 500 s\(^{-1}\) d) the same acceptor trap but simulated with different \(f_{TS}\).

Different densities of a passivation interface acceptor trap. The density is set to 0, 2\(\times\)10\(^{12}\), or 4\(\times\)10\(^{12}\) cm\(^{-2}\). The energy of the trap is defined at 0.5 eV below the conduction band and the trap is defined with a constant emission rate of 500 s\(^{-1}\). When electrons start to accumulate in the barrier they will immediately start to be trapped. Since \(f_{TS}\) is comparable to the trap emission rate some trapped electrons will have time to emit with the test signal while others remain trapped, explaining the stretched capacitance compared to the \(C(V)\) for the simulation without the trap. Furthermore, the Fermi level will be pinned at the trap level until the trap state is completely filled, explaining the sudden drop in capacitance before the \(C(V)\) behavior returns to that of the barrier accumulation process. Fig. 3.11(d) plots simulations for different \(f_{TS}\) with the same acceptor trap as previously defined. For the \(f_{TS}=1\) kHz some captured electrons have time to emit during the test signal excitation while others remain trapped. When the frequency is significantly higher than the emission rate, electrons will be trapped but will not have time to emit with the variation of the test signal. Finally for a \(f_{TS}\) significantly lower than the trap emission constant the electron will be trapped and will have time to emit with the signal variation. For this case the capacitance directly steps up to the passivation capacitance since the trap is located directly at passivation interface. When the trap is filled the capacitance briefly drops down to \(C_{tot}\) before the capacitance increases due to barrier accumulation. The basic assumptions made with equations (3.6) to (3.10) with regards to the general behavior when an electron is trapped at the passivation interface has been verified.
3.4 Pulsed I(V)

Pulsed characterization is commonly employed to investigate trapping in the form of lag effects [80]. The most common lag metric is the slump ratio which compares the current when pulsing from a bias where surface traps are filled to the current that is pulsed from a bias where trapping is negligible. From experimental point of view it is important that the quiescent bias \((QB(V_{GS},V_{DS}))\) is not resulting in significant steady-state currents, since a current may empty traps or otherwise disturb the measurement.

\(QB_0=QB(0,0)\) is often used as the ”trap-effect-free” characteristic. Current output from other biases are then compared with the current from \(QB_0\) to measure lag effects. Gate lag is measured when the device is pulsed from a bias with \(V_{DS}=0\) V and a negative bias is applied to the gate. Most often the gate lag will increase as the gate is biased more and more negatively until the lag effect saturates. With the gate biased below the pinch-off voltage a non-zero drain voltage can be applied without drain current and a combination of gate and drain lag is measured. The bias is designated \(QB_{CB}\), since it resembles a bias used for class B operation. Normally the lag increases as \(V_{DS}\) of the \(QB_{CB}\) increases since there is a higher electric field in the gate to drain region, allowing for trapping of more electrons. It is only under very special circumstances, like for the sample passivated with the highest strike power of paper [F], that the lag behavior does not follow the general behavior.

It is not uncommon to use the pulsed characterization as an indication regarding the elimination of traps at the passivation interface. However it was claimed in paper [F] that lag-free characteristics are not equivalent to a trap-free passivation interface. There remains some work to solidify the connection between the features of the MISH capacitor to the lag of devices. Lag-free operation, with or without states at the interface, is of course necessary for practical operation of HFETs. However it is reasonable to assume that states that exist at the passivation interface, even if they do not result in current collapse, may have detrimental effects during other operation conditions.

3.5 Epitaxial wafer surface roughness

As was shown in paper [C] the surface roughness of the AlGaN/GaN heterostructure material can be quite different between materials, even when the epitaxial grown was performed at the same occasion. On about 25% of delivered wafers there is a very prominent large aspect ratio surface roughness which is often having a hexagonal surface morphology.

Fig. 3.12 shows the surface roughness of two epi-wafers that were grown on 3-inch 4H semi-insulating SiC substrates cut from the same SiC boule (delivered by Cree Inc.). The epitaxial layer specification of both wafers is the same but the growth was performed in two separate growth-runs. The surface orientation (SO) of the two wafers is 0.05° (specified by the substrate supplier). The plot shows five measurements at different locations of each wafer: one measurement at the center of the wafer; and one measurement 20 mm away from the center in each direction. The similarity between the roughness of the two wafers is apparent: both have a region with a prominent roughness at the same area of the wafer while the rest of the wafer is smooth.
The mixed roughness by itself is quite unusual since most measured wafers are either rough or smooth. These wafers with SO=0.05° should, according to the statistical data presented in paper [C], have the hexagonal roughness. The similarity of the surface roughness of these two wafers further proves that the roughness is related to the substrate.

The quite surprising conclusion in paper [C] was that the extreme roughness had no significant influence on any of the investigated electrical characteristics. However, there are still some interesting aspects of the surface roughness that has not been investigated. These are related to MMIC processing where one of the unanswered questions are if the roughness may affect the passive components of the circuits. It is thus highly recommended to keep track of this kind of prominent surface roughness.

Figure 3.12: Surface roughness on five locations of two different wafers. Each OSP measurement area is 300 by 230 \( \mu \text{m}^2 \) and the height difference between white and black is about 60 nm.
Chapter 4

Passivation dielectrics and passivation characterization

Passivation is of crucial importance for AlGaN/GaN devices in order to reduce dispersion and other trapping related phenomena. Many different passivation schemes have been evaluated by several different research groups in order to find a passivation that provides stable and reliable HFETs. The most commonly used type of dielectric is silicon nitride, which can be deposited in many different ways: PECVD [81,82], reactive sputtering [83], catalytic CVD [84], electron-cyclotron resonance CVD [85], LPCVD [86], remote plasma CVD [87], and in-situ CVD [88]. Other types of dielectrics are for example: SiO$_2$ [81], SiO$_x$N$_y$ [89], and HfO [90]. The sheer amount of investigations reporting on the surface passivation of the AlGaN/GaN heterostructure indicates that this is an extremely critical part of the AlGaN/GaN HFET technology.

4.1 Low pressure chemical vapor deposition SiN$_x$

The LPCVD process relies on the formation of SiN$_x$ through a reaction between dichlorosilane (DCS, SiCl$_2$H$_2$) and ammonia (NH$_3$) at low pressure (100-500 mTorr) and high temperature (750 – 830 °C). The reaction process for Si$_3$N$_4$ is presented in reaction chain (4.1) [91].

$$3 \text{SiCl}_2\text{H}_2 + 4 \text{NH}_3 = \text{Si}_3\text{N}_4 + 6 \text{HCl} + 6 \text{H}_2$$

(4.1)

The LPCVD process has been developed for microelectronic fabrication where it is preferred since it is a uniform process that can be deposited on many wafers at the same time [91].

There are a few basic motivations for exploring the LPCVD SiN$_x$ for surface passivation. One motivation is that deposition of a SiN$_x$ passivation layer before the ohmic contact annealing process will prevent the degradation of $R_{sh}$ caused by the annealing [92]. A second more speculative motivation is that a passivation that is deposited at a high temperature will be less likely to degrade during high power operation. Channel temperatures of 250 °C has been reported [93] which is higher or comparable to the deposition temperatures of several other passivation deposition methods.
4.1.1 Influence of deposition parameters

The deposition parameters of the LPCVD constitute a large parameter space: the precursor flow rates, the deposition temperature \( (T_{\text{dep}}) \), the deposition pressure \( (p_{\text{dep}}) \), and the deposition time \( (t_{\text{dep}}) \) may be varied. The relative content of DCS to NH\(_3\) will determine the stochiometric relation between Silicon and Nitrogen in the SiN\(_x\). Changing temperature and pressure will affect the deposition rate and may affect the density of the SiN\(_x\) which will result in different stress in the passivation layer [94].

The deposition parameters are described in Table 4.1 together with extracted film properties. Three samples are deposited at 770 \(^\circ\)C with different precursor gas flow rates, resulting in refractive indices spanning from approximately 2.0 to 2.2. Each sample is designated according to the refractive index of its passivation (DP20-DP23). The fourth sample is deposited with the same flow ratio as DP22 but at a higher temperature, resulting in an even higher refractive index, designated DP23. The stresses in the different films were measured on silicon wafers deposited at the same time as the samples. The positive stress values represent tensile stresses which for DP20 and DP21 is higher than other reported values [82] while DP23 is almost stress-free.

<table>
<thead>
<tr>
<th>T(_{\text{dep}}) [(^\circ)C]</th>
<th>DCS:NH(_3)</th>
<th>(d_{\text{pass}}) [(\AA)]</th>
<th>n</th>
<th>Stress [MPa]</th>
</tr>
</thead>
<tbody>
<tr>
<td>DP20 770</td>
<td>23:137</td>
<td>620</td>
<td>2.01</td>
<td>1310</td>
</tr>
<tr>
<td>DP21 770</td>
<td>80:80</td>
<td>650</td>
<td>2.07</td>
<td>1150</td>
</tr>
<tr>
<td>DP22 770</td>
<td>137:23</td>
<td>550</td>
<td>2.24</td>
<td>405</td>
</tr>
<tr>
<td>DP23 820</td>
<td>137:23</td>
<td>600</td>
<td>2.34</td>
<td>87</td>
</tr>
</tbody>
</table>

C(V) and I(V)

Fig. 4.1a) to d) plots the MISH C(V) characteristics of each sample and Fig. 4.2a) and b) plots the integrated charge and MISH-I(V), respectively. The characteristics are visually very different, the largest differences and similarities are:

- Sample DP20 has a large semi-permanent shift of the characteristics seen when comparing the forward sweep of the first measurement with all subsequent measurements (the first and second measurements are presented in the figure).

- Disregarding the semi-permanent hysteresis, DP20 and DP21 are quite similar with large \(\Delta V_{\text{BA}}\) hysteresis indicating large quantities of traps. The I(V) shows that both dielectrics are highly resistive.

- DP22 and DP23 are quite similar with no hysteresis at all. However, both samples have a much lower resistivity. The very low resistivity of DP23 is causing the peak around \(V_{2A}\) for \(f_{\text{TS}}=1\)kHz in Fig. 4.1d).

The extracted trap densities using (3.6) to (3.10) are presented in Table 4.2.
Figure 4.1: MISH C(V) forward (solid) and reverse (dashed) 1 kHz, 10 kHz, 100 kHz, and 1 MHz characteristics for DP20 to DP23. For DP20 the first and second measurements are plotted for which the forward sweeps are identified by the numbers.

Figure 4.2: a) Integrated charge and b) MISH capacitor I(V).
Chapter 4. Passivation Dielectrics and Passivation Characterization

Table 4.2: Summary of different states extracted using the MISH capacitor formulae. $C_{barr} = 390 \, \text{nF/cm}^2$ and $n_{ref} = 10 \times 10^{12} \, \text{cm}^{-2}$. All quantities in the table are given in units of $[\times 10^{12} \, \text{cm}^{-2}]$.

<table>
<thead>
<tr>
<th>Sample</th>
<th>$N_{fix}$</th>
<th>$N_{slow}$</th>
<th>$N_{disp}$</th>
<th>$N_{hystBA}$</th>
<th>$N_{hyst2A}$</th>
<th>$n_{C(0)}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>DP20</td>
<td>+4.4</td>
<td>1.0</td>
<td>0.8</td>
<td>4.6</td>
<td>6.0</td>
<td>13.3</td>
</tr>
<tr>
<td>DP21</td>
<td>+4.9</td>
<td>1.8</td>
<td>1.5</td>
<td>6.7</td>
<td>0.7</td>
<td>13.5</td>
</tr>
<tr>
<td>DP22</td>
<td>+1.3</td>
<td>0.7</td>
<td>0</td>
<td>1.2</td>
<td>0.3</td>
<td>10.4</td>
</tr>
<tr>
<td>DP23</td>
<td>+1.0</td>
<td>0.6</td>
<td>0</td>
<td>1.3</td>
<td>0.2</td>
<td>10.3</td>
</tr>
</tbody>
</table>

The extracted trap densities confirm what has already been stated, DP20 has large densities of $N_{hyst2A}$ and $N_{hystBA}$ traps. DP21 has a lower quantity of $N_{hyst2A}$ traps but larger quantities of $N_{hystBA}$ and $N_{disp}$ traps. DP22 and DP23 have generally lower trap densities. The $n_{C(0)}$ of DP20 and DP21 are almost identical and larger than those of DP22 and DP23.

Hall

The measured Hall parameters are presented in Table 4.3. The difference between the samples is small but a trend can be extracted. Comparing $n_{meas}$ with $n_{C(0)}$ from Table 4.2 it is possible to see that the values for DP22 and DP23 agree quite well, while the $n_{C(0)}$ values of DP20 and DP21 are higher than $n_{meas}$. The mobilities of DP20 and DP21 are also lower than the mobilities of DP22 and DP23. These results indicate that there is small effect of two layer conduction in DP20 and DP21.

Table 4.3: Hall parameters for samples DP20 to DP23.

<table>
<thead>
<tr>
<th>Sample</th>
<th>$R_{sh}$ [Ω/sq]</th>
<th>$n_{meas}$ [cm$^{-2}$]</th>
<th>$\mu_{meas}$ [cm$^2$/Vs]</th>
</tr>
</thead>
<tbody>
<tr>
<td>DP20</td>
<td>392</td>
<td>10.6</td>
<td>1500</td>
</tr>
<tr>
<td>DP21</td>
<td>383</td>
<td>10.5</td>
<td>1540</td>
</tr>
<tr>
<td>DP22</td>
<td>387</td>
<td>10.3</td>
<td>1560</td>
</tr>
<tr>
<td>DP23</td>
<td>389</td>
<td>10.0</td>
<td>1590</td>
</tr>
</tbody>
</table>

Summary

The semi-permanent shift of DP20 was also observed for the LPCVD passivated sample of paper [D]. Hence it is concluded that using a nitrogen rich LPCVD SiN$_x$ will result in semi-permanent electron trapping. The shift caused by the trapped electrons will neither recover when biasing the capacitor structure in depletion nor after a few days of rest. Tests at elevated temperatures indicate that the trapped electrons are emitted when the sample is heated to about 200°C. It is possible that the traps are inherent to the bulk SiN$_x$ like in silicon nitrides used for charge-trap flash memories [95, 96].

The resistivity of the LPCVD SiN$_x$ is closely related to the relative content of DCS and NH$_3$ during deposition. DP22 and DP23 have a much lower resistivity which is due to a higher silicon content in the SiN$_x$ [97]. Furthermore, the current leakage through DP23 is comparable to the current through
4.2 Reactively sputtered SiN$_x$

a Schottky diode. This passivation may, therefore result in an increase of gate current.

The advantages (+) and disadvantages (-) for each sample is listed below.

- DP20: -large semi-permanent trap density; -generally large trap densities; -barrier conduction; +high SiN$_x$ resistivity.
- DP21: -largest densities of $N_{\text{hystBA}}$ and $N_{\text{disp}}$ traps; -barrier conduction; +high SiN$_x$ resistivity.
- DP22: +low density of interface states; +no barrier conduction; -low SiN$_x$ resistivity.
- DP23: +low density of interface states; +no barrier conduction; -too low SiN$_x$ resistivity.

The conclusion is that DP22 is most suitable for passivation of the Al-GaN/GaN heterostructure, even though a higher SiN$_x$ resistivity would be desirable. The conclusion of this experiment was utilized for selecting the deposition parameters of the LPCVD SiN$_x$ utilized in paper [C], where the deposition was performed with DCS:NH$_3$ flow ratio of (5:1). This provided a SiN$_x$ layer with higher resistivity and interface state densities comparable to DP22. At this stage the physical explanation for the differences in interface state densities is not known. The difference could be explained by a difference in refractive index or stress. More experiments are necessary to identify the physical explanation.

The reactively sputtered passivation (RS) has been deposited on several different heterostructures. For example it was used in the illumination study of paper [E]. The RS passivation can result in very good performance but a problem with reproducibility is sometimes experienced. While passivation using LPCVD SiN$_x$ provides almost identical characteristics from run to run, passivation by RS SiN$_x$ can result in quite different characteristics. This is not necessarily due to the intrinsic properties of the RS passivation, but may to a large extent explained by the process flow. The RS nitride is deposited after the ohmic contact annealing. The annealing will affect the heterostructure by reducing $n_s$ and there is no guarantee that the annealing affects two samples in the same way. Even though the RS passivation process always appears to make the sample more uniform it can not compensate for the complete effect of the annealing. Furthermore, the passivation process starts with a 30s surface Ar-plasma cleaning step, possibly introducing surface damage similar to that discussed in paper [F].

In paper [E] the MISH C(V) was also extracted with the sample illuminated from the backside. In Fig. 4.3 the MISH C(V) characteristics of the RS sample used in the paper is plotted for three different illumination conditions: a) non-illuminated characteristics, b) top-side illuminated, c) backside illuminated, and d) all together. The non-illuminated characteristic has large hysteresis due to trapping in the barrier accumulation region. The top-illuminated characteristic has a much smaller hysteresis and it is possible to see that the reverse
characteristic at $V_{2A}$ is less abrupt. The slightly smeared out characteristic is due to gradual emission of trapped electrons as the reverse sweep is progressing towards depletion. The illumination from the top side appears to spread out under the gate contact and assist in emitting trapped electrons. This is an example that also shows that under the right circumstances the interface states can also be analyzed in the $V_{2A}$-interval as has been reported by Mizek et al. [64]. Illumination from the backside results in very different characteristic. There is no longer any hysteresis which is attributed to the illumination emptying traps that are captured during passivation accumulation. The $V_{2A}$ voltage measurements using backside illumination is more negative than for the non-illuminated measurement, which is attributed to emission of very deep traps that would otherwise have too long emission times to be emitted during the non-illuminated characterization. The difference in forward $V_{2A}$ of the non-illuminated and backside illuminated sweep corresponds to a charge of $1.9 \times 10^{12}$ cm$^{-2}$.

This method of characterization could be interesting from MISHFET point of view since illumination from different angles could have a large effect on trapping/de-trapping at the gate dielectric/barrier interface.

**Figure 4.3:** 10 kHz MISH C(V) of a RS passivated sample measured under different illumination conditions. a) Non-illuminated, b) top side illuminated, c) backside illuminated, and d) all measurements.


Chapter 5

HFET fabrication and MISHFET characterization

5.1 HFET fabrication process

The HFET fabrication process as can be divided into five main processing steps. The steps are listed below with a short motivation for each step. Each main step is divided into several process-steps which are reported inside parentheses. Each process step may then be further divided into fundamental steps of the type: apply resist, bake resist, expose resist, develop resist, ashing of resist etc.

1. Isolation: Since the as-grown material is basically a conductive sheet, discrete structures have to be isolated from each other in order to avoid short circuits and/or parasitic conduction paths. Furthermore the removal of conducting material decreases parasitic capacitances. (Photo lithography (PL), dry etch)

2. Ohmic contacts: Provide low loss connections to the channel 2DEG. (PL, metalization by lift-off, annealing for contact formation)

3. Passivation: A necessity to impede trapping related phenomena. (Passivation deposition, PL, passivation opening at contacts by dry etching)

4. Gate electrodes: Deposition of a Schottky contact in order to modulate the density of the 2DEG in the channel below the contact. Also includes the removal of the passivation below the gate. (PL or electron beam lithography (EBL), passivation opening by dry etch, PL/EBL, metalization)

5. Pad metalization: Deposition of large area contacts that enables probing of ohmic and gate contacts. In some cases the pads can be deposited in the gate electrode step, in those cases this step is redundant. (PL, metalization)

This is also the process flow reported in most papers describing fabrication of HFETs. However, using the LPCVD deposition requires a different process-flow since the LPCVD furnace must not be used any metalizations since these
may contaminate the deposition furnace. For the LPCVD process the passivation is deposited first, known as early passivation or passivation first. When using the LPCVD process, the HFET process is simplified by one lithography step since opening of the passivation can be made using the same mask as for the deposition of the ohmic metalization, i.e. a self aligned ohmic contact.

One of the process steps having the largest influence on the heterostructure characteristics is the ohmic contact annealing, which has been shown to cause significant increase of $R_{sh}$ [92].

### 5.1.1 Ohmic contacts and annealing

Annealing Ti/Al/Ni/Au [98] or Ti/Al/Mo/Au [99] metal stacks at temperatures around 800°C is one of the most commonly employed methods to form ohmic contacts. A few different theories explaining the physical mechanism of ohmic contact formation have been presented. The out-diffusion of nitrogen from the AlGaN resulting in nitrogen vacancies acting like donor states has been presented as a possible reaction [100]. Other contributing mechanisms may be spiking, where the ohmic metal penetrates the barrier through defect states in the AlGaN barrier [101].

Apart from Ti/Al-based ohmic contacts, there has also been work presented on Ta based contacts [102] which can be made ohmic at a lower annealing temperature (575°C). Furthermore, the reduction of contact resistance by introducing a thin layer of Si at the bottom of the Ti/Al/Ni/Au stack has been demonstrated [103].

A completely different fabrication approach, avoiding the process of alloying a metal stack, is the fabrication of ohmic contacts by ion implantation of Si into the ohmic contact region of the heterostructure [104]. The implantation process does however include an activation annealing step at temperatures exceeding 1200°C [104,105], allowing for the same degradation as for the ohmic contact annealing.

Fig. 5.1 presents the Hall characteristics of three different heterostructure

![Figure 5.1: Hall characteristics for three different materials annealed at different temperatures.](image-url)
Table 5.1: \( n_s \) and epitaxial structure of the three different structures used for the annealing experiment (\( t = \)thickness of layer).

<table>
<thead>
<tr>
<th>Layer</th>
<th>Structure</th>
<th>H1</th>
<th>H2</th>
<th>H3</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Nucleation layer</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>GaN</td>
<td>GaN</td>
<td>GaN</td>
<td>GaN</td>
</tr>
<tr>
<td>2</td>
<td>Al(_{22})%GaN</td>
<td>18</td>
<td>18</td>
<td>19</td>
</tr>
<tr>
<td></td>
<td>t [nm] 20</td>
<td>20</td>
<td>20</td>
<td>20</td>
</tr>
<tr>
<td>3</td>
<td>Al(_{25})%GaN</td>
<td>1540</td>
<td>2030</td>
<td>1860</td>
</tr>
<tr>
<td></td>
<td>( R_{sh} ) [( \mu )m]</td>
<td>462</td>
<td>316</td>
<td>302</td>
</tr>
<tr>
<td></td>
<td>( n_s ) [( \times 10^{12} ) cm(^{-2})]</td>
<td>8.79</td>
<td>9.74</td>
<td>11.1</td>
</tr>
<tr>
<td></td>
<td>( \mu_{\text{meas}} )</td>
<td>1540</td>
<td>2030</td>
<td>1860</td>
</tr>
</tbody>
</table>

The epitaxial layer structures and the Hall parameters of the as-grown materials are presented in Table 5.1. The samples were first annealed and then contacted using the gallium ohmic contacts of paper [A] i.e. the samples are annealed without any metals on top of the heterostructure. For H1 a small effect of the annealing is experienced already at 500 °C and at 650 °C the sheet density of all materials has already decreased by about 10-20%. However the decrease is only resulting in a small increase of \( R_{sh} \) since \( \mu_H \) is increasing at the same time. After annealing at 800 °C the effect is also prominent for H2 with a significant increase of \( R_{sh} \). Annealing at 850 °C resulted in even larger decrease of \( n_s \) now also for H3.

At the highest annealing temperature all three samples have been affected to a large degree. The larger sensitivity at lower annealing temperature of H1 can be explained by the lack of an AlN exclusion layer. The difference in sensitivity of H2 and H3 is not obvious, it could be the lower aluminum concentration in the barrier of H2. The difference could also be due to different epi-growth parameters since these materials are not from the same exp-wafer supplier.

Reducing the resistance of ohmic contacts by recess etching has also been investigated and implemented [106]. The recess etch has been especially effective for reducing the contact resistance to heterostructures containing an AlN exclusion layer [107]. An etch process was developed in paper [B] by utilizing the MSHM characterization presented in Chapter 3.

When utilizing a process flow with early passivation i.e. the LPCVD process, there may be problems of the edge of the ohmic contact becoming rougher than for normally processed ohmic contacts. The reason is not clear, but has to be related to some reaction between the SiN\(_X\) and one of the metals in the ohmic metal stack. Different methods to improve the edge acuity of the ohmic contact when working with an early passivation process has been reported [108]. However, the ohmic contact process is not always reported to be problematic [109]. In this work there is sometimes no problem with the edges of the ohmic contact, at other times outflowing of the ohmic contacts results in total loss of yield.
5.2 MISHFET

Depending on the choice of gate dielectric there are a few different fabrication process possibilities. The most recent publications concerning MISHFET/MOSHFET fabrication utilize atomic layer deposition (ALD) deposited oxides [110]. ALD can be deposited at low temperatures making it compatible with the present HFET process since the dielectric may be deposited directly after the gate passivation opening.

Silicon nitride has also been used in several reports for gate insulation [56]. In this work SiN$_x$ deposited by LPCVD is used for gate dielectric deposition as well as surface passivation. The gate dielectric is required to be deposited before any metalizations as discussed previously. Hence the gate passivation opening step is moved and performed directly after the mesa isolation step.

The process flow for the fabrication of the MISHFET is:

1. Passivation
2. Isolation: (PL, dry etch)
3. Gate passivation opening: (PL/EBL, dry etch)
4. Gate dielectric deposition
5. Ohmic contacts: (PL, dry etch, evaporation, lift-off)
6. Gate: (PL/EBL, ebeam evaporation, lift-off)
7. Pad: (PL, metalization, lift-off)

It is the same number of steps as for the early passivation HFET process. Furthermore, the process is easily extended with a gate recess etch inserted as a part of the gate passivation opening step, which has been done in the process described below.

5.2.1 MISHFET fabrication

In the following section the fabrication of gate-recessed, gate insulated HFETs is described. The sample was first surface passivated using a 50 nm thick LPCVD SiN$_x$ deposited at 820° C and 250 mTorr with a DCS:NH3 ratio of 5:3.

After device isolation the gate footprint was opened and a gate recess etch was employed to reduce the channel to gate distance, the gate footprint was etched to a length of about 1 μm, which will be the gate length of the MISHFET. The etch recipe was the same as reported in paper [B], i.e. Cl/Ar based ICP/RIE with 25W power. The recess etch time ($t_{RE}$) was set to 15, 25, 35, and 45 s. Parts of the sample was etched in two steps with the longest total etch duration adding up to 70 s. Equation (5.1) is used to extract the ratio of barrier etched ($RBE$).

$$RBE = \frac{d_{RE}}{d_{B0}} = 1 - \frac{C_{B0}}{C_{BE}}$$  \hspace{1cm} (5.1)

where $C_{B0}$ is the capacitance of the non-etched barrier and $C_{BE}$ is the capacitance of the etched barrier as defined in Fig. 5.2a). Figure 5.2b) shows the
RBE against etch duration. The ratio has been calculated by using equation (5.1). The open circles represent the RBE for gates recess etched once, and the closed circles represent gates recess etched twice. The etch delay is shorter than was observed for the material in paper [B], which can be due to a thinner surface oxide for this material compared to the material in paper [B] since the etch delay has been identified to be due to slowly etching surface oxides [111]. It is also observed that the gates etched a second time are affected by an additional etch delay, indicating that the etched areas will oxidize in the short time interval (2 to 5 minutes) the samples are in air in between separate etches.

After the gate recess etching the sample was annealed up to a maximum of 800 °C in order to cure possible plasma induced damage of the recessed AlGaN. Annealing has been reported to reduce plasma induced damage [112] and was also used to reduce the effect of the plasma strike power in paper [F]. The utilized process flow, where the chemically and thermally stable LPCVD surface passivation protects everything except the gate footprint, allows for a large number of different cleaning processes as well as thermal processes where only the gate recessed region is affected.

The gate dielectric deposition time was determined from an earlier characterization run where the electrical thickness versus deposition time was extracted using capacitance of MISHIM structures (MSHM structure with thin insulator layer). Fig. 5.3(left) plots the passivation extracted from that experiment versus deposition time, where a dielectric constant of 7.5 has been used to transform the electrical thickness to physical thickness. The extrapolated thickness at t=0 is 2.5 nm which is partly due to a delay during the pre-deposition step where the stability of the gas flows are monitored before the deposition timer is started. The gate insulator was deposited at \( T_{\text{dep}} = 770 \) °C, \( p_{\text{dep}} = 120 \) mTorr and with a DCS:NH\(_3\) flow ratio of 1:4. A nitrogen rich SiN\(_x\) was utilized in order to make sure that the gate insulation would have a high resistivity. The gate dielectric thickness was extracted to be about 5 nm.

A 2 μm long gate contact of Ni/Au was defined by photo lithography and ebeam evaporation. The ohmic contact process which utilized recess-etched ohmic contacts with a Ti/Al/Ni/Au based ohmic metal resulted in \( r_c = 0.3 \) Ω·mm. After the ohmic contact process the remaining steps are trivial.
CHAPTER 5. HFET FABRICATION AND MISHFET CHARACTERIZATION

Figure 5.3: a) Schematic showing the MISHFET device. b) Thickness of LPCVD SiN$_x$ versus short $t_{\text{dep}}$ extracted from MISHIM measurements.

5.2.2 MISHFET electrical characteristics

In Fig. 5.4a) and b) the drain current and transconductance are plotted for different $t_{\text{RE}}$, respectively.

In Fig. 5.5a) and b) $V_{\text{PO}}$ and $g_m$ extracted from the transfer characteristics are plotted versus $t_{\text{RE}}$. In Fig. 5.5b) the same extractions are plotted versus $R_{\text{BE}}$. The pinch of voltage of the non-etched device is -5 V. As the recess is etched deeper $V_{\text{PO}}$ is becoming less negative, somewhere in the range of $R_{\text{BE}}$=0.7-0.86 there is no longer a channel 2DEG for the non-biased gate and device operation changes from depletion mode to enhancement mode. For the longest etch duration the pinch-off voltage, or threshold voltage, is 0.6 V. $g_m$ is seen to increases as the gate to channel distance decreases, until it peaks at 290 mS/mm for $R_{\text{BE}}$=0.6 after which it decreases to 120 mS/mm for the enhancement mode device.

The gate current measured on circular gate diodes for $t_{\text{RE}}$=0, 45 s and 35+45 s are plotted in Fig. 5.6a). A reference sample from the same epitaxial structure with a similar LPCVD surface passivation but without gate insulation or gate recess is also plotted for comparison. The gate current is lower by

Figure 5.4: a) $I_{DS}$ as a function of $V_{GS}$ measured on one device of each $t_{\text{RE}}$, and b) extracted $g_m$. 
at least two orders of magnitude for the insulated gate devices. Figure 5.6b) plots the pulsed I(V) characteristics of a device with \( t_{RE}=25 \) s. The solid characteristic is the curve measured from \( QB_0 \) while the dashed curve is measured from \( QB_{CB}=QB(-7,20) \) with a slump ratio of 80-90\% which is acceptable.

These results indicate that the LPCVD Si\(_x\) can also be utilized as a gate insulator for MISHFET type devices. It can also be used in combination with a gate recess etch in order to: either maintain the electrical distance between the gate and the channel to avoid short channel effects; or fabricate normally-off transistors. The important evaluation of high frequency and power performance remains to be done.

**Figure 5.5:** Extracted \( V_{PO} \) (circles) and \( g_m \) (squares) versus: a) etch duration, and b) \( RBE \). The dashed lines are visual guides for \( V_{PO} \) and the dash-dotted lines are visual guides for \( g_m \).

**Figure 5.6:** a) \( I_G \) for \( RBE=0, 0.52, \) and 0.86 and reference sample. b) Pulsed I(V) for device with \( t_{RE}=25 \) s, pulsed from \( QB_0 \) (solid) and \( QB_{CB} \) (dashed).
Chapter 6

Summary of appended papers

The major part of the writing of the appended papers have been executed by the first-name author, however the author has had invaluable help by discussing formulations with contributing authors.

**Paper A**

**A room temperature HEMT process for AlGaN/GaN heterostructure characterization**

The paper describes a method to swiftly screen heterostructure materials. The process is also used to monitor the effect of fabrication processing steps on fundamental heterostructure characteristics.

Processing, measurements, and writing were done by the author.

**Paper B**

**Optimization of recessed ohmic contacts for AlGaN/AlN/GaN heterostructures using C(V) characterization of MSHM structures**

The use of C(V) measurements on MSHM for developing shallow barrier etch recipes is presented. The recess etch is used to develop an etch recipe for reducing the contact resistance to an AlGaN/AlN/GaN heterostructure. Earlier publications stating that minimum contact resistance is obtained when 1-2 nm remains of the barrier are verified.

Processing, characterization, and writing was done by the author.

**Paper C**

**Influence of large aspect ratio surface roughness on electrical characteristics of AlGaN/AlN/GaN HFETs**

The influence on heterostructure electrical characteristics surface roughness with clear hexagonal morphology was investigated. The roughness is observed on about 25% of wafers and it is caused by the growth being based on SiC
substrates with a surface orientation close to 0°. Test structures and HFETs fabricated on one rough and one smooth wafer are compared. The roughness appears to only have negligible effect on the electrical properties of the heterostructure. No effect of the roughness was detected on HFET DC, RF, or reliability characteristics.

Processing, characterization, and writing was done by the author. The x-ray diffraction analysis and the text describing the analysis was performed by contributing authors at Linköping University.

Paper D

Investigation of the interface between silicon nitride passivations and AlGaN/AlN/GaN heterostructures by C(V) characterization of metal-insulator-semiconductor-heterostructure capacitors

Reports on the use of MISH C(V) characterization to probe the density of interface states at the interface between a passivation and the AlGaN/GaN heterostructure. The MISH C(V) analysis is applied to an investigation of three different SiNx passivation methods: LPVCD, PECVD, and RS. All passivations have significant trap densities, but the LPCVD is concluded to best suited for passivation.

The processing, measurements, and writing of the MISH capacitor related discussion were done by the author. The statements concerning epitaxial growth was written by contributing authors at Linköping

Paper E

Illumination effects on electrical characteristics of GaN/AlGaN/GaN heterostructures and HFETs and their elimination by LPCVD silicon nitride passivation

The illumination sensitivity of differently processed GaN/AlGaN/GaN heterostructures are investigated. The illumination sensitivity of non-passivated and annealed materials is seen to be extremely large, which was proposed to be due to generation of large quantities of surface states during annealing of the non-passivated material.

Processing, characterization, analysis, and writing was done by the author.

Paper F

Analysis of the effect of plasma power during ICP-PECVD SiNx passivation of AlGaN/GaN heterostructures by utilizing a two-layer conduction model

High plasma power during the initial stage of IC-PECVD passivation is shown to result in large redistribution of charge from the channel to the barrier of the heterostructure.

Processing, characterization, analysis and writing was done by the author.
Chapter 7

Conclusions and future work

The main contributions of this thesis are:

1. The development of methods for characterizing and analyzing process induced effects and reliable passivations for dispersion-free microwave HEMTs.

   The effect of surface passivation on the heterostructure transport properties has been characterized using Hall characteristics. At times the Hall analysis had to be extended with two layer conduction model in order to correctly interpret the Hall measurements due to significant charge transfer in an accumulation layer in the barrier.

   A more direct measurement and analysis of the passivation is by C(V) characterization of MISH capacitors. Procedures to measure and extract passivation interface state densities have been presented in this work.

   These methods have been used to investigate the influence of illumination conditions and plasma-induced damage. Illumination conditions are found to have a profound effect on device performance, which is often disregarded in many reports. Illumination insensitive HFETs have been demonstrated using a LPCVD SiN$_x$ passivation.

   Passivation using plasma assisted deposition methods have been shown to result in large positive charge at the passivation interface. Also, when applying increasingly larger plasma power during the initial stage of passivation deposition the result is an increasingly large redistribution of charge from the channel to the barrier of the heterostructure.

   Different methods and parameters of depositing SiN$_x$ has been evaluated. The deposition methods are LPCVD, PECVD, and RS. None of these processes are fully optimized. Hence, the results experienced for PECVD and ICP-PECVD deposition should not be generalized to be representative of these deposition methods. It is likely that using more optimal deposition parameters in combination with post deposition annealing will provide better results.

2. Development of well controlled recess etching techniques for ohmic and gate contacts
The use of C(V) measurements on MSHM for developing shallow barrier etch recipes has been presented. The method can be used to develop etch recipes for gate and ohmic contact recessing.

3. The development of a versatile MISHEMT fabrication process

By combining the extensive passivation analysis and the shallow etch recipes a versatile MISHFET fabrication process is developed. In this way both depletion and enhancement mode MISHFETs can be defined on the same epi-wafer. Gates insulated by a 5nm thick LPCVD SiNx has a gate leakage 10-100 times lower than the equivalent Schottky gate contact. Low dispersion characteristics of MISHFETs are demonstrated.

All methods and processes have been developed with the aim to be usable in a full HFET and MMIC process. No limitations in lateral and vertical scaling has been detected, so it is believed that the developed processes may be used in devices and circuits for millimeter applications.

7.1 Future work

The LPCVD SiN$_x$ passivation can most certainly be further optimized. Considering the very large effect of deposition parameters on extracted interface state densities it can be assumed that the optimum passivation remains to be developed.

It would be interesting to develop the MISH capacitor analysis further. In this process much can be learnt by studying the pioneering work on the SiO$_2$/Si interface [113]. It would be interesting to apply the methods summarized by Nicollian and Brews to the passivated AlGaN/GaN MISH capacitor, e.g. conductance analysis and density of interface states extractions. The first threshold to overcome is how to manage the more complicated physics involved when the bulk semiconductor is replaced with a heterostructure. A possible way to increase the understanding is to implement the structure in a physical simulator. Also the basic C(V) analysis can be made more powerful by measurements at elevated temperatures and by utilizing partial spectrum illumination.

The utilization of LPCVD SiN$_x$ gate dielectric for insulated gate HFETs is only in the initial phase. The first demonstrator batch needs to be fully characterized in order to verify high frequency and high power performance. Considering the large influence experienced during surface passivation development, it can only be assumed that large work still remains of characterizing a suitable combination of surface passivation and gate insulation. The motivation for utilizing the LPCVD silicon nitride for gate dielectric is the same as for the surface passivation: the passivation is deposited at an elevated temperature and should hence be more stable when thermally cycled. However, the MISHFET process as described can with small modifications be used with any kind of gate dielectric.

There are still some unresolved issues regarding the hexagonal type surface roughness regarding its effect on passive components in MMIC circuits.
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Bibliography


A room temperature HEMT process for AlGaN/GaN heterostructure characterization

M. Fagerlind, H. Zirath, and N. Rorsman

Paper B

Optimization of recessed ohmic contacts for AlGaN/AlN/GaN heterostructures using C(V) characterization of MSHM structures

M. Fagerlind and N. Rorsman

Paper C

Influence of large aspect ratio surface roughness on electrical characteristics of AlGaN/AlN/GaN HFETs

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M. Fagerlind, and N. Rorsman

Paper F

Analysis of the effect of plasma power during ICP-PECVD SiN$_x$ passivation of AlGaN/GaN heterostructures by utilizing a two-layer conduction model

M. Fagerlind, H. Zirath, and N. Rorsman