Integration of vertically-aligned carbon nanotubes into microsystems

A packaging perspective

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ABSTRACT
Carbon nanotubes (CNTs) have been proposed as a candidate material to meet the challenges of miniaturization, reliability, and heat dissipation of microsystems due to their attractive electrical, thermal, and mechanical properties. In the field of microsystem packaging technology, vertically-aligned CNT (VA-CNT) structures grown by chemical vapor deposition (CVD) have been proposed to be utilized as interconnects, thermal interface materials, and cooling fins. This thesis reports on a number of progress steps taken to overcome some of the limitations of as-grown VA-CNTs hindering the full exploitation of their promising potential.

The main field of application of CNTs studied in this thesis is their use in through-silicon vias (TSVs) as a material for replacing copper in 3D stacking of integrated circuits. An improved process for growth of vertically aligned CNTs in deep silicon vias using low pressure chemical vapor deposition (LPCVD) techniques has been developed. After detailed studies of the growth behavior of CNTs in deep silicon vias and the development of a new planarization technique, a method for producing TSVs filled with VA-CNTs was realized. However, there is one drawback of this method and that is this growth process is still not CMOS-compatible due to high growth temperature. Furthermore, the electrical properties of the CNTs are still order of magnitudes away from their theoretical values.

Two key post-growth processes have been developed for solving these problems and they are reported in this thesis. In the first of these processes, VA-CNTs were grown on a separate substrate and transferred to the target substrate at low CMOS-compatible temperatures by use of either conductive adhesives or metals. Using this method, CNTs can be integrated with temperature-sensitive devices and materials. Secondly, methods for densifying porous as-grown VA-CNT forests have been developed. By use of these methods, the packing density of CNT forests can be significantly increased and their conductivity per unit area increased correspondingly. This method made it possible to grow and densify CNT forests on one silicon substrate and then to transfer them to the target substrate. Combining low temperature transfer, densification, and planarization processes, a complete route to fabricate CNT TSVs was finally executed. These vias show improved electrical resistances and are compatible with existing technologies. An easy-to-implement scheme to interconnect the CNT TSVs is also presented in the thesis.

Keywords: carbon nanotube (CNT), packaging, three-dimensional integration, interconnect, through-silicon via (TSV), planarization, densification, transfer
To Chen
List of appended papers

The thesis is based on the following papers:

**Paper A**

*Low temperature transfer and formation of carbon nanotube arrays by imprinted conductive adhesive*

Teng Wang, Björn Carlberg, Martin Jönsson, Goo-Hwan Jeong, Eleanor E. B. Campbell, and Johan Liu


**Paper B**

*Ultrafast transfer of metal-enhanced carbon nanotubes at low temperature for large-scale electronics assembly*

Yifeng Fu, Yiheng Qin, Teng Wang, Si Chen, and Johan Liu

Advanced materials 22, 5039 (2010)

**Paper C**

*Dry densification of carbon nanotube bundles*

Teng Wang, Kjell Jeppson, and Johan Liu

Carbon 48, 3795 (2010)

**Paper D**

*Formation of three-dimensional carbon nanotube structures by controllable vapor densification*

Teng Wang, Di Jiang, Si Chen, Kjell Jeppson, Lilei Ye, and Johan Liu

Submitted to Materials Letters
Paper E
Through silicon vias filled with planarized carbon nanotube bundles
Teng Wang, Kjell Jeppson, Niklas Olofsson, Eleanor E. B. Campbell, and Johan Liu
Nanotechnology 20, 485203 (2009)

Paper F
Through-silicon via interconnects filled with densified and transferred carbon nanotube forests
Teng Wang, Si Chen, Di Jiang, Kjell Jeppson, Lilei Ye, and Johan Liu
Submitted to IEEE Electron Device Letters

Paper G
Carbon-nanotube through-silicon via interconnects for three-dimensional integration
Teng Wang, Kjell Jeppson, Lilei Ye, and Johan Liu
Small 7, 2313 (2011)

Paper H
Application of through silicon via technology for in situ temperature monitoring on thermal interfaces
Yifeng Fu, Teng Wang, Ove Jonsson, and Johan Liu
Journal of Micromechanics and Microengineering 20, 025027 (2010)
Other journal papers not included in the thesis due to being out of the scope of this thesis:

**Computational fluid dynamics for effects of coolants on on-chip cooling capability with carbon nanotube micro-fin architectures**  
Yi Fan, Xiaolong Zhong, Johan Liu, Teng Wang, Yan Zhang and Zhaonian Cheng  
Microsystems Technologies 19, 375 (2009)

**Polymer-metal nano-composite films for thermal management**  
Björn Carlberg, Teng Wang, Johan Liu, and Dongkai Shangguan  
Microelectronics International 26, 28 (2009)

**Photolithographic patterning of electrospun films for defined nanofibrillar micro-architectures**  
Björn Carlberg, Teng Wang, and Johan Liu  
Langmuir 26, 2235 (2010)

**Low partial pressure chemical vapor deposition of graphene on copper**  
Jie Sun, Niclas Lindvall, Matthew T. Cole, Koh T. T. Angel, Teng Wang, Kenneth B. K. Teo, Daniel H. C. Chua, Johan Liu, August Yurgens  
IEEE Transactions on Nanotechnology, in press (2011)
## Abbreviations

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
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<tbody>
<tr>
<td>3D</td>
<td>Three-dimensional</td>
</tr>
<tr>
<td>ACA</td>
<td>Anisotropic conductive adhesive</td>
</tr>
<tr>
<td>ACF</td>
<td>Anisotropic conductive film</td>
</tr>
<tr>
<td>AP-TCVD</td>
<td>Atmospheric pressure thermal chemical vapor deposition</td>
</tr>
<tr>
<td>CMOS</td>
<td>Complementary metal-oxide-semiconductor</td>
</tr>
<tr>
<td>CMP</td>
<td>Chemical mechanical polishing</td>
</tr>
<tr>
<td>CNT</td>
<td>Carbon nanotube</td>
</tr>
<tr>
<td>CTE</td>
<td>Coefficient of thermal expansion</td>
</tr>
<tr>
<td>CVD</td>
<td>Chemical vapor deposition</td>
</tr>
<tr>
<td>C-CVD</td>
<td>Catalytic chemical vapor deposition</td>
</tr>
<tr>
<td>DRIE</td>
<td>Deep reactive ion etching</td>
</tr>
<tr>
<td>FEM</td>
<td>Finite element method</td>
</tr>
<tr>
<td>IC</td>
<td>Integrated circuit</td>
</tr>
<tr>
<td>ICA</td>
<td>Isotropic conductive adhesive</td>
</tr>
<tr>
<td>IHS</td>
<td>Integrated heat spreader</td>
</tr>
<tr>
<td>I-V</td>
<td>Current-voltage</td>
</tr>
<tr>
<td>LP-TCVD</td>
<td>Low pressure thermal chemical vapor deposition</td>
</tr>
<tr>
<td>MEMS</td>
<td>Microelectromechanical system</td>
</tr>
<tr>
<td>MWNT</td>
<td>Multi-walled carbon nanotube</td>
</tr>
<tr>
<td>PCB</td>
<td>Printed circuit board</td>
</tr>
<tr>
<td>PECVD</td>
<td>Plasma-enhanced chemical vapor deposition</td>
</tr>
<tr>
<td>SEM</td>
<td>Scanning electron microscope</td>
</tr>
<tr>
<td>SOP</td>
<td>System-on-package</td>
</tr>
<tr>
<td>SWNT</td>
<td>Single-walled carbon nanotube</td>
</tr>
<tr>
<td>TCVD</td>
<td>Thermal chemical vapor deposition</td>
</tr>
<tr>
<td>TEM</td>
<td>Transmission electron microscope</td>
</tr>
<tr>
<td>TIM</td>
<td>Thermal interface material</td>
</tr>
<tr>
<td>TLM</td>
<td>Transfer length method</td>
</tr>
<tr>
<td>TSV</td>
<td>Through-silicon via</td>
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Chapter 1

Introduction

The word *integration* is explained as “the combining of two or more things so that they work together effectively” in Longman Dictionary of Contemporary English. In this thesis, I deal with combining of carbon nanotubes and microsystem packaging technologies so that they can work together effectively. This introductory chapter provides some information on the general background and the scope of this work.

1.1 Background

This thesis presents research work in the field of packaging technology of microsystems. A microsystem integrates microelectronics, microelectromechanical systems (MEMS), photonics, and radio frequency technologies to perform certain functions. The packaging of microsystems plays a critical role in interconnecting, powering, cooling and protecting various components. The performance, size, reliability, and cost of microsystems are to a large extent dependent on how they are packaged [1]. The importance of packaging has also been increasing in recent years. Further miniaturization of electronics to keep the “Moore’s Law” is expected to be driven mainly by integration technology rather than by further shrinking of transistor sizes in integrated circuits (ICs), which is becoming more difficult and costly due to physical limits [2].

One of the most important and recent trends in packaging technology is the integration in a three dimensional (3D) manner [3, 4], i.e. ICs are stacked vertically within a package. The utilization of the vertical dimension can dramatically increase the density of integration because multiple ICs can be packaged on the footprint of only one IC. It also shortens the interconnection lengths at the system level, leading to a reduction of interconnection delays and power consumption. One example of products deploying 3D packaging is Samsung’s 8 Gb memories
containing stacked circuits interconnected by through-silicon vias (TSVs) (figure 1.1). Very recently, Samsung also announced a 32 GB memory and claimed that the 3D integration and TSV technologies lowered the power consumption and achieved higher density and operational speed [5]. Furthermore, 3D packaging allows true heterogeneous integration of various components onto a system-on-package (SOP) platform to achieve a complete functional unit in a tiny space.

On the other hand, miniaturization, especially in the approach of 3D stacking, causes serious problems in manufacturing processes [6], in long-term reliability [7–9], and in thermal management [10, 11]. This explains why current application of 3D packaging is limited to low power circuits such as memories and why it is difficult to package more power-intense circuits such as CPUs in a 3D way. To meet the challenges of miniaturization while maintaining reliability and efficient thermal management, many efforts have been, and are being made, to develop innovative packaging solutions. One active research field in this area is the utilization of novel materials, nano-materials as one prominent example, for packaging purposes [12].

1.2 Scope

Among the novel packaging materials, carbon nanotubes (CNTs), discovered by Iijima in 1991 [13]∗, are proposed for and used in a number of packaging application due to their unique properties [15]. These applications include for instance flip chip bumps [16], through-silicon via (TSV) interconnects [17], thermal inter-
face materials (TIMs) [18], and cooling fins [19], etc. In the recent International Technology Roadmap for Semiconductors (ITRS, 2009 Edition) [20], CNTs were listed as one of the potential Cu replacements in interconnects and also a candidate for making next-generation TIMs.

In this thesis, only CNTs in their vertically-aligned form are studied. The focus of the present research is on experimental development of a few key steps for an efficient integration of VA-CNT structures into microsystems, from a perspective of packaging. This means that the technological development in this thesis has a strong bias towards the target applications in the field of microsystem packaging. The packaging applications also set boundary conditions for the process development. One such requirement is that the dimensions of the VA-CNT structures are mostly in the range from a few to hundreds of micrometers. Another limitation is that the processing temperature should not exceed the tolerance of complementary metal-oxide-semiconductor (CMOS) technology and common packaging materials such as FR-4 printed circuit boards (PCBs) because packaging is normally the final stage of semiconductor device manufacturing.

The research work performed in the framework of this thesis can be separated into two main parts. The first part is the development of basic processes, including growth of CNTs in deep vias, post-growth low temperature transfer of CNTs, and densification of VA-CNT forests. The growth of CNTs in vias is developed as a step in the fabrication of CNT-filled TSVs. The post-growth low temperature transfer processes are used for integration of CNTs into temperature-sensitive devices and materials while direct growth of CNTs needs to be done at high temperature. The motivation for developing the densification methods is to increase the volume fraction of CNTs in their forests, which are porous and inefficient in thermal and electrical transport.

In the second part of this thesis, the basic processes developed in the first part are combined into process flows for a packaging application - TSV. TSV is a critical component in 3D integration and thus attracts much attention in both academia and industry. In this part of the thesis, the possibilities of using CNTs as the filler in TSVs are examined and demonstrated.

1.3 Outline

This thesis is organized into seven chapters. Chapter 1 contains a brief introduction providing the background and the scope of this research work. In Chapter 2, structures and properties of CNTs and some of their applications, especially in

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†The other potential Cu replacements listed in ITRS are metal silicides, silver, metallic phonon engineering, metallic geometric resonance, graphene nanoribbons, optical interconnects, superconductors, and wireless interconnects.
the field of packaging, are introduced. The following three chapters discuss three basic processes. Chapter 3 is on the synthesis of CNTs, with a special focus on the thermal chemical vapor deposition (TCVD) method used in the majority of this thesis. Chapter 4 and 5 describe the low temperature post-growth transfer processes and the densification methods, respectively. In Chapter 6, it is shown how these basic processes can be combined for the development of CNT-filled TSVs. The thesis is summarized in Chapter 7, which also gives an outlook of this work.
Chapter 2

Carbon nanotubes

This chapter presents a brief introduction to structures and properties of carbon nanotubes. Their electrical, thermal, and mechanical properties are reviewed. After that, examples of applications, especially those for microsystem packaging, are given.

2.1 Structure of CNTs

Tubular structure
Carbon nanotubes can be described as hollow tubes of rolled one-atom-thick graphite layers (known as graphenes). Diameters of CNTs range from 0.4 nm [21,22] to tens of nm. Lengths of CNTs can be up to a few millimeters [23], making it a material with very high aspect ratio. The structure of a CNT is represented by a pair of indices \((n,m)\), where \(n\) and \(m\) are integers denoting the numbers of basis vectors \(a_1\) and \(a_2\) of graphene and atom \((n,m)\) is equivalent to the atom\((0,0)\) in the tube (figure 2.1). The diameter of a CNT can thus be calculated by

\[
d_t = \frac{\sqrt{3}a_{c-c}}{\pi} \sqrt{m^2+mn+n^2}
\]  

where \(a_{c-c}\) is the carbon bond length in graphene (1.42 Å) [24].

CNTs are terminated by carbon caps of different shapes [25], by open ends [25,26], or by metal particles used as the catalyst for CNT growth [27].

Chirality
A graphene layer can be wrapped into a tube along different directions. This is represented by the chiral vector \(C_h = na_1 + ma_2\). The chiral angle is defined as
\[ \theta = \tan^{-1}\left[\sqrt{3}n/(2m+n)\right] \]

CNTs can then be classified into three types: armchair when \( n = m \), zig-zag when \( m = 0 \), and chiral for other cases (see figure 2.1). The chirality is an important feature for a CNT because it determines its electronic property.

### Single-walled and multi-walled CNTs

The CNTs described above and illustrated in figure 2.1 contain only one rolled graphite layer. They are therefore called single-walled carbon nanotubes (SWNTs). A carbon nanotube may also consist of multiple coaxial shells, so called a multi-walled carbon nanotube (MWNT). The first CNTs reported by Iijima are actually MWNTs [13]. The number of walls in a MWNT can range from two (called double-walled CNT or DWNT in this case) up to a few tens. The inter shell distance in a MWNT is close to 0.34 nm, the inter layer distance of graphite. The inter wall attraction force in MWNTs is van der Waals force, the same as the inter layer bounding force in graphite. Different walls in a MWNT can have different chiralities [24].
2.2 Properties of CNTs

Electrical properties

The electrical properties of a CNT are determined by its chirality. A tube with the indices \((n,m)\) satisfying \(n - m = 3i\), where \(i\) is an integer, is metallic at room temperature. CNTs with all other chiralities are semiconductive with a band gap approximately inversely proportional to the tube diameter [29, 30]. The band gap can be approximately estimated as

\[
E_g \approx 2\gamma \frac{a_c - c}{d_t}
\]

(2.2)

where \(E_g\) is the band gap and \(\gamma\) is C-C tight-binding overlap energy. From experimentally measured band gap values, \(\gamma\) for CNTs is numerically fitted to be around 2.5 eV [31,32], a value close to that determined by calculation for a single graphene sheet [29].

Armchair CNTs \((n = m)\) are always metallic with a finite density of states at the Fermi level. Other metallic CNTs \((n - m = 3i\) where \(i \neq 0\)) have a small band gap induced by the curvature of the tube for those with small diameters [33, 34]. Statistically, one third of the CNTs are metallic and two thirds of them are semiconductive. The same proportion also applies to the walls of MWNTs. Practically, all CNTs with large diameter, true for most MWNTs, can be considered conductive based on the inverse proportion expressed in equation 2.2.

A conductive SWNT shorter than its electron mean free path behaves as a quantum conductor with twice of a quantum conductance, \(G_0 = 2e^2/h\) where \(e\) is the elementary charge and \(h\) is Planck’s constant [35]. Therefore the resistance of a SWNT cannot be lower than \(h/4e^2 = 6.45 k\Omega\). The electron mean free path of a CNT at room temperature can be up to a few tens of \(\mu\)m [36, 37].

For MWNTs, only the outermost shells were believed to participate in the conduction [35] but MWNTs have been experimentally shown to have multi-wall conduction [38]. Techniques such as etching [26, 39] and polishing [40] have also been shown to be capable of opening the ends of MWNTs and make the inner shells contribute to the conduction. It should be noted that the electrical conduction of CNTs with defects is much lower than that of CNTs with perfect structures [41].

CNTs also have some other unique electrical properties. CNTs can have a high current carrying capacity up to \(10^9\) A cm\(^{-2}\) [35,42], a few orders of magnitude higher than that of copper. CNTs do not fail due to electromigration [43]. The Joule heating in CNTs is two orders of magnitude less than the prediction by Joule’s law [44].
Chapter 2

Thermal properties

Thermal conductivity of CNTs is found to be higher than 3000 W m\(^{-1}\) K\(^{-1}\) at room temperature based on experimental measurements on individual nanotubes \[45, 46\]. These reported values are higher than those of copper (\(~400\) W m\(^{-1}\) K\(^{-1}\)) and diamond (\(~2000\) W m\(^{-1}\) K\(^{-1}\)). These results agree well with theoretical calculations and modeling work \[47–49\]. It has also been shown theoretically that the heat transport in CNTs at room temperature is due mainly to phonon transport \[50\]. Similar to the electron transport, it is also worthwhile to point out that defects and vacancies in CNTs significantly decrease their thermal conductivity \[48\].

CNTs have also shown very good thermal stability in both vacuum \[51\] and air \[52\].

Mechanical properties

The CNTs are very strong materials due to the covalent \(\sigma\) bonds between the carbon atoms. Exceptionally high Young’s modulus values of CNTs have been shown from experimental studies. For both SWNTs and MWNTs, the Young’s modulus is in the TPa range \[53–55\]. It can be up to 3.6 TPa for SWNTs and 2.4 TPa for MWNTs \[53\]. Theoretical work has predicted values in a similar range \[56–58\]. The tensile strength of CNTs is in the range of a few tens of GPa \[54, 55, 59\]. CNTs are also quite flexible and resilient \[60\], and they have low thermal expansion \[61\]. One important aspect of the mechanical properties of CNTs is their anisotropic nature. Young’s modulus in the transverse direction is much lower than that in the axial direction for CNTs with large diameters \[62\].

2.3 Applications of CNTs in packaging

Thanks to their unique structure and exceptional properties, CNTs have been proposed for all kinds of applications during the last two decades. Since 2005 more than 5000 papers about CNTs have been published every year.* It is nearly impossible to make a complete list of all the applications. Very limited number of examples are given here to show how wide in scale those applications span. On the nanometer scale, CNTs were used to make single-electron transistors \[63\], nanoelectromechanical systems \[64\], and nanoscale memory cells \[65\], etc. On the micrometer scale, CNTs were used as field emission sources \[66\], biosensors \[67\], and scaffolds for cell culture \[68\], etc. On the millimeter to centimeter scale, they were applied for dry adhesive films \[69\], artificial muscles \[70\], and brush contacts for motors \[71\], etc. On the meter scale, they found usage in bike frames \[72\]

*Based on searching “carbon nanotube” in Scopus.
and tennis rackets [73] etc. Even up to the thousands of kilometers scale, CNTs were proposed to be used as cables for space elevators [74].

CNTs have also been applied in a number of different packaging technologies. They are majorly used in two different ways: (1) used solely in the aligned forest form as electrical or thermal transport paths; (2) used as fillers in composite materials to improve their properties. Packaging applications of CNTs in both forms are shortly introduced below. To help readers with no packaging background to pinpoint the basic parts in an electronic package, an illustration of a typical packaged component is shown in figure 2.2. Actually, CNTs will most probably find their application in most of these basic parts within a packaged component.

**Interconnects**

Interconnection is one of the main functions of packaging. Interconnects are made on different levels of packaging† to connect various components and modules together to form functional microsystems. During assembly of ICs, interconnects are made between the ICs and chip carriers. In 3D integration, interconnects are also made vertically through silicon. These interconnects are commonly termed off-chip interconnects. Compared to their on-chip counterparts, they are normally much larger and carry more current. Due to the mismatch in coefficient of thermal expansion (CTE) between dissimilar materials, such as between a silicon die and a chip carrier made of polymeric materials, these interconnects are often exposed

---

† Chip-to-package packaging, or IC assembly, is normally referred to as level 1. Package-to-board integration, or board assembly, is termed as level 2. Connecting boards onto backplanes (motherboards) is on level 3. And housing the entire system is generally called level 4 packaging. The discussion here is limited to first level off-chip interconnects.
to mechanical strain and stress. Cyclic temperature changes present in electronics also lead to cyclic mechanical loadings on these interconnects. This fatigue phenomenon due to cyclic loadings is believed to be relevant for some 90% of all structural and electrical failures in electronics [1].

Materials for building off-chip interconnects vary in different technologies. In wire bonding technology, gold wires are drawn between ICs and chip carriers. In more demanding applications, the peripheral wire bonding was replaced by flip chip technology, in which the chip is flipped upside down and interconnection is accomplished directly between the pads on the active sides of the ICs and the carriers by for instance solder balls, gold bumps, or conductive adhesives. A new category of off-chip interconnects is the through-silicon vias used in 3D integration. CNTs have been used as flip chip bumps [16] and TSVs [17], thanks to their prominent properties. In Chapter 6, application of CNTs in interconnects, especially in TSVs, will be the central topic and discussed in more detail.

**Thermal interface materials**

The function of thermal interface materials (TIMs) is to fill the micro-scale gaps between two contacting surfaces for an efficient thermal transport through this interface [76]. In a package, TIMs are typically applied between the die and the lid, also called integrated heater spreader (IHS), and also between the IHS and the cooling device. They are called TIM 1 and TIM 2 respectively, reflecting the different levels of packaging on which they are used. Beside the obvious significance in thermal transport, TIMs also plays a critical role in maintaining the reliability of the package by absorbing the thermomechanical strain. Therefore, both thermal and mechanical properties are important in selecting and developing TIMs.

The most widely used TIMs are polymeric composites filled with thermally conductive metallic or ceramic particles. Pure indium, a highly conductive and ductile metal, is also commonly used as TIM 1 in high-performance applications.

Developing TIMs with better thermal and mechanical properties is one of the key measures to meet the increasingly difficult thermal management challenge. The high thermal conductivity of CNTs makes them a natural selection for developing or improving TIMs. The application of CNTs in TIMs falls into two major categories. One of them is to add CNTs into polymer matrix as randomly oriented fillers [77–79]. It was shown that a small filling ratio of CNTs (1 wt%) can significantly enhance the thermal conductivity of the composite (by 125% at room temperature) [77]. Treatments such as magnetic field processing to introduce alignment of CNTs in the matrix can further improve the thermal transport [80]. Introducing small amount of CNTs as an extra filler into existing TIMs can also greatly promote their thermal conductivity by enhancing the heat transfer...
between the original fillers [81].

Another approach is to use vertically-aligned CNT films directly, sometimes also infiltrated with a polymer, as TIMs, such as in ref. [18, 82, 83]. The results in these references differ for a factor of 1 to 2 orders of magnitude, which may be due to the variations in the quality of CNT films and measurement methods. In general, the measured thermal properties of most VA-CNT-based TIMs are still poorer than those of typical metal systems even though the thermal conductivity of bulk VA-CNT films can be quite high [84, 85]. It was found that the thermal contact resistances between the CNTs and the substrates dominate in the interfaces [86–88], thus their minimization is the key to develop efficient VA-CNT-based TIMs. By reducing these contact resistances by annealing or bonding, CNT TIMs with quite low thermal resistances (< 10 mm² K W⁻¹) can be obtained, suitable for applications such as cooling of light-emitting-diodes [89, 90].

Cooling fins

In the thermal management of microsystems, heat sinks or coolers consisting of arrays of cooling fins are often used to facilitate an efficient heat transfer from components to the ambient air by offering a large area of heat exchange surface. For applications where natural convection is not sufficient, fans are often attached onto the heat sinks to create more efficient forced convective cooling. Heat sinks used in both natural and forced convective cooling are mostly made of mechanically machined copper or aluminum.

Cooling fins are also necessary in liquid cooling where a liquid other than air is used as the coolant for more power-intensive components. In the case of forced convection, the heat transfer coefficient of using water as the coolant can be a few orders of magnitude higher than that of using air [91]. A development in this technology is the utilization of microchannels [92], the dimensions of which are in the micrometer range so that a very large heat exchange area is created. The microchannel coolers can offer very efficient cooling and be made very compact with a possibility of being directly integrated onto the ICs. In the first demonstration of microchannel coolers, consisting of 50 µm wide etched-out channels and 50 µm wide silicon cooling fins, a power density of 790 W cm⁻² could be dissipated with a temperature difference of 71 °C [93].

CNTs, in their forest form, have been used as cooling fins in both air [19] and liquid cooling [94, 95]. The major advantage of using CNT forests as cooling fins is the large heat exchange area of these porous structures. Other benefits include high fin efficiency, light weight, mechanical stiffness, and convenience of integration.
Chapter 2

Fillers in packaging materials

Another major usage of CNTs in packaging technology is their use as fillers in a variety of packaging materials for improving or tailoring the properties. Both MWNTs and SWNTs have been added into lead-free solders as reinforcements and produced improvements in wetting properties, melting characteristics, and mechanical strengths [96, 97]. Other important interconnection materials, conductive adhesives, have also been filled with CNTs in order to enhance their electrical and mechanical properties, and also their reliability [98–100]. Besides, underfills containing CNTs have also been developed and used in harsh superconductor electronics [101, 102].

Passives

Passives are components not capable of performing any amplifying or switching functions in circuits. The major types of passives are resistors, capacitors, and inductors, which are indispensable parts of microsystems. In modern electronic products, the number of passives is usually ten times more than that of active components [1]. Depending on the forms of packaging and integration, passives can be discrete, integrated, or embedded. Embedded passives, directly integrated in substrates, have gained much research interest due to their potential of enhancing integration density and reducing parasitics by eliminating leads [1].

CNTs provides an attractive choice to build miniaturized passives, thanks to their unique properties, their availability in various physical forms, and the variety of processing techniques at a small scale. CNT-based resistors [103, 104], capacitors [105, 106], and inductors [108] have all been experimentally demonstrated. Modeling and design issues of CNT-based passives have also been addressed [109–111].

\[\text{CNTs have also been proposed and used as an electrode material in electrochemical capacitors, also called supercapacitors. It is a popular research topic and numerous papers on this topic were published. Ref. [107] is a good review article of this general field. However, the target application of these supercapacitors is not the miniaturized passives used in densely packaged microsystems, thus being out of the scope of the discussion here.}\]
Chapter 3

Growth of carbon nanotubes

This chapter introduces the deposition, or growth as a more commonly used term, of carbon nanotubes. The focus is on the thermal chemical vapor deposition method for growing vertically-aligned CNTs, both on flat substrates and in vias. The growth processes described here serve as a basis for the post-growth processes presented in the succeeding chapters.

3.1 Overview of CNT growth by CVD

CNTs can be synthesized by different methods, including arc discharge [13], laser ablation [112], and chemical vapor deposition (CVD) [113]. Among these methods, CVD attracts extensive interest mainly due to the greater controllability it offers over the other methods.

The CVD of CNTs is a catalytic process, thus often termed C-CVD (catalytic CVD). The catalyst is normally a metal, mostly a transition metal such as iron (Fe), nickel (Ni), cobalt (Co), or any of their alloys. There are two major ways to provide the catalyst for the CVD process. One method is to deliver the catalyst particles through the gas flow, namely floating catalyst [116] or fluidized bed catalyst method [117]. Another approach is called supported catalyst method. The catalyst layer is deposited onto the substrate, silicon (Si) as the most common one, by physical vapor deposition processes prior to the CNT synthesis. A great advantage of this method is that by standard lithography processes the patterns of the catalyst film can be easily defined, naturally leading to any desired patterns of the synthesized CNT films. This patterned growth is necessary for many applications. The deposited catalyst layer is often annealed first to form discrete nano-sized particles, which later catalyze the CNT synthesis. In order to

*There are exceptions indeed. In 2009 two papers reported the metal-catalyst-free synthesis of CNTs [114,115], in which nano SiO$_2$ particles were proven to be capable of catalyzing the growth.
prevent the catalyst from diffusing into the substrate, a thin barrier layer, such as aluminum oxide (Al$_2$O$_3$) or titanium nitride (TiN), is often deposited prior to the deposition of the catalyst layer [118].

During the CVD of CNTs, carbon is usually provided through the flow of a hydrocarbon gas, such as acetylene (C$_2$H$_2$) or methane (CH$_4$). This deposition gas often needs to be diluted in a reducing gas, such as hydrogen (H$_2$) or ammonia (NH$_3$), serving the purpose of removing the amorphous carbon during the deposition [119]. The mechanism of catalytic CNT synthesis is a central topic of CNT research and is still not fully understood. It has been widely accepted that it involves decomposition of hydrocarbon molecules on the surface of the metal particles, dissolution and diffusion of the carbon atoms in the particles, and precipitation of the carbon atoms on the surface to form nanotubes [120]. Thus the diameters of the nanotubes are largely determined by the sizes of the metal particles, which can be varied by controlling the thickness of the deposited catalyst film [121]. From a macroscopic perspective, the CNTs “grow” from the seeding catalyst layer. CNT growth can be either a base growth, in which the metal particles stay on the substrate, or a tip growth where the particles are lifted and stay at the tips of the CNTs.

Depending on the form in which the energy is supplied to the reaction, CVD of CNT falls into two main categories, i.e. thermal CVD (TCVD) and plasma-enhanced CVD (PECVD). There exist a variety of reactor designs for both types. For example, a PECVD system for CNT growth may be equipped with a direct-current (dc), a hot-filament direct-current (HF-dc), or a microwave plasma source, etc [120]. In this thesis, based on the requirements of packaging applications, TCVD was chosen as the growth technique, mainly due to its capability of growing long CNTs of high growth rates.

### 3.2 Growth of VA-CNTs

In many applications it is necessary to grow the CNTs vertically aligned on the substrates. This alignment in the vertical direction can be achieved through two mechanisms. In PECVD, the alignment is induced by the electrical field [122]. An important benefit of using PECVD for CNT growth is the possibility of growing a single VA-CNT from a catalyst particle patterned sufficiently small (< 100 nm) [119].

The alignment in TCVD is achieved by crowding effect from neighboring CNTs. In this case, the catalyst film is normally bigger in the lateral direction (> 1 µm) and annealed to form a large amount of particles. A typical TCVD process of VA-CNTs with the necessary annealing and growth steps is illustrated in figure 3.1. This collective assembly of CNTs grown from a large catalyst pattern
Growth of carbon nanotubes

Figure 3.1: Illustration of a typical TCVD process of VA-CNTs

An atomic force microscopy (AFM) image of catalyst particles formed by the annealing of 1 nm thick Fe layer at 500 °C is shown in figure 3.2. The site density of the particles is in the order of $\sim 10^{10}$ cm$^{-2}$. This means that in a VA-CNT forest grown from a square catalyst pattern with 100 µm long sides, the number of CNTs is roughly in the order of 1 million.

Two TCVD setups have been used in the present work to grow VA-CNTs, including a home-made setup and a commercial system. The growth processes using both systems are introduced in this section.

†The word *forest* is normally used for structures with sparse VA-CNTs. Another term *bundle* is more commonly used referring to groups of closely packed CNTs, though it is used for structures which are actually forests in many papers.
Atmospheric pressure TCVD

The first TCVD setup used in this thesis is a home-made hot-wall system built by and located at Atomic Physics Group, Department of Physics, Göteborg University. An illustration of this setup is shown in figure 3.3. The reactor of the system is a quartz tube roughly 1 m long and 4 cm in diameter, inserted into a furnace. The quartz tube is connected to inlet and outlet ports. Reactant gases are input into the quartz tube and controlled by mass flow controllers (MFCs). There is no pressure control unit with this reactor, therefore the deposition is run at atmospheric pressure and called atmospheric pressure TCVD (AP-TCVD).

Before the growth some preparation steps need to be done. 10 nm thick Al₂O₃ and 1 nm thick Fe, as a typical catalyst layer, were sequentially evaporated onto a Si wafer by an electron beam evaporator. Si wafers with either native oxide or 400 nm thermally grown oxide layer can be used. The patterning of the catalyst layer was realized by standard photolithography and lift-off processes. The wafer was then diced to small chips, which were later taken into the growth process.

The procedure of a typical growth sequence in this TCVD system is as follows. The chip with the catalyst was inserted into the center of the quartz tube, later sealed and evacuated to a pressure lower than 1 mbar. The quartz tube was filled with Ar until a positive pressure difference over the atmospheric pressure is built. The outlet port was opened at this point. Then 900 standard cubic centimeter (sccm) Ar and 100 sccm H₂ were flowed through the quartz tube. Keeping this combination of gas flows, the furnace started to heat up until the temperature reached the growth temperature (700 °C as a typical value) and stayed there for 15 minutes. After that a controlled amount of C₂H₂ (3 to 6 sccm as a typical value) was input into the quartz tube to start the CNT growth while the Ar/H₂ flow was changed to 500/500 sccm. The growth lasted for 3 to 20 minutes depending on the desired CNT length. Afterwards, the C₂H₂ flow was terminated and the reactor cooled down to room temperature in a 900/100 sccm Ar/H₂ flow.

Scanning electron microscopy (SEM) images of typical CNT forests grown by
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TCVD using this home-made system are shown in figure 3.4. In general, the CNTs are well aligned in the vertical direction. One problem that can be clearly observed is the non-uniform growth of the CNT forests, especially noticeable along the edges of the array.

A more detailed description of this growth system can be found in ref. [123]. A complete investigation of the CNT growth behavior and its dependence on the catalyst pattern geometry using exactly the same system was reported in ref. [124].

Low pressure TCVD

Another CNT growth setup utilized in this thesis is a commercial system (Black Magic II, abbreviated as BM in the rest of this text) from Aixtron. This system can also be operated for dc-PECVD growth of carbon nanotubes or nanofibers. In this thesis, only the TCVD mode of BM is used. The structure of the reactor in BM is illustrated in figure 3.5.

Compared to the above-mentioned home-made setup, BM differs in two key aspects. First, the TCVD in BM is performed in a bell jar under low pressure (∼10 mbar) other than the atmospheric pressure in the home-made system. This growth process is thus denoted as LP-TCVD in the rest of this thesis. The reactant gases are pre-mixed and delivered into the reactor through a showerhead positioned above the growth sample. Second, BM is a typical cold-wall CVD system, while the home-made setup is a typical hot-wall system. The chip is directly placed on and heated by a 2-inch graphite heater, also acting as the sample holder, the temperature of which is monitored by a thermocouple and fed back to the control system.

A typical LP-TCVD growth procedure using BM is listed as follows. The chips were prepared in the same manner as for the AP-TCVD process and placed on the heater. The reactor was firstly pumped down to about 0.1 mbar before
sccm H₂ was input into the system. The holder was then heated up to 500 °C at a heating rate of 300 °C/min. The annealing of the catalyst was done at 500 °C for 3 minutes. After that an additional 200 sccm C₂H₂ was added to initiate the growth while the holder was quickly heated up to 700 °C. The time of this growth phase varied from 30 to 300 seconds to produce CNTs of different length. The growth rate is generally in the order of 1 µm/s. Finally, the chip was cooled down in a 1000 sccm N₂ flow before being taken out.

Some typical results from the LP-TCVD growth are displayed in figure 3.6 (SEM images) and figure 3.7 (a transmission electron microscopy (TEM) image). Figure 3.6 (a) and (b) are CNT films grown from an non-patterned catalyst layer, revealing the good alignment and straightness of the CNTs. Figure 3.6 (c) and (d) are CNT forests grown from patterned catalyst layer. Compared to figure 3.4, it is clear that the LP-TCVD produces CNT structures with better uniformity. This improvement can be attributed to the decrease of reaction pressure, which leads to an increase in diffusibility of the reactants [125]. This difference is more obvious when the geometries are more complex such as in the case of growth in vias, which will be discussed in the next section.
Figure 3.6: SEM images of typical results from the LP-TCVD growth. (a) and (b) CNTs in a film showing good alignment and straightness. (c) and (d) CNT forests with good uniformity.

Figure 3.7: A TEM image of a CNT grown by the LP-TCVD process.
Chapter 3

3.3 Growth of CNTs in vias

One of the techniques developed within the scope of this thesis is a CNT-filled through-silicon via technology (Chapter 6), in certain cases requiring direct CNT growth in deep vias. Both the home-made system and BM have been used for this purpose. The same catalyst layer as stated above is selectively deposited onto the bottom of the vias.

CNTs can be successfully grown from the bottom of vias deeper than 100 µm using both growth systems. However, the growth behavior in the two systems running at atmospheric and low pressures, respectively, differs significantly in terms of uniformity and controllability. At high pressure, the gas flow patterns have a significant impact on the deposition rates at different positions due to the low diffusibility of the gas molecules. At low pressure, this effect is much less important due to the higher diffusibility of the molecules [125].

Using the home-made system, the growth of CNTs at atmospheric pressure in deep Si vias is found to be different from that on a flat surface, possibly due to the differences of gas diffusion to the catalyst at the bottom of the vias giving different conditions of growth [124]. First, a relatively high flow rate of C$_2$H$_2$ needs to be supplied to achieve long and uniform CNT forests. A narrow process window of 5-6 sccm flow rate of C$_2$H$_2$ is found to generate reasonably good growth results. Furthermore, the growth of CNTs in deep Si vias is highly dependent on the arrangements and geometric dimensions of the vias. For example, two chips picked from the same wafer, carrying vias with the same diameter and depth but in different arrangements (figure 3.8 (a) and (b)), underwent the same growth conditions but produced different results. It can be observed that CNTs grown in vias in the array arrangement (figure 3.8 (a)) are quite uniform while those grown in vias in the peripheral arrangement (figure 3.8 (b)) are not uniform. A similar comparison can be made between two chips from the same wafer but with different geometric dimensions. A chip with 50 µm diameter and 162 µm depth vias and a chip with 20 µm diameter and 131 µm depth vias through the same growth conditions show very different results. CNT forests grown from the former one (figure 3.8 (c)) are very uniform and well aligned and those from the latter one (figure 3.8 (d)) are not uniform. Some CNTs on the chip shown in figure 3.8 (d) are even not tall enough to stick out from the vias.

On the other hand, the LP-TCVD growth using BM shows better uniformity and controllability for vias with different dimensions and different arrangements. CNT forests have been successfully grown in vias with depth from tens to hundreds of micrometers and arranged in different patterns, all of which give good uniformity across the whole chip. As an example, figure 3.8 (e) and (f) show the uniform CNT forests grown on two chips with same vias, 50 µm in diameter and 120 µm in depth, but in different arrangements. The chip shown in figure 3.8 (e)
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Figure 3.8: SEM images of CNT forests grown from the bottom of deep Si vias with different arrangements and geometric dimensions. (a) Vias with 50 µm diameter and 125 µm depth in an array arrangement. (b) Vias with 50 µm diameter and 125 µm depth in a peripheral arrangement. (c) Vias with 50 µm diameter and 162 µm depth. (d) Vias with 20 µm diameter and 131 µm depth. (e) Vias with 50 µm diameter and 120 µm depth in an array arrangement. (f) Vias with 50 µm diameter and 120 µm depth in a peripheral arrangement. (g) and (h) The chip in (e) after Si surrounding the CNTs being etched away. (a) to (d) are results from the growth by AP-TCVD using the home-made setup and (e) to (h) are results from growth by LP-TCVD using the BM system.
was further etched to reveal the structure of the CNT forests hidden inside the vias (figure 3.8 (g) and (h)). It can be observed that the CNT forests are straight and the CNTs are well aligned inside the vias.

3.4 Problems with VA-CNTs grown by CVD

From the description from previous chapters and sections, it can be concluded that VA-CNTs are a versatile material with many unique properties, attractive for various potential applications. However, the as-grown VA-CNT structures synthesized by CVD suffer from a few problems, hindering the exploitation of the material’s full potential and limiting the field of application. These problems are listed and discussed below.

- **Low structural quality of CNTs.** It has been shown that the structural quality of CNTs synthesized by CVD is poorer compared to those by arc discharge or laser ablation [126]. However CVD provides the only way to produce aligned CNTs at defined locations, thus being the only choice in many applications. It can be observed in the field of CNT research that there is a big gap between the results gained from single short CNTs and those from CVD-grown collective structures of long CNTs. One example is that a CNT film has a thermal conductivity one to two orders of magnitude lower than the values measured from single short tubes [127]. A major reason of this gap is the difficulty of growing long CNTs with good structural quality along the entire tube length, especially in the case where the CNTs are vertically aligned. Huang et al. have found that the resistance of a CNT increases dramatically after introducing bends in the nanotube during its growth [128]. Hence it is of critical importance to fabricate CNTs in good structural quality. The scale of packaging applications normally needs CNT structures a few tens to a few hundreds of micrometers long, making this requirement very difficult to meet. Improvements of the structural quality can be made by optimization of the growth process [129] and post-growth annealing at high temperature [130, 131].

- **Low volume fraction of CNTs in the forests.** CNT forests or films are a very porous material, with a typical porosity higher than 90% [132, 133], making it inefficient in electrical and thermal conduction. This low volume fraction is fundamentally limited by the standard catalyst preparation method of annealing a thin film to form discrete particles. Rather than generating more densely packed particles, increasing the thickness of the catalyst film only leads to sparser and bigger particles [121]. Attempts have been made
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to increase CNTs’ volume fraction by engineering the catalyst [134–136], though the outcomes were still much lower than the ideal situation.

- **High growth temperature of CNTs.** One central problem regarding the compatibility of CNTs with existing technologies, especially the CMOS technology, is the high synthesis temperature of CNTs. Many efforts have been made to lower the synthesis temperature of CNTs [137–140]. However the actual heating effect from the plasma in some works is questionable [141] and there is proof that the CNTs grown at lower temperature have poorer structures than those grown at higher temperature [142]. Low temperature growth also suffers from low deposition rate and the difficulty of growing long nanotubes [143]. An alternative strategy is to locally heat the growth sites using microfabricated thin film heaters instead of the whole substrate [144, 145]. This method is however not practical for many applications since it adds much complexity of fabricating micro heaters, not possible to be removed after growth, and electrical connection during the growth.

- **Selective growth of CNTs.** CVD growth of VA-CNTs is strongly influenced by the underlayers [146]. This selectivity is useful for patterning under certain situations but generally a problem for CNTs’ wide application. It is time-consuming and sometimes problematic to adjust growth conditions for a different underlayer.

- **Random distribution of CNT chiralities.** To control the chiralities of CNTs is always a focus of CNT research because of its critical importance in many applications. Using CNTs as transistors requires them to be semiconductive while interconnection application requires metallic tubes. Although it is possible to sort the CNTs with respect to their chiralities by various methods [147], it is preferable to control the chirality during the growth process, which remains as a big challenge. Remarkable progress in this area has been achieved in recent years. Preferential growth of semiconductive SWNTs up to 96% fraction has been demonstrated [148, 149]. Growth of SWNTs from seed nanotubes have been developed, showing that the grown SWNTs maintain the chirality of the seeding ones [150]. Wang et al. have developed a technique to vary the percentage of metallic SWNTs from 42% to 57% by controlling the ratio of carbon to oxygen atoms in the carbon feedstocks during the growth [151]. Harutyunyan et al. reported successful enrichment of metallic SWNTs up to 91% by controlling the catalyst annealing conditions [152]. It is worthwhile to note that for MWNTs, which are usually with large diameters and used in interconnection applications,
this problem is much less prominent because the band gap is very small even the wall is semiconductive.

One of the motivations of this thesis is to solve some of the problems listed above, from the perspective of microsystem packaging technology, the solutions being the topics in the following two chapters. Low temperature transfer processes presented in Chapter 4 aim at solving the high temperature and selective growth problems. Densification methods described in Chapter 5 from an approach to overcome the problem of CNTs’ low volume fraction in the as-grown forests.
Chapter 4

Transfer of carbon nanotubes

This chapter presents one of the basic processes developed in this thesis, namely the low temperature transfer of vertically aligned carbon nanotubes from one substrate to a target substrate. The chapter starts with a general overview of the technology, explaining the motivation of this development and introducing some related work done by other researchers. Two variations of the transfer process, using conductive adhesive and metal respectively as the transfer medium, are then described and discussed.

4.1 Overview of CNT transfer

In integration of VA-CNTs into Microsystems, their compatibility with current materials, devices, and manufacturing processes is a critical concern. As explained in Section 3.4, one major problem with growing VA-CNTs by chemical vapor deposition is the high growth temperature, which exceeds the tolerance of many materials and devices currently used in electronics fabrication, for example the complementary metal-oxide-semiconductor devices. While significant progresses have been made in low temperature CNT growth, there is always a dilemma of trading off CNT quality for lower growth temperature.

To solve this problem, one approach is to grow CNTs at a high temperature and then transfer them to the target substrates at a low temperature using a transfer medium material, e.g. solders or adhesives. This transfer strategy also provides a solution to the problem of CNTs’ selective growth on different underlayer materials. Transferring CNTs after growth brings the freedom to choose any substrate and growth conditions that generate CNTs of high quality. Furthermore, this transfer strategy makes it possible to apply post-growth treatments, such as doping and high temperature annealing, before the CNTs are assembled to devices not allowing such processes.
Table 4.1 summarizes the previous work found in literature on temperature transfer of VA-CNT structures. This summary is limited to those work in which the CNTs are vertically-aligned both before and after the transfer process. There are many papers on transferring randomly- or horizontally-aligned CNTs for applications such as transistors or interconnects, which are out of the scope of the present thesis.

Regarding the transfer of VA-CNTs, this process falls into two major categories. One category, denoted “wet” method herein, involves a lift-off step to separate the CNTs and the growth substrate by etching away the barrier layer, commonly done in hydrofluoride (HF). After that, the stand-alone VA-CNT film are placed onto the target substrate. The first demonstration of VA-CNT transfer by Huang et al. [153] belongs to this category. Because this method requires handling of entire stand-alone films, it is difficult to employ any fine patterning or alignment during the transfer. Moreover, this approach normally does not apply an assembly material between the CNTs and the target, making the adhesion between them quite weak. Therefore the applicability of this wet method is very limited.

A more widely studied and implemented route is to use an assembly material to transfer VA-CNTs, eliminating the wet processing step. These are marked as “dry” methods in table 4.1. A variety of materials has been used for the transfer purpose, including pure polymeric materials, conductive adhesives, and metals, etc. If electrical conduction from the CNTs to the substrate is needed, only conductive assembly materials can be used. A noticeable work was done by Lin et al.,
using a chemical process to transfer functionalized CNTs by a monolayer of thiol molecules on a gold surface [163]. The processing temperature of these dry transfer methods varies from room temperature to higher than 500 °C. The processing time ranges from a few minutes to a few hours.

Patterning in dry transfer of VA-CNTs can be realized in two different ways. One way is to simply grow the CNTs from the patterned catalyst and then transfer them with non-patterned assembly materials. If electrical insulation between CNT forests and conduction from the CNTs to the substrate are required, which is a common case using CNT forests as interconnects or electrodes, patterned assembly materials are needed. In table 4.1, only ref. [158, 160, 162, 169] fulfill this criterion. In this case, the pre-patterning of CNTs is usually not necessary. The patterning is realized through the transfer process because the CNTs attached to the assembly material can be easily separated from the rest of the film owing to the week van der Waals interactions between the aligned nanotubes. Using both patterned assembly material and patterned CNTs in the transfer process can help generating well-defined shapes of the transferred structures and improving the yield but requires fine alignment in the process.

The following two sections describe two low temperature processes for transferring VA-CNTs, using a conductive adhesive and a metal respectively.

4.2 Transfer of CNTs by conductive adhesive

Overall process

A process for transferring and forming CNT forests at a low temperature (150 °C) by patterned isotropic conductive adhesive (ICA) was developed in this thesis project. Figure 4.1 illustrates the overall process, which contains two phases: the patterning of the ICA and the transfer of the CNTs. The patterning of the ICA is realized through an imprint-transfer process. The patterned thin ICA films were then used to transfer and form an array of CNT forests.

Patterning of adhesives

One key step in the whole process is to make patterned thin flat films of conductive adhesives, which is difficult to achieve by conventional methods such as stencil printing or dispensing. A unique imprinting-transfer process has been invented for this purpose.

The mold used to imprint the conductive adhesive was made in Si by anisotropic wet etching in a tetramethylammonium hydroxide (TMAH) solution. The patterns
Figure 4.1: Schematic diagram of the overall process of CNT transfer by ICA. The ICA is patterned by an imprinting-transfer process and then utilized to transfer and form an array of CNT forests from a CNT film.
Transfer of carbon nanotubes

were defined by a standard photolithography process followed by buffered etching of a silicon oxide (SiO$_2$) layer in HF. Pyramid-like cavities were formed by the four {111} planes of Si. The SiO$_2$ mask layer was removed after the cavity etching since the undercut shapes might cause a bad release of the mold after the imprinting.

Before the imprinting step, the mold was spin coated with a thin layer of release agent, which prevented the conductive adhesive from sticking to the mold. The imprinting was carried out with the help of a flip-chip bonder, in which the pressure force, the temperature on both the mold and the substrate sides, and the heating time were accurately controlled. The ICA used in the present experiments needed to be melted repeatedly in different steps. For this reason, a silver-filled thermoplastic ICA was used in the present study. After the imprinting step, the mold was removed and the ICA was formed as uniform pyramid-like structures.

Due to the microstructure of the adhesive, a continuous residual layer connecting the pyramid-like structures was left even a very high pressure was applied for a long time. A transfer process was implemented to produce discrete ICA patterns without the residual layer. A second Si substrate was placed close to the original substrate. The two substrates were kept in parallel and the gap between the two substrates was fixed and controlled to be slightly smaller than the height of the ICA pyramids during the transfer process. In this way the target substrate could touch and flatten the adhesive pyramids without touching the residual layer. The temperature of the original substrate was set at a low temperature and that of the target substrate was raised. This configuration allowed the thermoplastic adhesive to reflow only at the surface of the target substrate. The two substrates were separated afterwards and an array of discrete thin ICA films was produced on the target substrate.

Figure 4.2 shows the scanning electron microscopy images of patterned adhesive on the target substrate (a) and the flattened pyramid-like adhesive structures connected by the residual layer left on the original substrate (b).

**Transfer and formation of CNT arrays**

The carbon nanotube films used here consist of well-aligned multi-walled CNTs prepared by the atmospheric pressure thermal CVD process described in Section 3.2.

A chip with CNT film was pressed onto the chip carrying the ICA array under a pressure of roughly 500 kPa. The chips were heated up and then separated after cooling down. Because the CNTs are aligned in the film and only attracted to each other by weak van der Waals forces, they are easily separated by applying external forces. Transfer of CNTs and formation of CNT patterns are achieved simultaneously. The nanotubes held by the adhesion provided by ICA are transferred to the...
Chapter 4

Figure 4.2: (a) SEM image of discrete ICA patterns. These patterns were transferred from the top of the original imprinted pyramid-like ICA structures. (b) The imprinted ICA pyramids with flattened tops were left on the original substrate after the heat transfer process. The residual layer connecting the ICA blocks can also be seen.

Figure 4.3: (a) SEM image of an array of transferred CNT forests with ICA underneath. (b) Cavities left on the original CNT film.

target substrate and the remaining CNTs are left on the carrier substrate. 2-3 µm thick adhesive layers are proven to be sufficient to transfer CNT forests taller than 20 µm. An example of transferred and patterned CNT forests is shown in figure 4.3 (a) and the cavities formed in the original CNT film are shown in figure 4.3 (b).

To verify the establishment of electrical connection, the current-voltage (I-V) curve of the transferred CNT-ICA structure was measured by a two probe method. The I-V curve of one transferred CNT-ICA block is shown in figure 4.4. The I-V response is highly linear, indicating that a good electrical connection has been established as a result of the transfer process.
Another implementation of low temperature VA-CNT transfer studied in this thesis uses a low melting point metal, indium (In), as the assembly material. The transfer process is similar to that stated in the previous section. The CNT forests need to be coated with a titanium/gold (Ti/Au) layer before being transferred by indium to the target substrate, also covered by a Ti/Au layer. Bonding of the CNTs to the target at 170 °C for 2 min is sufficient for a successful transfer. A higher temperature (200 °C) and longer time (10 min) produce transfer results with a higher yield. Both patterned and non-patterned indium has been utilized to transfer the CNTs. 1 µm thick evaporated indium is enough to transfer CNT forests with a high yield. An SEM image of an array of VA-CNT forests transferred by indium is shown in figure 4.5.

The choice of assembly material for CNT transfer depends on the fields of ap-
Applying and patterning conductive adhesives is a thick-film technique. Therefore transfer by conductive adhesives is more suitable to be integrated into a flow of thick-film processes. For example, Soga et al. used printed conductive adhesives to transfer CNT forests acting as flip chip bumps [162], by a process very similar to that presented in the previous section. It is also more tolerant to the surface finish of the substrates.

On the other hand, transfer by metals, which can be deposited and patterned by thin-film technologies, is preferable for integrating CNTs onto micro-structures where thick-film materials are difficult to be applied. Working with thin films of metals also provides possibilities of finer patterning and better contacts. For instance, this transfer process using indium is utilized for the development of CNT-filled through-silicon vias, described in more detail in Section 6.4. A limitation of using metals for CNT transfer is that a certain surface finish is required to achieve a strong bonding for a successful transfer.
Chapter 5

Densification of carbon nanotube forests

This chapter introduces another basic process developed in this thesis project: densification of vertically-aligned carbon nanotube forests. Existing work on this process is briefly reviewed. Two different approaches, namely dry densification and vapor densification, are then reported.

5.1 Overview of densification of CNT forests

VA-CNT structures made by chemical vapor deposition are a highly porous material with a typical porosity above 90% [132], i.e. less than 10% of the total volume of a VA-CNT forest is occupied by CNTs. The high porosity of VA-CNT structures is an important advantage in certain cases, such as in sensing applications where a large surface area is desired. It is however a drawback in some other applications which require a high volume fractions of CNTs, as discussed in Section 3.4. For example, the high porosity makes VA-CNT structures ineffective in thermal and electrical transport, and also deteriorates their mechanical strength. Therefore it is essential to create VA-CNT structures in which the nanotubes are closely packed.

Attempts were made to optimize the catalyst to allow for direct growth of dense CNT forests [134–136]. However their density was still far from that of closely packed ones. An alternative approach is to densify the VA-CNT forests after their growth. Futaba et al. demonstrated that porous CNT forests could be densified to closely packed CNT solids by capillary force from a solvent in which they were immersed [171]. The interactions between CNTs and liquids were actually studied earlier to generate self-assembly in CNT films [68, 172–174]. This immersion-based wet densification method was applied to make CNT-polymer
composites [175] and to improve the electrical performance of CNT interconnects [176, 177]. This method was later modified in diverse ways to create dual-porosity CNT structures [178]. One of the modifications reported in ref. [178] was to expose the CNTs to a solvent vapor instead of direct immersion. The vapor densification method has been further investigated to create diverse CNT structures [179].

Besides, VA-CNT structures can also be densified by dry methods in which external forces were applied to press the CNTs together [180,181]. This approach is however not capable of densifying microscale patterned VA-CNT structures.

In this thesis project, two densification processes have been developed and investigated. They are reported in the following two sections.

5.2 Dry densification of CNT forests

Mechanism

A unique dry densification method has been developed and applied on VA-CNT forests. The mechanism of this dry densification method, as illustrated in figure 5.1 is based on sealing the surface of the CNT forest by the deposition of a thin sealing film at a low pressure. Afterwards, when the sealed CNT forest is returned to ambient pressure, a pressure difference almost equal to the atmospheric pressure is established between the outer and the inner sides of the deposited thin film. This large pressure difference makes the thin film deform inwards. Consequently the CNTs are compressed to form a densified bundle. Thin film sealing has already been proven a useful method to seal porous low-k materials used for integrated circuit fabrication [182–184]. CNT forests or films are typically highly porous materials with pore sizes in tens of nanometers [185]. In this study it is demonstrated that thin film sealing can be used as an efficient densification method.

This concept has been verified by finite element method (FEM) modeling using COMSOL Multiphysics (version 3.5, COMSOL). For simulation purposes a group of 10 parallel aligned carbon nanotubes, 10 µm long and 20 nm in diameter, is set up (see the leftmost part of figure 5.1 (b)). The CNTs are placed 80 nm apart from each other and are covered with a thin layer of SiO₂, 200 nm thick on the top surface and 100 nm thick on the side wall. This structure is much simplified so that it is possible to compute this simulation with a common computer. Therefore the results from this simulation cannot be directly compared to the experimental results. The simulation structure before applying the pressure is shown as the leftmost structure in figure 5.1 (b). The boundary conditions are then given by the leftmost tube and the roots of the tubes being fixed. A 10⁵ Pa pressure (about one
Figure 5.1: (a) Illustration of the mechanism of the dry densification process. (b) FEM simulation of a simplified model with 10 parallel aligned CNTs. The color bar indicates the horizontal displacement in µm.

atmospheric pressure) is applied to the top and rightmost surfaces of the structure. The simulation result shown as the rightmost structure in figure 5.1 (b) indicates that a nanotube forest can be largely deformed inward by the pressure difference between the inner and outer sides of the sealing layer.

Experimental verification

The CNT forests used in the experimental study were synthesized by the low pressure thermal CVD process described in Section 3.2. To seal the CNT forests, thin SiO\textsubscript{2} films were deposited by reactive sputtering. By varying the deposition time, sealing SiO\textsubscript{2} layers with thicknesses ranging from 25 to 200 nm were deposited. The thickness values given here and throughout this section indicate the thicknesses of films deposited on a flat substrate by the same process for the same deposition time. Due to the porous surface of the CNT forests and the anisotropic nature of the deposition processes, the actual film thicknesses on the top surfaces and on the sidewalls of the CNT forests are difficult to define.

Some SEM images of CNT forests before and after the densification process are demonstrated in figure 5.2. For these CNT forests, which are approximately 50 µm in diameter and 150 µm tall, a 50 nm thick SiO\textsubscript{2} layer was proven to be
enough to produce a profound densification effect. The mushroom-like shape of the densified forests can be clearly observed, meaning that the middle sections of the forests are more closely densified than the fixed top and bottom surfaces. In average, the diameter at these locations is densified to $26 \pm 3\%$ of its original value. The calculation of this densification result is based on measuring the diameters of the narrowest densified sections in the SEM images. Thus the volume in the middle section of the forests is densified to roughly 7% of the original size. This result matches the 90% porosity value measured by Puretzky *et al.* [132] from similar VA-CNT films. To further validate the proposed dry densification mechanism, the top and side surfaces of the CNT forests were examined before and after the densification. SEM images of the porous top and side surfaces of an as-grown CNT forest is shown in figure 5.2 (c) and (d). The same surfaces after deposition of the sealing SiO$_2$ film are shown in 5.2 (e) and (f). The dense structures clearly indicate that the porous surfaces have been sealed by the deposited thin film.

**Further investigation**

As expected, the thickness of the sealing film is crucial for the densification process. If the film is too thin it will not have the expected sealing effect.
5.3 (a-d) show some SEM images of CNT forests originally of the same size but sealed with films of four different thicknesses. The four different thicknesses of the SiO₂ layers are 25, 50, 100, and 200 nm, respectively. It is obvious that a sealing film of 25 nm thickness (figure 5.3 (a)) produces less densification than the other three samples with SiO₂ layers at least 50 nm thick. This may be due to the different levels of hermeticity produced by the thin films of different thicknesses.

For comparison, immersion-based wet densification was also executed. A method similar to that in ref. [171] was utilized. It is done by immersing the sample into isopropyl alcohol (IPA) for 1 min and then letting it dry naturally in air. The results of these densification experiments are shown in figure 5.3 (g) and (h). The diameter of the most densely packed parts of the CNT forests is 28 ± 4% of their original size.

The dry and wet methods can reach similar densification levels. However, two major differences can be seen between the results of the dry and wet densification methods. The first one is the mushroom-like shape of the dry densified forests, which has not been observed in the wet one. In the dry densification, the thin films deposited on the top surface of the forests may be the factor preventing the densification in the upper sections. The same phenomenon is noticed in the simulation result (figure 5.1 (b)). The second difference between the dry and wet methods is the uniformity of the shape control during the densification across the chip. Comparing figure 5.3 (e) and (f) to (g) and (h), it can be clearly observed that the dry process generates better uniformity in controlling the shapes of the densified forests than the wet process. An analogy to the dry etching processes used in microfabrication can be made here. Dry etching has been favored by the industry due to several key advantages, such as better controllability, better repeatability, and less chemical waste [186].

The dry densification process also demonstrates a good scalability concerning the diameter of the forests. CNT forests of different diameters have been densified through the same process. Figure 5.4 (a) and (b) display the successfully densified CNT forests which are originally 10 µm and 100 µm, respectively, in diameter. Thin films made by plasma-enhanced CVD have also been proven to deliver a similar densification effect, revealing the generality of this process. One example is shown in figure 5.4 (c), where CNT forests are shown to have been effectively sealed during densification, protected by 100 nm thick PECVD SiO₂. It can be expected that by optimizing the thin film deposition processes to make them capable of sealing nanometer scale pores, various materials and thin film deposition techniques can be applied for this densification purpose. Besides, the dry densification process has been proven to be irreversible. No change of the shape of the forests can be detected after removing the SiO₂ on their top surfaces by dry etching (see figure 5.4 (d)).

Despite the advantages discussed above, this method also has a few limitations.
Figure 5.3: SEM images of various densification results. (a-d) CNT forests densified by reactive sputtered SiO$_2$ layers with different thicknesses. ((a) 25 nm. (b) 50 nm. (c) 100 nm. (d) 200 nm.) (e) and (f) Zoomed out view of the samples shown in (a) and (b) respectively. (g) and (h) CNT forests of the similar dimensions as in (a-f) densified by the wet method.
Densification of carbon nanotube forests

Figure 5.4: (a) Densified CNT forests with an original diameter of 10 µm. (b) Densified CNT forests with an original diameter of 100 µm. (c) Densified CNT forests by SiO\textsubscript{2} deposited using PECVD. (d) Densified CNT forests after the SiO\textsubscript{2} layer being dry etched. The inset shows the top surface of the forests with SiO\textsubscript{2} removed.

compared to its wet counterpart at this stage. First, there is a fundamental difference between the mechanisms of the dry and wet densification. In the wet one, the driving capillary forces are applied on all the nanotubes in forests or films by the liquids penetrating into the pores. Conversely, in this dry densification method the forces are applied from outside of the CNT forests, thus only directly applied on those CNTs in the outer part of the forests. The dry method is also very dependent on creating sealed surfaces composed of the deposited thin films and the substrate. These factors make it difficult to apply the dry densification to large and freestanding CNT films, such as the wet densified films in ref. [171]. Moreover, although the uniformity between the densified forests is superior in the dry method, the homogeneity of the densification effect through the vertical axis in one structure is poorer due to the SiO\textsubscript{2} layer on the top surface. The middle sections are much more densified than their tips and roots. This naturally leads to a poorer overall densification effect although the middle sections can be densified to a similar level as in the wet method. Another potential weakness of the dry method worth pointing out is that the deposited sealing films may be difficult to remove completely. This may hinder the use of the dry densification in certain applications.
5.3 Vapor densification of CNT forests

Mechanism

In the present thesis, a new vapor densification method has also been developed and investigated. The major difference between this vapor method and the immersion-based one is the possibility of collecting a small amount of solvent on the CNTs, which eliminates the interactions between neighboring structures during evaporation of the solvent to achieve a uniform densification effect across the whole chip. The novelty of the method presented in this thesis is that the exposure time of the CNTs to the solvent vapor is introduced into the method as a control parameter so that the amount of solvent collected on the CNTs can be accurately varied to create different degrees of densification. The method is demonstrated to be capable of producing various three-dimensional (3D) VA-CNT structures with high controllability and uniformity.

The experimental setup of the vapor densification is illustrated in figure 5.5 (a). A chip carrying CNT forests was placed on a lid above a beaker of boiling solvent. The solvent used here was acetone diluted in water, heated to 75 °C. Other solvents, such as isopropanol and methanol, were also proven be able of delivering similar densification results. The entire vessel was closed. Longer exposure time led to more solvent condensed on the chip.

The mechanism of the vapor densification effect is explained in figure 5.5 (b). By exposing the CNT structures to the solvent vapor for different time, the amount of solvent condensed on the CNT structures can be controlled to generate different degrees of densification. After short exposure, the amount of solvent collected is small and only causes the top parts of the forests to densify. Long exposure leads to more collected solvent on the chip and makes the forests to densify fully.

This mechanism is verified by a series of densification experiments done for different time (figure 5.5 (c-h)). Figure 5.5 (c) shows an example of an array of as-grown CNT forests, 200 µm in diameter and roughly 500 µm tall. After 20 s exposure to the solvent vapor, only the top parts of the forests are densified, forming truncated cone structures (figure 5.5 (d)). Results after 30, 40, 50, and 60 s densification are displayed in figure 5.5 (e-h) respectively. It can be clearly observed that the densified sections extend from the top towards the bottom of the CNT forests with increasing exposure time. This contradicts the observation in ref. [179] where the densification seemed to start from the base. For the CNT forests work with the dimensions as mentioned above, they are fully densified after exposing to the solvent vapor for 60 s. High-magnification SEM images of the side walls of the CNT forests (figure 5.5 (i) and (j)) reveal the shrank gaps between the aligned nanotubes after the densification.
Figure 5.5: (a) Illustration of the experimental setup of the vapor densification. (b) Illustration of the mechanism of the vapor densification. (c) Un-densified CNT forests. (d-h) CNT forests densified after exposing to the solvent vapor for 20 (d), 30 (e), 40 (f), 50 (g), and 60 (h) seconds. (i) Aligned CNTs in an Un-densified forest. (j) Closely packed aligned CNTs in a densified forest. (k, l) A needle-like densified CNT forest with small dimension (~2 µm in diameter) and high aspect ratio (~10). (m) CNT forests made upside down by a transfer process.
Chapter 5

Scalability and uniformity

The vapor densification method was also applied on small structures to investigate its scalability and capability of fabricating high-aspect-ratio structures. As an example, a needle-like densified CNT forest approximately 2 µm in diameter and with a high aspect ratio of roughly 10 is shown in figure 5.5 (k) and (l). Densification processes can make typical CNT forests to shrink to about 20% - 40% of its original size in lateral directions. This means that the aspect ratios of as-grown CNT forests, which can already be made quite high, can be increased further by a few times through densification.

Moreover, the vapor densification method presented in this study is capable of generating dual-porosity CNT structures, similar to those made in ref. [178]. A progress made in this work is that the position where the upper low-porosity (densified) and the lower high-porosity (un-densified) sections are separated can be tuned by easily changing the densification time. Combined with the previously reported post-growth transfer techniques for CNTs, these structures can be reversed so that the high-porosity parts are on the top and the low-porosity parts are on the bottom in contact with the substrate.

Another important advantage of the vapor densification method is the good uniformity of densified structures across the chip, which is achieved by eliminating the interactions between neighboring structures owing to the very small amount of solvent involved in the process. On the other hand, in the immersion-based wet densification process the evaporation of large amount of solvent collected between neighboring structures causes bending and distortion of the forests, resulting in poor uniformity after densification. The heights of two samples each containing an array of 8 × 8 CNT forests and prepared in the same batch, one un-densified and one densified by vapor densification, are presented in table 5.1. The as-grown CNT forests are highly uniform, the standard deviation being lower than 0.3% of the average height. The vapor densification process only slightly deteriorates the uniformity. The standard deviation of the forest heights is still lower than 1% of the average height after densification. Heights of the tallest and shortest forests are both within 10 µm from the average value, 368.6 µm. This good uniformity makes the vapor densification method applicable in those applications requiring good uniformity of CNT structures across a big surface, such as interconnects and field emission sources.

Further investigation

It is also found that the densification results are highly dependent on the intrinsic properties of the CNT forests. CNT forests with different volume fractions were prepared and densified. Figure 5.6 (a), (d) and (j) show the SEM images taken on
Table 5.1: Heights of one un-densified and one densified array of 8 × 8 CNT forests.
(All values are in µm.)

<table>
<thead>
<tr>
<th></th>
<th>Un-densified</th>
<th>Densified</th>
</tr>
</thead>
<tbody>
<tr>
<td>Average height</td>
<td>523.6</td>
<td>368.6</td>
</tr>
<tr>
<td>Standard deviation</td>
<td>1.4</td>
<td>3.5</td>
</tr>
<tr>
<td>Maximum height</td>
<td>527.6</td>
<td>375.6</td>
</tr>
<tr>
<td>Minimum height</td>
<td>521.5</td>
<td>358.7</td>
</tr>
</tbody>
</table>

the side walls of such as-grown CNT forests. This variation of volume fraction of CNTs in their forests is achieved by varying the temperature at which the growth is initiated, higher initiation temperature producing bigger and sparser catalyst particles and thus lower volume fraction of CNTs. For forests with high CNT volume fraction, their original shape (circular in this case) is maintained after the densification (figure 5.6 (b) and (c)). For more porous CNT forests, their original shapes are distorted after densification (figure 5.6 (e), (f), (k), and (l)). It is interesting to notice that self-assembled patterns is observed on very sparse CNT forests after densification (figure 5.6 (l)), similar to those previously reported [174], but not on denser CNT forests.

It was argued by De Volder et al. that this distortion after densification was due to the top entangled parts of CNT forests and removing them by O$_2$ plasma helped to maintain the original shapes [187]. It is found in this investigation that this technique only works for CNT forests within a certain range of volume fraction. The structures of plasma treated CNT forests are shown in figure 5.6 (g) and (m). The cone-like shapes after this treatment agree well with those previously studied [188]. For the sample with medium CNT volume fraction (shown in figure 5.6 (d-f)), removal of the top entangled sections makes the shape distortion much less noticeable (figure 5.6 (h) and (i)). On the other hand, for those with low CNT volume fraction (shown in figure 5.6 (j-l)), this modification makes no improvement in keeping the original shapes (figure 5.6 (n) and (o)). It is also observed in this case that the self-assembled patterns as in figure 5.6 (l) do not appear in densification after the sample being treated by O$_2$ plasma (figure 5.6 (o)), indicating that the self-assembly of CNTs in this kind of structures is strongly related to the entanglement of CNTs in the top sections.

The relation between the shape distortion after vapor densification and the CNT volume fractions is further investigated by densifying CNT forests patterned in other shapes, square and hexagon as two examples. The original shapes are well preserved after densification if the CNT volume fractions are high (figure 5.7 (a), (b), (e), and (f)). For sparse CNT forests, the vapor densification process changes the original polygonal shapes to star-like ones (figure 5.7 (c), (d), (g), and (h)).
Figure 5.6: Densification results of CNT forests with different volume fractions. (a-c) CNT forests grown at an initiation temperature of 500 °C. (d-f) CNT forests grown at an initiation temperature of 600 °C. (g-i) The same as in (d-f), but treated with O₂ plasma. (j-l) CNT forests grown at an initiation temperature of 700 °C. (m-o) The same as in (j-l), but treated with O₂ plasma. The images in the first column (a, d, g, j, and m) were taken before densification, showing the alignment and porosity of the CNTs. All the other images were captured after densification.
Figure 5.7: Densification results of CNT forest in different shapes. (a-d) Densification of square patterns. (e-h) Densification of hexagonal patterns. The images in the second column (b, d, f, and h) are magnified views of those in the first column (a, c, e, and g).
Chapter 5

This vapor densification method is chosen to be used in the development work of CNT-filled through-silicon vias, which will be introduced in detail in Section 6.4.
Chapter 6

Carbon nanotube-filled through-silicon vias

This chapter deals with using carbon nanotubes as a filling material in through-silicon vias. The chapter starts by briefly introducing three-dimensional integration and the role of TSVs in this technology. After that, a general discussion on the use of CNTs as interconnects is presented. The experimental realization of CNT-filled TSVs (abbreviated as “CNT-TSVs” in the rest of this thesis) in two different ways is then described, followed by a demonstration of a simple scheme to interconnect CNT-TSVs.

6.1 3D integration and TSVs

Continuous size miniaturization and performance promotion of electronics can be achieved through both the downscaling of on-chip transistors and the progresses of packaging technology. While the integration of more transistors on a single integrated circuit is becoming more and more difficult and costly, high-density integration at the system level, supported by advanced packaging solutions, is expected to be the main driving force for the future shrinking and performance improvement of electronics [2].

One recent focus in the field of electronics packaging is the vertical stacking of ICs to form 3D integration [3, 189], which offers some important advantages. First, a much higher integration density can be obtained by stacking multiple ICs on the footprint of only one chip. Second, 3D integration significantly shortens the lengths of interconnects between different components, thus reducing signal delays in a system, as well as the power consumption.

Furthermore, 3D integration technology allows true heterogeneous integration of various components onto a system-on-package platform to achieve a complete
functional unit in a tiny space. Thus 3D integration becomes an important building
block in the “More-than-Moore” scheme, which addresses growth in the diversity
of functions and technologies rather than the extreme miniaturization predicted by
Moore’s Law [190].

The realization of 3D integration falls into two major categories: 3D Si inte-
gration and 3D IC integration [191]. In 3D Si integration, stacking is achieved
through direct wafer-to-wafer bonding, by either copper-to-copper [192, 193] or
oxide-to-oxide bonding [194, 195], without using any bumps. In contrast, 3D
IC integration technology uses micro bumps to connect stacked ICs [4]. 3D Si
integration has some advantages over 3D IC integration, including better elec-
trical performance, less power, lower profile, etc., but is more difficult to im-
plement [191]. Therefore the recent application of 3D integration favors 3D IC
integration, whereas 3D Si integration is the industry’s long-term preference.

A central task in 3D integration is to build reliable and efficient electrical
interconnects for signal transfer and power distribution among the stacked lay-
ers. Although conventional wire-bonding technology has already been applied
for this purpose [189], a true 3D integration, with high integration density and
input/output counts, and short interconnection lengths, can only be achieved by
TSV interconnects. * Besides 3D integration, the TSV is also a favorable choice
in some sensing applications where a direct connection to the sensing side is
needed [197, 198].

While there are a number of mature etching techniques widely available to
create high-aspect-ratio vias in silicon, deep reactive ion etching (DRIE) being
the most prominent example, the major difficulty in TSV development lies in the
filling of a conductive material in deep vias, as well as their interconnection and
insulation.

The most common method to fill TSVs is electroplating copper (Cu), the reli-
ability of which is, however, a serious concern [199, 200]. The manufacturability
of Cu-filled TSVs is also a barrier towards their successful application due to
highly demanding fabrication processes, such as seed and barrier layer deposi-
tion in high-aspect-ratio vias [201]. Some other materials, such as tungsten and
polysilicon [202, 203], have also been used as via filling materials but all have
limitations in reliability, manufacturability, and performance.

In this thesis, I explored the possibilities of using CNTs as a filling material in
TSVs, the potential of which has been predicted by recent modeling work [204,
205].

*The concept of using a through-via in Si to connect components vertically can be traced back
to a patent filed by Shockley, the co-inventor of transistor, in 1958. The patent was granted in
1962, with a US patent number of 3,044,909 [196].
6.2 CNTs as interconnects

The electrical, thermal, and mechanical properties of carbon nanotubes have been described in the Section 2.2. Some of the properties, for example their high current carrying capacity, low electromigration and Joule heating, high thermal conductivity, mechanical flexibility and low thermal expansion, are very attractive for interconnect application. Hence, CNTs have been proposed as a promising candidate material to build next generation interconnects in miniaturized electronics, as both on-chip and off-chip interconnects.

Modeling

A series of modeling work on CNT interconnects has been done by Naeemi and Meindl [206–209]. A very simplified introduction to the basis of their work is given in this subsection.

Based on Landauer formula [210] and the band structure of a SWNT [24], the average number of conduction channels of a SWNT (may also be considered as one shell) or a shell of a MWNT can be approximately expressed as

\[
N_{\text{chan}} \approx \begin{cases} \frac{aT D + b}{\frac{D}{T}} & D > \frac{d_T}{T} \\ \frac{2}{3} & D < \frac{d_T}{T} \end{cases},
\]

(6.1)

where \(a \approx 3.87 \times 10^{-4} \text{nm}^{-1} \text{K}^{-1}\), \(b \approx 0.2\), †\(T\) is the temperature, \(D\) is the diameter, and \(d_T = 1400 \text{nm K}\). Equation 6.1 is valid in the low voltage bias range, which is applicable for electronic interconnects. The expression is based on the assumption that one third of the tubes or shells are metallic. At room temperature \((T = 300 K)\), \(d_T/T\) is about 4.3 nm and \(aT\) in equation 6.1 can be replaced by \(a' \approx 0.116 \text{nm}^{-1}\). The estimation of conduction channels by Naeemi and Meindl’s model agrees well with another model developed by Forestiere et al. [211].

For a CNT with a length \(L\) shorter than its electron mean free path \(\lambda\), the conductance per channel is \(G_{\text{chan}} = G_0\), where \(G_0\) is quantum conductance \((2e^2/h, 1/12.9k\Omega^{-1})\). For \(L > \lambda\), the conductance per channel can be expressed as [210]

\[
G_{\text{chan}} = \frac{G_0}{1 + \frac{L}{\lambda}}.
\]

(6.2)

For SWNT bundles, the total conductance is given by

\[
G_{\text{swnt bundle}} = \sum_{\text{all tubes}} N_{\text{chan}} G_{\text{chan}}.
\]

(6.3)

†The \(a\) and \(b\) taken here are corrected values used in ref. [208] and [209], which are different from those they used in ref. [206] and [207].
In equation 6.3, $N_{\text{chan}}^{\text{tube}}$ is the same as the $N_{\text{chan}}^{\text{shell}}$ in equation 6.1 because for a SWNT a tube has only one shell.

For a simplified case where $N_{\text{swnt}}$ SWNTs have the same diameter, $D < 4.3 \text{ nm}$, and the same length, $L > \lambda$, equation 6.3 becomes

$$G_{\text{swnt bundle}} = \frac{2}{3} N_{\text{SWNT}} \frac{G_0}{1 + \frac{L}{\lambda}}.$$  \hspace{1cm} (6.4)

For one MWNT, its total conductance can be calculated as

$$G_{\text{mwnt}} = \frac{D_{\text{max}} - D_{\text{min}}}{2\delta} N_{\text{chan}}^{\text{shell}} G_{\text{chan}},$$ \hspace{1cm} (6.5)

where $D_{\text{max}}$ and $D_{\text{min}}$ are the outer and inner diameters of the MWNT, respectively, and $\delta$ is the inter wall distance $\sim 0.34 \text{ nm}$. For a simple case when $N_{\text{MWNT}}$ MWNTs have the same diameters, $D_{\text{min}} > 4.3 \text{ nm}$, lengths, $L > \lambda$, and an average diameter $\bar{D}$, the total conductance of this MWNT bundle is

$$G_{\text{mwnt bundle}} = N_{\text{mwnt}} \frac{D_{\text{max}} - D_{\text{min}}}{2\delta} (a'\bar{D} + b) \frac{G_0}{1 + \frac{L}{\lambda}}.$$ \hspace{1cm} (6.6)

Finally the resistance is

$$R = G^{-1}.$$ \hspace{1cm} (6.7)

Only the resistance component is described here because the focus of this work is on characterizing and decreasing the resistivity of VA-CNT forests as a TSV filling material. The modeling of the capacitance and inductance components of CNT interconnects can be found in ref. [212, 213]. A high frequency analysis of CNT interconnects has also been performed [111], in which one interesting conclusion is that the skin effect of CNT interconnects is significantly less severe than that of metal lines.

**A reality check**

Based on the model described above, the resistances of CNT off-chip interconnects, such as TSVs, can be estimated by straightforward calculations assuming some typical dimensions. A MWNT with 30 nm outer diameter and 15 nm inner diameter, 100 µm length, and 1 µm electron mean free path, at room temperature has a conductance of 0.048 k$\Omega^{-1}$, calculated using equation 6.5. This leads to an estimated resistance of 21 k$\Omega$ for such a MWNT if all its walls can be contacted. Note that here the electron mean free path is taken as 1 µm based on experimental observations such as in ref [214]. In modeling papers such as ref. [110, 206], the
Carbon nanotube-filled through-silicon vias

Figure 6.1: Arrangement patterns of CNTs in a forest or bundle. (a) Loosely packed with roughly 93% porosity. (b) Closely packed with an inter tube distance of $\delta \approx 0.34$ nm. (Not drawn to scale.)

$\lambda$ value is set to be 1000 times of the tube diameter, which is a very optimistic assumption and consequently leads to a much higher estimated conductance.

Two arrangements of a forest or bundle of these MWNTs can be presumed and their corresponding resistance can be estimated as follows.

In the first pattern (figure 6.1 (a)), the CNTs are assumed to be arranged in a square lattice with 70 nm spacing between the neighboring tubes. This leads to a site density of 100 tubes per $\mu m^2$ ($10^{10}$ cm$^2$) and a porosity of roughly 93%, which is close to an experimentally measured value (92%) for a typical MWNT film [132]. In this case the resistance of a forest $50 \mu m$ in diameter can be calculated as $21 k\Omega/[100 \mu m^{-2} \cdot \pi \cdot (50 \mu m/2)^2] = 0.11 \Omega$. If the CNTs are closely packed in the bundle with the inter tube distance of $\delta$ (the inter layer distance in graphite, $\sim 0.34$ nm) as illustrated in figure 6.1 (b), the site density of CNTs is $1.28 \times 10^3$ tubes per $\mu m^2$ ($1.28 \times 10^{11}$ cm$^2$). The resistance of a bundle with the same diameter is then $21 k\Omega/[1.28 \times 10^3 \mu m^{-2} \cdot \pi \cdot (50 \mu m/2)^2] = 8.4 m\Omega$.

The resistance values calculated above for a $100 \mu m$ long MWNT structure $50 \mu m$ in diameter in both loosely and closely packed cases are acceptable values for off-chip interconnect applications, showing the feasibility of using CNTs for this purpose. The estimation also reveals the importance of producing closely packed CNTs in a good structural quality.

Requirements

Based on the discussion above, the following requirements for CNT-based interconnects can be identified. Some of these requirements correspond closely to the problems of as-grown VA-CNTs listed in Section 3.4. Therefore for these points any detailed discussion is skipped here, and can be found in Section 3.4.
• High structural quality of CNTs. The structural quality of CNTs directly affects the performance of CNT-based interconnects.

• Large fraction of metallic CNTs. It is important for applications requiring the use of SWNTs. This is however not a must if MWNTs with large diameters are used as interconnects.

• Large volume fraction of CNTs in the structures. In Chapter 5, this issue is discussed and a solution is provided.

• Good compatibility with existing materials, devices, and manufacturing processes. The focus is the growth temperature of CNTs. In Chapter 4 this issue is discussed and a solution is provided. Contact of CNTs with other materials is another important subject. The contacts between CNTs and different metals have been made and compared [215–217], showing the possibility to achieve ohmic CNT-metal contacts with low resistances. Rapid thermal annealing has been used to decrease the contact resistance and to improve the contact’s long time stability [216, 218].

• Reasonable process time and manufacturing cost. As any practical technology, the time and cost of making CNT-based interconnects must be taken into account. No significant additional process time is expected because growth of CNTs is generally a quick and parallel process which normally lasts for a few minutes to one or two hours. The subsequent processes are also standard manufacturing processes. Recent development of commercial CNT growth systems makes CNT growth very close to a standard and cost-effective manufacturing process [219, 220].

Experimental development

Attempts have also been made experimentally to develop CNT-based interconnects, both for on-chip and off-chip interconnection.

On-chip interconnects based on CNTs have been realized through various technical routes. The majority of the work is focusing on vertically aligned CNTs in via interconnects [40, 221–227]. The CNTs are directly grown from the bottom of the vias. Polishing methods have been applied to make good contact to MWNTs [40, 223, 225]. The best result achieved so far, to the author’s knowledge, is reported by Yokoyama et al. [40, 225], 0.6 Ω resistance for a via 250 nm deep and 2 μm in diameter. CNT on-chip interconnects in the form of horizontal wires have also been demonstrated [228–230]. In ref. [230] one horizontally placed 13 μm long MWNT is measured to have a resistance of 49 kΩ.
Carbon nanotube-filled through-silicon vias

Figure 6.2: Fabrication process of the CNT-filled TSVs. (a) Photolithography to define the shapes and patterns of the vias. (b) DRIE to etch deep vias into Si. (c) E-beam evaporation of the catalyst layer. (d) Stripping the photo resist to remove the catalyst deposited on the top of the Si, leaving catalyst only at the bottom of the vias. (e) TCVD to grow CNT forests from the bottom of the vias. (f) Deposition of supporting layer. (g) Lapping and CMP to planarize the Si-CNT structure. (h) Photolithography, evaporation and lift-off to form metal pads on the front side. (i) Dry etching of Si from the backside to expose the bottom of the vias. (j) Sputtering of conduction layer onto the backside.

Off-chip interconnects bridging chips to substrates or to other chips based on CNTs are also under intensive development. Iwai et al. and Soga et al. have fabricated and assembled CNT flip chip bumps, which are highly thermally conductive and mechanically flexible [16, 162]. Hermann et al. have demonstrated that CNT-based flip chip bumps have good long time stability under thermal stress [231]. Yung et al. made “Velcro”-like CNT assembly and proposed to use this structure for flip chip interconnects [232]. Xu et al. fabricated CNT based through wafer interconnects [17]. In the following sections, the experimental progresses made on CNT-TSVs during this thesis project are introduced.

6.3 TSVs filled with planarized CNT forests

Overall process

A basic fabrication process of the CNT-filled TSVs is shown in figure 6.2. The process started by photolithography on a Si wafer. The Si wafer was then etched by a DRIE process to create vias of different depth. The catalyst layer was then evaporated onto the wafer and selectively removed in a lift-off process, leaving it only at the bottom of the Si vias. These preparation steps for CNT growth are illustrated in figure 6.2 (a-d).

The growth of the CNTs in these vias, already introduced in Section 3.3, is illustrated in figure 6.2 (e). The Si-CNT structure was planarized afterwards (figure 6.2 (f) and (g)). A few post planarization steps were performed to ease the
electrical measurement (figure 6.2 (h-j)).

**Planarization**

One important step in the process flow is the planarization process of the as-grown CNT-Si structure (figure 6.2 (f) and (g)). This planarization process is necessary due to the difficulty of controlling the length of all the CNTs so that these are exactly equal to the depth of the Si vias. The flat surface created by this planarization process will enable the subsequent processing steps on the CNTs, such as metalization and bonding. Horibe et al. [223] and Yokoyama et al. [40] also claimed that the polishing of multi-walled CNTs may make their inner shells contribute to the electrical conduction. The conduction of the MWNT forests can thus be improved.

Prior to the planarization of this structure, a supporting layer was deposited to hold the CNTs. Otherwise the CNTs are easily deformed or pulled out of the vias during the planarization process. Both the work of Horibe et al. [223] and Yokoyama et al. [40] focused on the development of on-chip vertical CNT via interconnects, the depth of which is below 0.5 µm. The top of the as-grown CNT forests in their work is only about a half to a few micrometers higher than the surface of the chip. Therefore they could deposit a thin supporting layer and employ chemical mechanical polishing (CMP) afterward to flatten the structures. Horibe et al. [223] used a spin coated thin photoresist and Yokoyama et al. [40] used a spin-on glass layer for this purpose. In the present case, the length of the CNTs is on the order of a few hundred micrometers and they stick out from the chip surface for more than tens of micrometers. Therefore a thick supporting layer has to be used in our study. A thick negative photoresist SU-8 was thus chosen as the supporting layer. Approximately 15 µm thick SU-8 was then spin coated onto the chip, followed by a soft bake, exposure to ultraviolet (UV) light, and post-exposure soft bake. Hard bake was finally done to further cure the SU-8 layer.

The planarization of the CNT-Si structure was achieved by a combination of lapping and CMP. The lapping step quickly removed the materials, followed by the CMP step to fine polish the surface. The lapping step was done on a glass lapping plate assisted by a suspension containing Al₂O₃ powders. After the supporting SU-8 layer was removed, the sample was further polished on a polishing cloth with a polishing fluid. Both the lapping and CMP steps were done under low pressure. After the CMP the sample was rinsed in acetone and deionized water and it then underwent a post-CMP cleaning process similar to the standard cleaning of Si wafers.

The lapping and CMP processes described above are shown to be able to effectively planarize the CNT-Si structures. Figure 6.3 shows SEM pictures taken
both before and after the planarization step. The flat surface created by the planarization is essential for some subsequent processes.

**Electrical testing**

A series of processes was executed after the planarization to finalize the fabrication of the CNT-TSVs and to facilitate the electrical measurement (figure 6.2 (h-j)). First, Ti/Au pads were made on the top of the planarized CNT forests by photolithography, evaporation and lift-off processes. A dry etching process was then done to remove the Si from the backside of the chip until the bottom of the vias is revealed. A Ti/Au layer was sputtered on the etched backside to form a conducting surface.

The current-voltage response of the CNT-filled vias was measured by two probe method. The measured I-V curves of the CNT vias are highly linear, three examples of which, measured from vias with 50 µm diameter and 86 µm, 120 µm and 139 µm depth respectively, are shown in figure 6.4 (a). These three samples grown by the low pressure process have 0.21 kΩ, 0.28 kΩ, and 0.34 kΩ resistances respectively. From the depths and resistances measured, it can be estimated that the contact resistance in the stated configuration is much smaller than the bulk resistance of the CNT forests (figure 6.4 (b)) using transfer length method (TLM) [233], although further investigation on this issue needs to be done. Vias, 50 µm in diameter and 125 µm deep, filled with CNTs grown by the atmospheric pressure process were also measured. The resistance of the vias in these dimensions is approximately 1.8 to 2.0 kΩ, which is about one order higher than that grown at low pressure probably due to the poorer tube quality grown at high pressure. This value is however very close to the result previously reported by Xu et al. [17].
Figure 6.4: (a) I-V curves of a measured CNT-TSV. S1 (square): 86 µm deep via; S2 (circle): 120 µm deep via; S3 (diamond): 139 µm deep via. (b) Estimation of the contact resistance based on S1, S2, and S3. The total contact resistance is where the dashed line intercepts the y-axis.
6.4 TSVs filled with densified and transferred CNT forests

Process flow

A more complicated approach to fabricate CNT-based TSV interconnects with CMOS compatibility and low resistances is also developed. The methodology presented here overcomes the two limitations of the basic process described in the previous section, by deploying a densification process to densify the CNT forests and a transfer process to lower the manufacturing temperature.

The fabrication process of these CNT-filled TSVs is illustrated in figure 6.5. It started with LP-TCVD of aligned CNT forests on a Si substrate at a high temperature (figure 6.5 (a)). The as-grown CNT forests were then densified to form closely packed CNT bundles by the vapor densification method presented in Section 5.3 (figure 6.5 (b)). Subsequently, this chip carrying densified CNT forests was aligned and transferred to another chip with vias prepared and a layer of indium on the bottom of the vias at a low temperature using the process described in Section 4.3 (figure 6.5 (c-e)).

The finished CNT-in-via structure was then spun coated with a layer of benzo-cyclobutene (BCB) polymer to fill the gaps between the CNTs and the sidewalls of the vias (figure 6.5 (f)). BCB is commonly used as a dielectric material in packaging of electronics and has already been utilized in a previous studies to fill deep trenches for TSV applications with a capability of being planarized by CMP [234, 235]. A planarization process consisting of a lapping step to quickly remove the materials and a CMP step to generate a fine surface finish was applied to flatten the CNT-BCB structures (figure 6.5 (g)). The BCB also acted as a supporting material in the planarization step. Finally Ti/Au pads were deposited and patterned on the flattened top of the CNT-TSVs to finish the fabrication process flow (figure 6.5 (h)).

Results and discussion

Some SEM images of the fabricated structures are shown in figure 6.6. The vertically-aligned CNT forests, before and after the densification, are displayed in figure 6.6 (a) and (b) respectively. The diameter of the top parts of these forests shrinks to approximately 40% of its original value. At the central parts, where most intensive densification happens, the diameter is decreased to roughly 30% of its value before the densification. This non-uniformity of densification in the vertical direction is caused by the top entangled CNTs grown in the initial stage of the CVD. It is expected that this can be improved by optimizing the CVD process or
Figure 6.5: Illustration of the fabrication process of TSVs filled with densified CNT forests. (a) VA-CNT forests were grown by the LP-TCVD at a high temperature (700 °C). (b) The as-grown CNT forests were densified through a vapor densification process. (c) The target chip was prepared with an indium layer on the bottom of the vias. (d) The two chips in (b) and (c) were aligned and then bonded at a low temperature (200 °C). (e) The growth substrate was separated. (f) BCB was spin-coated to fill the gaps between the CNTs and the sidewalls of the vias. (g) The BCB-supported CNT forests were planarized. (h) Metallic pads were formed on the CNT-filled vias.
by removing the entangled CNTs before the densification. Figure 6.6 (c) and (d) are SEM images of the sidewalls of the forests before and after the densification, revealing the good alignment of the CNTs in these structures. The gaps between the nanotubes in as-grown forests are unnoticeable after they are densified.

A CNT forest transferred into a TSV is shown in figure 6.6 (e). Herein CNTs originally grown from a catalyst layer patterned 200 µm in diameter is packed into a via 100 µm in diameter. Higher filling content of CNTs in vias can be reached by reducing the gaps between the CNTs and the sidewalls of the vias. The CNTs need to be slightly compressed to ensure a successful transfer. However this does not affect the final performance of the vias because the deformation caused by the transfer process is only presented near the un-densified roots of the CNT forest, which are removed in the subsequent planarization process. The location of the deformation agrees with a reported experiment performed on aligned CNT films [236]. A final finished via with metallic pads formed on the top is shown in figure 6.6 (f). This structure is ready for the possible succeeding processing, such
The I-V response of the fabricated vias was measured by four probe method. One such example of measurement results is shown in figure 6.7. The I-V curve is highly linear, indicating the establishment of good ohmic contacts on both ends of the CNTs. The resistance of the vias, 100 μm in diameter and 195 μm deep is $2.7 \pm 0.5 \, \Omega$. Taking account of the effective area occupied by CNTs in the vias, the resistivity of the densified CNT bundles is thus calculated be $3.9 \, \text{mΩ cm}$. Compared to the value from CNT forests directly grown in vias ($33.8 \, \text{mΩ cm}$, presented in next section), the resistivity is reduced by an order of magnitude. This reduction is a result of the densification process, which permits packing much more CNTs in the same footprint.

In addition to the reduction in resistance and processing temperature, this CNT-TSV technology based on densification and transfer also possesses advantages in other aspects. The post-growth transfer strategy brings much freedom in adjusting the growth process and introducing possible post-growth modification processing. For instance, it is not necessary to limit the CNT growth temperature to be compatible with devices, while low temperature normally leads to low quality of CNTs. And post-growth treatment such as high temperature annealing can be introduced into our process flow to improve the quality of CNTs, which is not possible for CNTs directly grown in the vias. This transfer approach also eliminates the necessity of developing different conductive barrier layers under the catalyst layer and modifying the growth process for vias with different materials on the bottom.
6.5 Interconnecting CNT TSVs

Schemes of interconnection

In this section, an easy-to-implement scheme for interconnecting CNT-based TSVs in stacked structures for 3D integration is demonstrated. There are two scenarios in interconnecting TSVs, namely connecting one TSV to another and connecting a TSV to a metal pad or line, both of which are addressed in this work.

This process flow is shown in figure 6.8. The vias were etched in Si by a standard DRIE process. The CNT forests were directly grown by the LP-TCVD process introduced in Section 3.3 (figure 6.8 (a)). Two chips with these CNT TSVs were then bonded by an adhesive at the center of the chips so that the CNT forests were compressed toward each other and directly contacted (figure 6.8 (b)). In another route, a chip with CNT TSVs was bonded to a chip coated with a Ti/Au layer by the same method (figure 6.8 (c)). The CNT forests in this case were compressed against the Au layer and direct CNT-to-Au contacts were made.

Because the CNT forests were in deep vias, after bonding they were mechanically fastened and reliable contacts were made. While macroscale direct CNT-to-CNT and carbon nanofiber (CNF)-to-CNF contacts for both electrical and mechanical connections have already been reported [232, 237], such contacts on a microscale are realized for the first time in the present work.

For the three fabricated structures of figure 6.8 (a-c), three different test con-
configurations were made as shown in figure 6.8 (d-f). These structures were made for measuring the resistances of the interconnected CNT TSVs. The first configuration (figure 6.8 (d)) was made from samples on which the length of the CNT forests was controlled to be equal to the depth of the vias during the growth. A Ti/Au layer was subsequently sputtered onto the chip and the Si was dry etched from the back side to expose the bottom of the vias. A similar process was applied to make configuration 2 (figure 6.8 (e)). Configuration 3 was simply made from the structure shown in figure 6.8 (c) with the top Si part etched (figure 6.8 (f)).

Results

Some SEM images of the fabricated structures are displayed in figure 6.9. The CNTs in figure 6.9 (a-c) show a well-aligned and uniform growth. To reveal the hidden CNT-to-CNT and CNT-to-Au contact interfaces, the top chips in the structures shown in figure 6.9 (b) and (c) were dry etched away before the SEM observation. Figure 6.9 (d-f) displays the CNT forests stacked onto another layer of forests. Figure 6.9 (g-i) presents the CNT forests assembled onto an Au surface. It can be clearly observed that tight CNT-to-CNT and CNT-to-Au contacts are obtained. Because the lengths of the extended parts of the CNT forests were intentionally controlled to overcome the thickness of the adhesive film for reliable contacts, the CNT forests are slightly deformed at their roots.

The via resistances were then measured by two probe method. The major part of this work used vias 100 µm in diameter and 132 µm deep. For such vias, the resistances for one via (as in configuration 1), two stacked vias (as in configuration 2), and one via on Au (as in configuration 3) are (16.1 ± 2.2), (46.0 ± 12.4), and (25.6 ± 4.5) Ω, respectively. Examples of I-V curves from each configuration are shown in figure 6.10. The relatively good linearity of these curves indicates that ohmic contacts are established in all three cases.

Extraction of contact resistances

The total resistance of one via or two stacked vias in configurations 1 and 2 can be expressed as:

$$R_{total} = R_{CNT-probe} + nR_{bulk} + (n - 1)R_{CNT-CNT} + R_{CNT-back}.$$  (6.8)

where $R_{CNT-probe}$ is the contact resistance between the CNT forest and the top probe, $R_{bulk}$ is the bulk resistance of the CNT forest, $R_{CNT-CNT}$ is the contact resistance between two stacked CNT forests, $R_{CNT-back}$ is the back side contact resistance between the CNT forest and the conductive substrate holder connected
Figure 6.9: SEM images of (a-c) CNT forests grown from the bottom of deep vias in Si; (d-f) CNT forests stacked onto each other as in configuration 2, with the top Si chip dry etched away to reveal the CNT/CNT interfaces; (g-i) CNT forests pressed to Au as in configuration 3, with the Si chip dry etched away to reveal the CNT/Au interface. The quarter circular parts in (d) and (g) are adhesives.
Figure 6.10: I-V curves from electrical measurements of one via as in configuration 1 (circles), two stacked vias as in configuration 2 (diamonds), and one via on Au as in configuration 3 (squares).

To another probe, and $n$ stands for the number of stacked layers, one in configuration 1 and two in configuration 2.

To extract the resistance components in equation 6.8, samples in configuration 1 of three different thicknesses were fabricated and measured. Using TLM [233], the total contact resistance in the measurement setup, including $R_{CNT-probe}$ and $R_{CNT-back}$, is estimated to be $9.8 \Omega$, as shown in figure 6.11. From this curve, the resistance of the bulk CNT forests 180 µm long used in the stacking experiments to make configuration 2 and 3 samples can also be calculated to be about $9.1 \Omega$. This measurement also gives a resistivity of $33.8 \text{ m}\Omega \text{ cm}$ for the CNT forests. Inserting the extracted contact and bulk resistances into equation 6.8 for configuration 2, the direct contact resistance between two CNT forests is extracted to be $18.0 \Omega$, about twice the CNT forest bulk resistance. This result partly supports a reported observation that the electrical resistances of CNT networks are dominated by the junction resistances between CNTs [238]. From the CNT-to-CNT contact resistance and the measured diameter of the CNT forests, the specific contact resistance between two VA-CNT forests is calculated to be approximately $1.2 \times 10^{-3} \Omega \text{ cm}^2$.

While it is not possible to separate $R_{CNT-probe}$ from $R_{CNT-back}$ in the measurements, it is difficult to extract the CNT-to-Au contact resistance (denoted as $R_{CNT-Au}$ in the following text) in configuration 3, because the measured total re-
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Figure 6.11: Extraction of the resistances of contacts and bulk CNT forests from measurements on samples in configuration 1 of different thicknesses. The total contact resistance is where the dashed line intercepts the y-axis.

The resistance in this case is a sum of $R_{\text{CNT-probe}}$, $R_{\text{bulk}}$, and $R_{\text{CNT-Au}}$, and the negligible resistance of the Au layer and from it to the probe. However, a rough estimation of $R_{\text{CNT-Au}}$ can be made if $R_{\text{CNT-back}}$ is assumed to be close to zero. This assumption is indeed reasonable based on the measurement in Section 6.3 and the very small contact resistance between VA-CNT forests and Ti reported in another study [217]. Then $R_{\text{CNT-Au}}$ can be roughly estimated to be 6.7 Ω, which gives a specific contact resistance of $4.5 \times 10^{-4}$ Ω cm$^2$ between the vertically aligned CNT forest and the Au surface. The result that $R_{\text{CNT-Au}}$ is smaller than $R_{\text{CNT-CNT}}$ may be due to the bigger contact area between a CNT forest and a flat Au surface compared to that between two rough CNT forests. In the CNT-to-Au case, it could be expected that some large contacts exist between the sidewalls of the CNTs and the Au surface, because the CNTs were slightly deformed and pressed onto the Au surface during the assembly process. On the other hand, CNT-to-CNT joints are dominated by point-to-point contacts between CNTs.

6.6 Summary of CNT-TSV development

In this chapter I have summarized the experimental development of CNT-TSVs within the framework of this thesis project. Through developing the basic process in the first work, carried out in an early stage of this thesis project and described
in Section 6.3, the feasibility of using CNTs as the filling material of TSVs is clearly demonstrated. Valuable knowledge on growing VA-CNTs in deep vias and planarization of these structures are also gained. Furthermore, this initial work indicates the limitations of using as-grown VA-CNTs in real applications, including the high growth temperature and low volume fraction of the grown VA-CNT forests.

This finding triggered the development of a more sophisticated approach (reported in Section 6.4), which integrates a few basic processes, also developed as a part of this thesis. The two key techniques, densification and transfer of VA-CNT structures (reported in Chapter 5 and 4 respectively), successfully improve the performance and process compatibility of the CNT-TSV technology.

The two demonstrations mentioned above both involve the planarization of CNTs. Hence in future applications, micro bumps need to be made to interconnect them, making this work belong to the route of 3D IC integration. At some later stage of the thesis project, I realized that planarization is not necessary in certain cases and skipping this step just makes interconnection of the vias easier. This work is introduced in Section 6.5. Because no bumping is needed to interconnect the CNT-TSVs, this scheme fits well into the 3D Si integration technology.

The measured bulk and contact resistances of CNT-TSVs in the present thesis are compatible with reported results for CNT forests or films, but they are still worse than those for Cu-filled vias. On the other hand, the results are competitive to an existing technology on the market using polysilicon as the via filling material [203]. Nevertheless, since the development of CNT-TSVs is still in its infancy there is still much room to improve the conductivity of the CNTs by a number of different measures, such as optimizing the growth [129], post-growth high temperature annealing [130, 131], and doping [239, 240].

Despite the higher resistances compared to metal-filled TSVs at this stage, the CNT TSVs have a number of attractive advantages. First, the technology shows good manufacturability. Filling TSVs with CNTs is easier and much faster than that with electroplating Cu. The growth of CNTs in TSVs in our work only took 1.5 to 3 min using the LP-TCVD process. In the case of post-growth transfer of CNTs into vias, the processing time is also quite short (~2 min). Deposition of the catalyst layer for CNT growth can be easily done by standard evaporation. On the other hand, high-quality electroplating of Cu in deep TSVs needs deposition of a continuously uniform seed layer. This process itself is a highly demanding and challenging task. Furthermore, the interconnection scheme shows great simplicity of implementation. The CNT TSVs can be easily interconnected by simple mechanical fastening with the extended parts of the CNT forests acting as bumps.

From the perspective of mechanical reliability, CNT TSVs may also be superior to Cu-filled ones. The low thermal expansion of CNTs will not introduce big stress and strain into the structure compared to the Cu vias, reducing the risks of
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mechanical failures such as cracking and delamination. Moreover, CNTs are thermally and chemically stable. While Cu-filled TSVs need good barrier layers on the sidewalls to prevent the diffusion of Cu and their electromigration is a serious concern [241], CNT TSV technology is much more tolerant in these aspects.
Chapter 7

Conclusions and outlook

This thesis explores and examines the possibilities and potential of integrating vertically-aligned carbon nanotubes into microsystems, from a perspective of packaging technology. The properties and growth processes of CNTs are reviewed and their potential applications in the field of packaging are introduced. Limitations of the as-grown VA-CNTs by chemical vapor deposition, which hinder their wide applications in packaging, are identified. These limitations include for example the high growth temperature and the low volume fraction of VA-CNT forests.

To solve some of these problems, experimental progresses in two major aspects of basic process development have been made. First, low temperature transfer processes have been developed to assemble VA-CNT structures onto target substrates at low temperatures, thus providing a solution to the problems of CNTs’ high temperature and selective growth. The processing temperature of the transfer methods is below 200 °C. Second, densification methods have been developed and investigated to increase the volume fraction of CNTs in their forests.

Regarding the applications of VA-CNTs in microsystem packaging, the focus in this thesis is on through-silicon via interconnects, a critical element in three-dimensional integration. A few different routes to fabricate and interconnect CNT-filled TSVs have been demonstrated, showing great potential of using CNTs in this application with good manufacturability and reliability.

At this stage, the electrical performance of CNT-TSVs is still far away from the theoretical expectations, but they may still be sufficient for certain applications. The gap between the experimental results and theoretical estimations on the one hand reveals the great potential of this technology. One the other hand, this gap reflects an often underestimated difficulty in nanotechnology research and development: how to extend the great properties of nanomaterials into applications at an engineering scale. In this context, it is the author’s hope that the basic methods developed in this thesis can contribute to the utilization of CNTs’ excellent properties in future highly integrated microsystems.
It is worthwhile to mention that the application of the methods developed in this thesis is not limited to the TSV interconnects. These methods can be used in a number of different packaging applications. For instance, the transfer methodology can be directly applied to assemble CNT-based thermal interface materials or cooling devices. The interconnection scheme demonstrated on CNT-TSVs may easily be adapted to connect CNT flip chip bumps.

Furthermore, these methods can find applications in a much wider range and are not limited to microsystem packaging. For example, the transfer process can be used to assemble VA-CNTs as sensors or electrodes into microfluidic devices, very often made of temperature-sensitive polymeric materials. The densification methods can help to create various dual-porosity and high aspect ratio 3D structures. And they can also be used for other aligned nanotube or nanowire structures rather than those of CNTs.

From the microfabrication point of view, VA-CNTs are a unique material to link thin film and thick film technologies. In a few minutes, a thin film of catalyst with a thickness of a few nanometers can be transformed to a thick film of VA-CNTs hundreds of micrometers to a few millimeters thick. This opens various possibilities for using VA-CNTs as basic building blocks in future microsystems, for example, as moving parts [242–244] or as contacts [245] in microelectromechanical systems, or even as sacrificial layers in fabrication processes [246]. The post-growth processes developed in this thesis offer a capability to modify the VA-CNT structures in a variety of ways, and may thus assist in the future efficient integration of VA-CNTs into microsystems.

The continuation of the CNT-TSV work can be diversified into two different directions. The first direction will concentrate on making this technology deliver high performance and reliability in 3D stacked packages to meet the requirements of high-end applications. Improvement can be achieved by shrinking the dimensions and promoting the conductivity of CNTs. Reliability tests and failure analysis are also needed. In the other direction, efforts can be made to modify and optimize this technology for applications with special needs, e.g. flexible electronics or high temperature devices.
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Bibliography


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