Thesis for the Degree of Doctor of Philosophy

Efficient and Wideband Power Amplifiers for Wireless Communications

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November, 2012
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Doktorsavhandlingar vid Chalmers tekniska högskola
Ny serie nr 3430
ISSN 0346-718X

Technical report MC2-236
ISSN 1652-0769

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Printed by Chalmers Reproservice
Göteborg, Sweden, November, 2012
To My Beloved Family
Abstract

The rapid evolution of wireless communication systems and the development of new standards require that wireless transmitters process several types of standards across multiple bands. Power amplifiers (PAs) are key components in wireless transmitters because they have a big impact on the overall system performance in terms of their bandwidth, efficiency, and linearity. This thesis presents various design techniques that improve bandwidth and efficiency characteristics of the PA.

For narrowband transmitters, a circuit design methodology that enables first-pass design of high efficiency single-ended PAs is presented. The method, based on employing bare-die transistors, specialized modeling technique, and optimization of harmonic impedances, is validated with excellent experimental results. A class-F\(^{-1}\) PA at 3.5 GHz and a harmonically tuned PA at 5.5 GHz are designed and implemented demonstrating 78\% and 70\% PAE respectively.

For broadband transmitters, a design methodology for single-ended PAs with octave bandwidth is presented and verified. The method is based on a harmonic tuning approach combined with a systematic design of broadband matching networks. The demonstrator PA achieves 50-63\% PAE across 1.9-4.3 GHz. Then, extending the bandwidth beyond one octave while maintaining high efficiency is investigated by adopting a push-pull configuration. For this reason, a novel push-pull harmonic load-pull measurement setup is proposed and a push-pull PA operating between 1-3 GHz is designed and implemented. The investigation demonstrates the proposed setup as an important tool for understanding and optimizing PAs and baluns for wideband push-pull microwave PAs.

For multi-band transmitters, using signals with large peak-to-average ratio, the design of dual-band Doherty PAs (DPAs) is considered. A detailed analysis of each passive structure constituting the DPA is given, leading to different configurations to implement dual-band DPAs. One of the configurations is implemented, leading to state-of-the-art results for dual-band DPAs. Finally, the multi-band branch-line coupler (BLC) is a key component for also extending the design of DPAs to multi-band in the future. A closed form design approach for multi-band BLCs operating at arbitrary frequencies is presented and validated by the successful design of dual-band, triple-band, and quad-band BLCs.

The excellent results obtained demonstrate the success of the developed design methodologies for high efficiency and multi-band/wideband PAs. These methods will contribute to the design of future wireless systems with improved performance in terms of efficiency, bandwidth and hence cost.

**Keywords:** Branch-line coupler, Doherty power amplifier, GaN-HEMT, high efficiency, multi-band, power amplifier, wideband.
List of Publications

Appended papers

This thesis is based on the following papers:


Other papers and publications

The following papers and publications are not appended to the thesis, either due to contents overlapping that of appended papers, or due to contents not related to the thesis.


[g] Paul Saad, Hossein Mashad Nemati, Mattias Thorsell, Kristoffer Andersson, and Christian Fager "Design of High Efficiency Power Amplifiers using a Bare-die Approach," in 2nd Workshop on Future Microwave Products, University of Gävle, October, 2009.


[j] Paul Saad, Roman Merz, Cyril Botteron, and Pierre Andre Farine "Performance comparison of UWB impulse-based multiple access schemes in
# Notations and abbreviations

## Notations

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C$</td>
<td>Capacitance</td>
</tr>
<tr>
<td>$f$</td>
<td>Frequency</td>
</tr>
<tr>
<td>$f_0$</td>
<td>Center frequency or fundamental frequency</td>
</tr>
<tr>
<td>$I$</td>
<td>Current</td>
</tr>
<tr>
<td>$I_A$</td>
<td>Current level of the auxiliary amplifier</td>
</tr>
<tr>
<td>$I_{dc}$</td>
<td>Drain bias current</td>
</tr>
<tr>
<td>$I_{di}$</td>
<td>Intrinsic drain-to-source current</td>
</tr>
<tr>
<td>$I_{ds}$</td>
<td>Drain-to-source current</td>
</tr>
<tr>
<td>$I_M$</td>
<td>Current level of the main amplifier</td>
</tr>
<tr>
<td>$I_{max}$</td>
<td>Maximum current</td>
</tr>
<tr>
<td>$L$</td>
<td>Inductance</td>
</tr>
<tr>
<td>$L_{bgw}$</td>
<td>Inductance of bondwires at gate side</td>
</tr>
<tr>
<td>$L_{bdw}$</td>
<td>Inductance of bondwires at drain side</td>
</tr>
<tr>
<td>$P_{in}$</td>
<td>Input power</td>
</tr>
<tr>
<td>$P_{out}$</td>
<td>Output power</td>
</tr>
<tr>
<td>$P_{out,avg}$</td>
<td>Average output power</td>
</tr>
<tr>
<td>$P_{1-dB}$</td>
<td>1-dB compression point</td>
</tr>
<tr>
<td>$Q$</td>
<td>Q-factor</td>
</tr>
<tr>
<td>$R$</td>
<td>Resistance</td>
</tr>
<tr>
<td>$R_L$</td>
<td>Load resistance</td>
</tr>
<tr>
<td>$S$-parameters</td>
<td>Scattering-parameters</td>
</tr>
<tr>
<td>$V$</td>
<td>Voltage</td>
</tr>
<tr>
<td>$V_{br}$</td>
<td>Breakdown voltage</td>
</tr>
<tr>
<td>$V_{DC}$</td>
<td>DC supply voltage</td>
</tr>
<tr>
<td>$V_{di}$</td>
<td>Intrinsic drain-to-source voltage</td>
</tr>
<tr>
<td>$V_{ds}$</td>
<td>Drain-to-source voltage</td>
</tr>
<tr>
<td>$Y_C$</td>
<td>Common mode conductance</td>
</tr>
<tr>
<td>$Z_A$</td>
<td>Load seen by the auxiliary amplifier</td>
</tr>
<tr>
<td>$Z_D$</td>
<td>Differential mode impedance</td>
</tr>
<tr>
<td>$Z_M$</td>
<td>Load seen by the main amplifier</td>
</tr>
<tr>
<td>$Z_L$</td>
<td>Load impedance</td>
</tr>
</tbody>
</table>
Angular frequency
Dielectric constant
Drain efficiency
Infinity
Wavelength
Reflection coefficient
Electrical length
Conduction angle

Abbreviations

ACLR Adjacent channel leakage ratio
AM Amplitude modulation
BJT Bipolar-Junction Transistor
BLC Branch line coupler
CAD Computer-aided design
CN Common node
CO₂ Carbon dioxide
CW Continuous wave
CRLH Composite Right/Left Handed
EB Exabyte
EER Envelope elimination and restoration
EM Electromagnetic
ET Envelope tracking
DC Direct current
DPA Doherty power amplifier
DPD Digital predistortion
EER Envelope elimination and restoration
ET Envelope tracking
FET Field Effect Transistor
GaN Gallium Nitride
GaAs Gallium Arsenide
GSM Global system for mobile
HT Harmonically tuned
HEMT High Electron Mobility Transistor
ICT Information and Communication Technologies
IIN Impedance inverter network
IPS Input power splitter
ITN Impedance transformer network
LTE Long term evolution
MC Monte-Carlo
MMIC Microwave monolithic integrated circuits
OBO Output back-off
OFDM Orthogonal frequency-division multiplexing
PA Power Amplifier
<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Term</th>
</tr>
</thead>
<tbody>
<tr>
<td>PAE</td>
<td>Power-added efficiency</td>
</tr>
<tr>
<td>PAPR</td>
<td>Peak-to-average power ratio</td>
</tr>
<tr>
<td>PCB</td>
<td>Printed circuit board</td>
</tr>
<tr>
<td>PCN</td>
<td>Phase compensation network</td>
</tr>
<tr>
<td>PM</td>
<td>Phase modulation</td>
</tr>
<tr>
<td>Q</td>
<td>Quality factor</td>
</tr>
<tr>
<td>QAM</td>
<td>Quadrature amplitude modulation</td>
</tr>
<tr>
<td>RBS</td>
<td>Radio base station</td>
</tr>
<tr>
<td>RF</td>
<td>Radio Frequency</td>
</tr>
<tr>
<td>Si</td>
<td>Silicon</td>
</tr>
<tr>
<td>SMPA</td>
<td>Switched mode power amplifier</td>
</tr>
<tr>
<td>TL</td>
<td>Transmission Line</td>
</tr>
<tr>
<td>TWA</td>
<td>Traveling Wave Amplifier</td>
</tr>
<tr>
<td>UMTS</td>
<td>Universal mobile telecommunications system</td>
</tr>
<tr>
<td>Vs</td>
<td>Versus</td>
</tr>
<tr>
<td>WCDMA</td>
<td>Wideband code division multiple access</td>
</tr>
<tr>
<td>WiFi</td>
<td>Wireless fidelity</td>
</tr>
<tr>
<td>WiMAX</td>
<td>Worldwide interoperability for microwave access</td>
</tr>
<tr>
<td>4G</td>
<td>The fourth generation of cellular wireless standards</td>
</tr>
</tbody>
</table>
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Chapter 1

Introduction

1.1 Motivation

Mobile and wireless communications systems have revolutionized our daily life and business. We are observing a rapid growth in these technologies where mobile and wireless communications have become so important in our society and indispensable for our daily lives. Consequently, due the increasing growth of user subscribers and the emergence of new technologies in the mobile communication systems, the data traffic is estimated to increase to $10.8 \text{EB}$ per month by 2016 [1]. As shown in Fig. 1.1, this corresponds to an 18-fold increase over 2011. To handle growing mobile data traffic requirements, mobile network operators have begun to introduce small cells into their networks in order to keep up with demand. This will further increase the number of radio base stations (RBSs) installed and hence, results in increased energy consumption caused by the Information and Communication Technologies (ICT).

![Mobile data traffic forecast, 2011 to 2016](image)

**Fig. 1.1:** Global Mobile Data Traffic forecast, 2011 to 2016 [1].

$1 \text{ Exabyte} = 1.048576 \cdot 10^6 \text{ Terabytes} = 1.1529215 \cdot 10^{18} \text{ Bytes}$
The RBS consumes power in order to transmit RF signals and to process the incoming signals from subscriber cell phones. The total efficiency of the RBS, which is usually very low, is calculated as the ratio of the total RF output power to the total consumed power. The RBSs are the main contributor to the energy consumption of the wireless infrastructure and are therefore, the highest contributors of CO₂ emissions in mobile networks [2]. To reduce the CO₂ emission, the energy consumption of the RBS has to be minimized and hence its efficiency should be maximized. The energy per function distribution of a RBS blocks presented in [3], shows that RF power amplifiers (PAs) are the most energy-consuming blocks of RBSs and therefore their energy efficiency have a high impact on the total energy consumption of RBSs. Increasing the energy efficiency of PAs does not only reduce the total energy consumption and the CO₂ emission. It also affects other critical parameters of wireless systems such as weight and reliability. Higher efficiency means that less power is dissipated and less heat removal is needed which directly translates to the weight, the volume, and the cost of the RBS.

In addition to the efficiency issue, and as shown in Fig. 1.2, the number of mobile radio standards (GSM, UMTS, WiFi, 4G LTE, WiMAX, etc.) and frequency bands (0.9, 1.8 GHz, 2.1 GHz, 2.4 GHz, 0.8, 1.9, 2.6 GHz, 3.5 GHz, etc.) have increased and therefore, the demand for multiband/multistandard capable RBSs arise in order to reduce system manufacturers product diversity and to support the flexibility of mobile operators. This makes multiband/wideband PAs that cover many frequency bands while maintaining high efficiency an important and hot research topic.

Usually, the design of PAs is the result of trade-offs, trying to accomplish several conflicting requirements such as efficiency vs. linearity and efficiency vs. bandwidth. These conflicting requirements are addressed in the following.

1.2 Efficiency versus linearity

A typical output power versus input power characteristic of a PA is shown in Fig. 1.3(a) while a typical output power probability density function of a modulated mobile communication signal and the power-added-efficiency (PAE) of a PA are shown versus output power in Fig. 1.3(b). As the input power increases (Fig. 1.3(a)), the output power increases until it reaches saturation where it does not increase any further (compression). The PA is usually driven so that the peaks of the input signal reaches the beginning of the saturation region where the output power has dropped by 1-dB compared to an ideal linear behavior (the so-called 1 dB compression point). This typically occurs close to the point where the efficiency is maximized [4].
1.2 EFFICIENCY VERSUS LINEARITY

![Diagram](image)

**Fig. 1.3:** (a) Output power versus input power of an ideal and a real power amplifier (b) efficiency and typical probability density function of a mobile communication signal versus output power backoff.

In earlier communication systems, like Global System for Mobile (GSM), the communication signal has a constant amplitude. This allows the PA to be operated in compression and hence in high efficiency. In contrast, modern wireless communication systems employ modulation schemes such as Orthogonal Frequency-Division Multiplexing (OFDM) and Quadrature amplitude modulation (QAM) in order to maximize the spectral efficiency [4]. These modulation schemes result in signals with large amplitude variations and peak-to-average power ratios (PAPRs) in the range of 6-12 dB [5,6]. In order to prevent clipping of the signal peaks and thereby strong distortion of the signal, these signals requires the PA to operate at an average output power far below the saturation region and hence, at low efficiency levels as illustrated in Fig. 1.3(b).

Different high efficiency architectures have been proposed to increase the average efficiency of PAs defined as the ratio between average output power and average supplied DC power [7]. Envelope elimination and restoration (EER) [8], envelope tracking (ET) [9], Doherty amplifiers [10] and varactor based dynamic load modulation [11] are the most common. In EER and ET, the supply voltage of the power amplifier is designed to track the instantaneous envelope of the modulated signal. Hence, it operates in saturation and recovers its peak efficiency for a wider range of output power levels [8,9]. In Doherty amplifiers and varactor based load modulation transmitters, high average efficiency is achieved by dynamically adapting the PA load impedance to keep the amplifier in compression during modulation [4,10,12,13].

The average efficiency of the PA is scaled by the PA peak efficiency and hence, the average efficiency is limited by the peak efficiency of the PA. Therefore, the peak efficiency has a direct implication on the average efficiency when the PA is used in a high efficiency architecture, e.g. ET or EER. In such architectures, the PA is kept in saturation for a large output power dynamic range. Our main goal in this thesis is to investigate methods for improvement of PA peak and average efficiencies.
1.3 Efficiency versus bandwidth

As discussed earlier, efficient wideband PAs are highly demanded for modern and future communication systems. Usually, high efficiency PAs operate over narrow bandwidth, since for a given device technology, the bandwidth of the PA decreases as the efficiency increases. The basic limitations in designing efficient and wideband amplifiers are associated with the device technology used.

The output impedance of the device is usually characterized by a complex impedance, i.e. shunt $R - C$ circuit. In [14], it is demonstrated that the bandwidth over which a good match of a complex load can be obtained is limited by the $RC$ product. If the impedance at the interface of the transistor (die) is very low, then the quality factor ($Q$) value of the transformation, between a low impedance at the transistor to a 50 Ω load, is high and consequently decreases the useful bandwidth. Hence, it is of great importance to have devices with high output impedance to facilitate the matching and to obtain wider bandwidth. In the following, a comparison of the different devices used for RF PA stages is given.

1.3.1 Comparison of different devices characteristics

Different types of RF solid state transistors are used in the design of PAs. These transistors can be divided in two main groups, the Field Effect Transistors (FETs) and the Bipolar-Junction Transistors (BJTs) [15]. Usually, these devices are fabricated from Silicon (Si) or from III-V compound semiconductors like Gallium Arsenide (GaAs) and the recently developed wide band gap semiconductor Gallium Nitride (GaN). Table 4.5 shows a comparison of some performance metrics of Si, GaAs, and GaN.

<table>
<thead>
<tr>
<th>Properties</th>
<th>Si</th>
<th>GaAs</th>
<th>GaN</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bandgap (eV)</td>
<td>1.12</td>
<td>1.42</td>
<td>3.20</td>
</tr>
<tr>
<td>Breakdown Field (10^5V/cm)</td>
<td>3.80</td>
<td>4.20</td>
<td>50.00</td>
</tr>
<tr>
<td>Saturated Velocity (10^7cm/sec)</td>
<td>0.70</td>
<td>2.00</td>
<td>1.80</td>
</tr>
<tr>
<td>Electron Mobility (cm^2/V·sec)</td>
<td>1500</td>
<td>8500</td>
<td>2000</td>
</tr>
<tr>
<td>Thermal conductivity (W/cm·°C)</td>
<td>1.40</td>
<td>0.45</td>
<td>1.70</td>
</tr>
</tbody>
</table>

A wider bandgap semiconductor means supporting higher internal electric fields before the dielectric breakdown occurs. Consequently, the device will be able to allow higher output voltage swings and thus, attain higher output power levels. The wide bandgap of GaN semiconductors offers the potential to fabricate RF devices with an order of magnitude improved RF output power compared to traditional devices based on Si and GaAs [16]. The improved RF output power is made possible due to the unique material properties of the GaN semiconductor presented in Table 4.5. The electron mobility mainly determine
1.4. THESIS CONTRIBUTIONS

This thesis addresses the performance improvement of RF PAs used in wireless transmitters. In particular, the thesis concentrates on enhancing the efficiency of the PA, on operating the PA simultaneously in different bands, and on widening its operating frequency bandwidth.

Regardless of the well established PA theory [4,13], the real implementation of efficient PAs is often based on experience of the designer, where tuning of the fabricated PA is used to achieve the same performance predicted by Computer-aided design (CAD) simulations. To enable first-pass design and to improve the peak efficiency of the single-band PAs, a complete systematic design procedure is proposed. The procedure includes a bare-die mounting technique, dedicated transistor modeling technique, and circuit design methodology. The latter includes comprehensive source-pull/load-pull simulations at fundamental and harmonics, Monte-Carlo (MC) simulations that study the impact of the components variability on the PA performance, and Electromagnetic (EM) simulations that enable accurate synthesis of the matching networks. This procedure has allowed us to implement first-pass designs having excellent performance. We demonstrated the success of this procedure at S-band in [Paper A], and at C-band in [Paper B].

Having this procedure as a basis, we have tried to widen the frequency operation bandwidth of the PA while maintaining high efficiency. The high-efficiency wideband PAs reported in the literature generally have a bandwidth of less than one octave [18–21]. Moreover, they rarely present any general method or analytical derivation for the design of the wideband matching networks used. In this thesis, a design procedure based on a source pull/load pull simulation approach together with an extensively detailed method for the design of suitable broadband matching network solutions. In [Paper C], we demonstrate the success of the proposed approach by the design and implementation of an octave bandwidth PA.

Increasing the bandwidth to more than one octave while maintaining high efficiency was investigated by adopting a push-pull configuration. Even though the bandwidth potential of the push-pull configuration has been demonstrated...
[22], there is no possibility to investigate or verify the true operation and interaction between PA and balun. In [Paper D], we propose a novel push-pull harmonic load-pull measurement setup able to emulate the balun operation, at the output of a push-pull PA, while setting any fundamental and second harmonic loading conditions. By using the proposed measurement setup, together with a push-pull PA prototype, we demonstrate the importance of the even mode second harmonic response of the output balun for the design of wideband push-pull microwave PAs.

To increase the average efficiency, the efficiency in back-off must increase. Therefore, the design of the DPA has been considered in the thesis. So far, lot of work has been done on DPAs [12, 23–32]. However, most of the published DPAs were designed to work in a single-band and therefore they do not satisfy the multi-band, multi-standard requirements of the modern RBSs. Recently, there have been some efforts to optimize a DPA for dual-band operation. The first prototype of dual-band DPA reported in [33] was working only in the first band. Two working dual-band DPAs are presented in [34,35]. However, there is no general theoretical analysis presented and the achieved performance is quiet modest. In [Paper E], a dual-band single-ended PA is firstly designed to serve as Main PA for the Doherty PA. In [Paper G], a detailed design methodology, based on comprehensive design of the passive structures, for dual-band is presented and validated by successfully state-of-the-art experimental results.

To develop multi-band DPAs in the future, multi-band BLCs are needed. Solutions to design BLCs having more than two operating bands can be found in [36–39]. However, the methods proposed in [36–38] are not assisted with a full theoretical analysis that demonstrates the possibility to extend them for an arbitrary number of operating frequencies. Moreover, the approach presented in [39] is limited to commensurate frequencies. In this thesis, a design approach for multi-band BLCs for arbitrary operating frequencies is presented. The complete theoretical analysis of the topology is derived in [paper F], leading to a closed form system of equations for its design. Three couplers based on the proposed structure are implemented for dual-, triple-, and quad-band operation to validate the methodology.

1.5 Thesis outline

This thesis focuses on the design of highly efficient single-band, dual-band, and wideband PAs using GaN-HEMT devices. Chapter 2 reviews some of the most typical classes of PAs and presents the design and implementation of an inverse class-F PA and a harmonically tuned PA with high peak efficiency. Chapter 3 focuses on design techniques developed to design highly efficient and wideband single-ended PAs. Moreover, a comprehensive investigation on the interaction between push-pull PAs and baluns for broadband microwave applications is also presented. In Chapter 4, design approaches for dual-band DPAs and multi-band BLCs are presented and experimentally validated. Chapter 5 concludes by summarizing the main points discussed in the different chapters, followed by some suggestions for future research directions. In Chapter 6, a short introduction of appended papers is given and the contributions of the author are specified.
Chapter 2

Efficient single-band saturated power amplifiers

As already discussed in Chapter 1, high efficiency saturated PAs are important components to obtain small, and low cost transmitters for wireless communications systems. To date, lot of effort has been put to obtain the highest possible efficiency values in a PA. Therefore, several classes, e.g. class-D, -E, -F, -F\(^{-1}\), -J, have been proposed [4, 25]. In these classes, the transistor current and voltage waveforms are tailored by specific load network designs to prevent an overlap between them, thus minimizing power dissipation and ensuring the highest efficiency level.

This chapter focuses on the design of PAs used in high efficiency architecture where the PA is kept in saturation for a large output power dynamic range. In the following, an overview of PA operation classes is given and a design procedure for first-pass design of high efficiency saturated PAs is presented. The design procedure consists of using a bare-die technique, an optimized transistor model, and a methodology to locate the fundamental and harmonic impedances. The success of the presented procedure is demonstrated by the design of an inverse class-F GaN-HEMT PA at 3.5 GHz and a harmonically tuned PA at 5.5 GHz.

2.1 Idealized power amplifier classes

PAs can (in general) be classified into two main categories: Transconductance amplifiers and switched mode power amplifiers (SMPAs). The transconductance amplifiers are traditionally categorized into class-A, class-AB, class-B, and class-C amplifiers. The classification of the transconductance amplifiers depends on the quiescent bias point of the active device or, equivalently, on the device current conduction angle. In SMPAs, where the device is operated like a switch rather than a current source, the classification is related to the active device dynamic operating conditions (e.g. class-E) or to the matching network terminating conditions (e.g. class-F) [4, 25].

The mentioned classes above, except for class-A, require termination for all harmonics of the input signal. This becomes difficult when the operating frequency range is moved towards the microwave region [25]. Therefore, in
practice, only the fundamental and first few harmonics (second and third or just second) can be controlled. Consequently, class-J amplifier has been proposed in [4]. It provides same efficiency and linearity as Class-B amplifiers by controlling only the fundamental and second harmonic while the higher order harmonics are assumed to be short-circuited by the output capacitance of the device.

2.1.1 Traditional transconductance amplifiers

Class-A, Class-AB, Class-B, and Class-C amplifiers, known as transconductance amplifiers, use active transistors as voltage controlled current sources [4, 40–42]. Fig. 2.1(a) shows a simplified circuit topology of these amplifiers consisting of a transistor, RF choke \( L_{RF} \), DC blocking capacitor, and a bandpass filter to short circuit the out of band tones. This parallel resonator configuration also ensures a sinusoidal voltage waveform across the transistor.

![Circuit topology](image)

**Fig. 2.1:** Transconductance amplifiers (a) Circuit topology (b) Voltage and current waveforms.

These four types of PAs are distinguished by the device conduction angle, i.e., the portion of \( 2\pi \) rad over which a current is flowing through the transistor. Voltage and current waveforms for different classes are shown in Fig. 2.1(b). The class-A amplifier has a conduction angle of \( \Theta = 2\pi \) rad. It has in practice the highest linearity but the lowest peak efficiency (50%) over the other classes. The class-B amplifier operates ideally at zero quiescent current so the transistor will be conducting for a half cycle (\( \Theta = \pi \) rad). Therefore, its theoretical efficiency (78%) is higher than that of the class-A amplifier. The class-AB amplifier is a compromise (\( \pi < \Theta < 2\pi \) rad) between class A and class B in terms of efficiency and therefore often employed in traditional transmitter implementations such as RBSs. The transistor is biased slightly above pinch-off, typically at 10% to 15% of the drain saturation current. In this case, the transistor will be conducting for more than a half cycle, but less than a full cycle of the input signal. The Class-C amplifier can achieve an ideal efficiency of 100% when the conduction angle is reduced to zero. However, there are several drawbacks in this class of operation at microwave frequencies. The first drawback is that the gain and the
output power approaches zero, as the efficiency approaches 100%. The second drawback is that the amplifier is highly nonlinear, so it has to be used with linearization techniques.

### 2.1.2 Switched mode power amplifiers

In contrast to the transconductance amplifiers, where the device is operating as a current source, SMPAs are based on the notion that the transistor is operating as a switch. In the on-state, while the device acts as a short circuit and the current flows through it, the voltage across it should be zero. In the off-state, the device acts as an open circuit and no current flows through it. Therefore, ideally, in both states there is no power dissipated in the device and hence 100% efficiency is theoretically achieved [43].

Unfortunately, in practical high frequency SMPAs the efficiency is degraded from 100% due to non-idealities of the components. Typical non-idealities are parasitic elements, finite on-resistance, non-zero transition time, and non-zero knee voltage [4, 44].

Inverse Class-F is very popular in microwave applications because the designer only need to control the fundamental and the second harmonic. Short circuiting the third harmonic may be obtained by the output capacitor of the device. A description of ideal inverse class-F is given hereafter.

#### 2.1.2.1 Ideal inverse class-F power amplifiers

Due to the active device physical limits for output current and voltage swings, the output current and voltage of a PA with large-signal drive are no longer purely sinusoidal but contains a large number of harmonics. The wave shaping of these harmonics leads to high power conversion efficiency [25] and hence Inverse-F PA definition. The structure of an inverse class-F PA is shown in Fig. 2.2(a) where filters are used to control the harmonic contents of the drain current and voltage. Fig. 2.2(b) shows the ideal voltage and current waveforms of the inverse class-F PAs. They have half-sinusoidal voltage and square-wave current signals. The ideal waveforms can be analyzed using Fourier series expansion, which gives expressions for voltage and current waveforms and their harmonics [4, 25]. The values of impedance terminations can be easily obtained by the ratio between respective Fourier voltage and current components.

In order to achieve 100% drain efficiency with ideal waveforms, the following impedance conditions should be met for inverse Class-F amplifiers:

\[
Z_L[f_0] = Z_{opt}, \quad (2.1)
\]

\[
Z_L[2nf_0]_{n>1} = \infty, \quad (2.2)
\]

\[
Z_L[2(n+1)f_0]_{n>1} = 0, \quad (2.3)
\]

where \(f_0\) is the fundamental frequency, \(n\) is the harmonic number, and \(Z_{opt}\) is the optimal load impedance at the fundamental frequency. It is important to note that class-F is a dual of the inverse class-F PA. Therefore, to obtain class-F operation, the harmonics impedance conditions, as well as the current and voltage waveforms, are interchanged.
2.1.3 Practical high frequency power amplifiers

In the previous section, the ideal impedance termination conditions for the different classes of operation are given. In practice, it is not possible to control all the harmonics and obtain ideal operation. Therefore, the so-called harmonically tuned and class-J PAs can be regarded as a practical solution for their implementation.

2.1.3.1 Harmonically tuned power amplifiers

In low frequency applications, a large number of harmonic terminations can be controlled. Hence, it is possible to achieve performances close to the ideal figures when the device has low knee voltage $V_k$ and/or high breakdown voltage $V_{BR}$. However, this is not the case for high frequency applications (microwave region and beyond), where the performance is degraded compared to the theoretical ones. The main reason for this degradation is the limited number of harmonics that can be controlled in practice. As the frequency increases, the control of higher order harmonics becomes very difficult, because the output capacitance of the device short-circuit higher frequency components, therefore not allowing the desired wave-shaping. According to [45, 46], controlling the second, $2f_0$, and the third, $3f_0$, harmonics is usually enough for practical applications. Trying to control more harmonics will increase the complexity of the circuit without improving the performance considerably [47].

As an example, when designing a practical inverse class-F PA, typically the fundamental and one or two harmonics are only controlled. However, this opens up the question if this still corresponds to an inverse-F operation or to another operation mode. In this case, studying the intrinsic drain current and voltage waveforms can be very helpful to determine the mode of operation of the PA. Therefore, a device model that allow the intrinsic waveforms to be inspected during simulations is highly desirable.

2.1.3.2 Class-J power amplifiers

A new class of operation named as Class-J was introduced recently by Cripps [4]. Class-J became popular due to its high performance in terms of efficiency and
2.2 Design procedure for high efficiency power amplifiers

The proposed design procedure for high efficiency PAs includes a bare-die mounting technique, an accurate nonlinear transistor model that allows reliable simulations, and a circuit design methodology. This latter involves comprehensive fundamental and harmonic source-/load-pull simulations. Moreover, EM and MC simulations are finally used to allow accurate simulations and ensure first-pass design.

2.2.1 Bare-die mounting technique

Two of the most important transistor parasitics, the lead inductances and tab capacitances ($L_1$ and $C_1$ in Fig. 2.3(a)) associated with transistor packages have in our work been eliminated by using a transistor chip without any package (Fig. 2.3(b)). Using this approach, we reduce the extrinsic parasitics, and therefore facilitating a more wideband and less sensitive harmonic matching. The bare-die transistor chip is mounted to the PA fixture and connected directly to the printed circuit boards (PCBs) using wire bonding ($L_g$ and $L_d$ in Fig. 2.3). The thickness of the ridge where the transistor chip is mounted, is carefully adjusted to align the surface of the chip to the transmission lines.
(TLs). Hence, the distances between the TLs and the transistor chip are mini-
mized as shown in Fig. 2.4(a). The bond wires used are of gold, and as depicted 
in Fig. 2.4(b), we use at least three bond wires to connect the transistor chip 
to the TLs. An equivalent inductance in the range 0.15-0.2 nH is estimated on 
each side.

![Fig. 2.4: Bare-die transistor mounting technique: (a) Cross section view; (b) Top view.](image)

### 2.2.2 Transistor modeling for high efficiency power amplifiers

The determination of the optimum impedances of fundamental and harmon-
ics that maximize the efficiency can be obtained by either using a load-pull 
measurement setup [51–53] or a device model that can be used for performing 
load-pull in a circuit-simulator [49, 54, 55]. The use of a non-linear transistor 
model has many advantages over the load-pull measurement setup. It allows 
the investigation of the drain voltage and current intrinsic waveforms 
and therefore the PA class of operation. The effect of fundamental and harmonic impedances 
is easy to carry out. Moreover, it allows multi-harmonic PAE sensitivity anal-
ysis, which is useful in determining how deviations in matching network design 
affect the PA performance.

Accurate modeling of the bare-die transistor is important to achieve first-pass 
high efficiency PA design. To obtain an accurate model, the mode of operation 
of the transistor in the specific application must be considered. Unlike the 
traditional PAs, the transistor for high efficiency PAs operates in the on- 
and off-regions. This is illustrated in Fig. 2.5 where the loadline of a tradition-
class-AB PA is compared with the loadline of high-efficiency PA. In general, the 
available transistor models are optimized for class-AB operation. This implies 
that the model may not be accurate in the high-efficiency loadline region.

In [Paper A] and [Paper B], an in-house model optimized for high efficiency 
operation is developed for the bare-die transistors. The extracted model is based 
on simplified expressions for the nonlinear currents and capacitances where focus 
is put on accurately predicting on- and off-regions where the high-efficiency 
loadline is located [49]. As mentioned in section 1.2, the PA is used in a high 
efficiency architecture which keeps the PA in saturation for a large output power 
dynamic range, therefore the linearity and the agreement in backoff were not 
taken much into consideration. The model has been extracted from DC- and 
S-parameter measurements referred to the die surface reference plane. The 
simplified expressions ensure a good convergence during simulations and an
2.2. DESIGN PROCEDURE FOR HIGH EFFICIENCY POWER AMPLIFIERS

excellent accuracy in high-efficiency PA operation. Moreover, the model permits
the intrinsic waveforms to be inspected during simulations and therefore allows
a careful study of the transistor operation which is usually not possible with
commercial models.

2.2.3 Circuit design methodology

As mentioned in section 2.1.2, the high efficiency PAs impose different tailored
waveforms for drain-current and drain-to-source voltage, respectively. These
waveforms can be obtained by the control of the harmonic content of the voltage
and current waveforms at the transistor intrinsic terminals. The procedure that
we have followed for optimizing the fundamental and harmonic impedances is
summarized below:

Step 1 Perform a fundamental load-pull/source-pull simulation to find the op-
timum fundamental load and source impedances that maximize the effi-
ciency. The harmonic loads can be initially set to values like open or short
circuit.

Step 2 Using the impedances found in the previous step, perform a harmonic
load-pull/source-pull simulation to find the optimum second and third har-
monic load and source impedances for high efficiency operation. Step 1 is
then repeated to re-optimize the fundamental impedances so the influence
of the new harmonic impedances are taken into account.

Step 3 Design of suitable matching networks that provides those impedances at
the device input and output terminals.

Step 4 Check the intrinsic voltage and current waveforms excursions to prevent
dangerous operation, and to verify that the overlap between the waveforms
is minimized.

Fig. 2.5: Loadline of class-AB and switched-mode operation.
Step 5 Perform MC and EM simulations to study the reliability and the robustness of the design and thus, to ensure first-pass design. We perform EM simulations on the TL parts to ensure accurate synthesis of the input and output matching networks, while MC simulations study the uncertainties introduced by the lumped components and the manufacturing process.

A stability network has to be designed to stabilize the PA and to avoid any oscillation in band or at low frequencies. The stabilization network can be designed either before starting step 1 or after completing step 3 by modifying the input matching network. To improve the stability in the high-frequency band, a series resistance can often be added at the input of the amplifier. A parallel resistance is also needed to reduce the low-frequency gain and hence to increase low-frequency stability.

In the next section, the proposed design procedure is validated by the design and implementation of two high efficiency PAs operating at 3.5 GHz and 5.5 GHz.

### 2.3 3.5 GHz Inverse Class-F power amplifier design example

In paper [A], a 3.5 GHz, high efficiency inverse class-F PA is presented. This PA demonstrates excellent efficiency performance considering the output power, the particular topology and transistor generation used. The parasitic lead inductances and package tab parasitic capacitances degrade the performance in high frequency applications. Thus, in our design and following the discussion in Section 2.2.1, we use bare-die (unpackaged) devices in order to eliminate the effects of the package and get maximum performance. In this design, a 15 W GaN-HEMT bare-die device from Cree [56] is used.

![Simulated intrinsic current and voltage waveforms of the transistor resulting in 80% PAE at 3.5 GHz.](image)

**Fig. 2.6:** Simulated intrinsic current and voltage waveforms of the transistor resulting in 80% PAE at 3.5 GHz.
A simplified transistor model, optimized for SMPAs, is developed in-house and used in the PA design. The model is based on simplified expressions for the nonlinear currents and capacitances where focus is put on accurately predicting the high efficiency, on- and off-regions of the transistor characteristics. The model allows the intrinsic waveforms to be studied in the PA design and therefore allows a careful investigation of the transistor operation. Using the transistor model, the optimum impedances have been determined using the procedure presented in section 2.2.3. Fig. 2.6 shows the simulated intrinsic drain voltage and current waveforms of the transistor (obtained when the transistor see the determined optimum impedances). We notice that the drain voltage waveform is a half-sinusoid whereas the drain current waveform is close to a square wave, which correspond to the inverse class-F waveforms (see Fig. 2.2(b)).

![Fabricated inverse class-F 3.5 GHz PA. Size: 11 × 8cm².](image)

The input and output matching networks were designed to provide, at the fundamental and harmonics, the optimum impedances obtained from the source/load pull simulations. Details about the circuit design is presented in [Paper A]. A photo of the implemented PA is shown in Fig. 2.7.

It is important to remind here that the intention was to obtain the highest peak efficiency in this design. The optimization result of the proposed method has lead to inverse class-F. Moreover, the recent published work on high efficiency PAs are demonstrating peak results in this mode of operation. These results demonstrate that inverse class-F is an excellent mode of operation for maximum peak efficiency at these frequencies using GaN-HEMT devices.

### 2.3.1 Static measurements

Large signal measurements have been performed in order to evaluate the PA performance under static conditions and to evaluate the agreement vs. circuit simulations. A frequency sweep measurement between 3 GHz and 4 GHz has been performed to study the PA performance versus frequency. The PAE and gain of the PA are plotted versus frequency in Fig. 2.8(a) and compared with simulations. A maximum gain and PAE of 12 dB and 78% respectively are located at 3.5 GHz corresponding to a drain efficiency of 82% at this frequency.
The amplifier exhibits higher than 50% PAE between 3.32 GHz and 3.72 GHz, which corresponds to greater than 10% fractional bandwidth. Fig. 2.8(b) shows the simulated and measured gain and PAE versus input power. A peak PAE of 78% is measured for an input drive level of 29 dBm. As expected, good agreement between simulation and measurement results is obtained at high power levels, where the transistor is operated in a high efficiency mode that the model was optimized for.

Fig. 2.8: Simulated and measured (a) PAE and Gain vs. frequency for 29dBm input power; (b) PAE and gain vs. input power.

### 2.3.2 Linearized modulated measurements

The purpose was to design a PA for saturated applications and focus was on obtaining the highest peak efficiency. However, it is still interesting to investigate its performance in a linear application. Therefore, linearized modulated measurements have been performed using realistic input signals such as WCDMA and LTE.

![Digital predistortion scheme](image)

**Fig. 2.9:** Digital predistortion scheme [57].

AM-AM and AM-PM have been traditionally used to develop behavior models for the PA in which the output characteristic of the PA is approximated as a complex polynomial of instantaneous input power level [57]. However, as the bandwidth of the signal increases, memory effects in the transmitter become
significant. Memory effects are attributed to the frequency response of the matching networks, nonlinear capacitances of the transistors, and the response of the bias networks [58]. In our work, we have used the memory polynomial model, presented in [57], that captures both memory effects and nonlinear behavior of the PA. The structure of the corresponding DPD scheme is shown in Fig. 2.9 where $U_n$ and $X_n$ are the input and output of the DPD function. The downconverted and normalized output of the PA, $Y_n$, is compared to $X_n$ for characterization of the PA.

![Fig. 2.10: PA output signal spectrum of at 3.5 GHz before and after DPD (a) 5 MHz WCDMA signal; (b) 20 MHz LTE signal.](image)

The linearized modulated measurements were performed using the memory polynomial model. In the modulated experiments, both a 20 MHz LTE signal with 11.2 dB Peak-to-Average Power Ratio (PAPR) and a 5 MHz WCDMA signal with 6.6 dB PAPR were used. The measured output spectrum at 3.5 GHz of the WCDMA and LTE signals, before and after DPD are shown in Fig. 2.10. Table 2.1 summarizes the average performance of output power and PAE obtained from these experiments, highlighting the minimum ACLR level as well. These results show that standard DPD methods can be used to linearize the PA to meet modern wireless communication system standards.

<table>
<thead>
<tr>
<th></th>
<th>Pout (dBm)</th>
<th>PAE (%)</th>
<th>ACLR (dBc)</th>
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<tr>
<td></td>
<td>w/o</td>
<td>w</td>
<td>w/o</td>
</tr>
<tr>
<td>WCDMA</td>
<td>35</td>
<td>34</td>
<td>45</td>
</tr>
<tr>
<td>LTE</td>
<td>33</td>
<td>32</td>
<td>35</td>
</tr>
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Table 2.1: Measured average output power, average PAE and minimum ACLR level, without (w/o) and with (w) DPD.
2.4 5.5 GHz harmonically tuned power amplifier design example

After the successful validation of the design methodology at 3.5 GHz, we explored, in [paper B], the high frequency capabilities of the design methodology by the design of a harmonically tuned PA at 5.5 GHz. In the design, a 10W GaN bare-die device from Triquint Semiconductors, Inc. has been used [59]. An in-house model optimized for high efficiency operation is developed for the bare-die transistor and used in the design. Using the design methodology presented in section 2.2.3, the simulations showed that the effect of the third harmonic on the efficiency is very small. This is expected since the third harmonic frequency in this case is very high (16.5 GHz) and effectively short circuited by the output capacitance. Therefore, the source and load impedances at fundamental and second harmonic have been considered in the design of the matching networks.

![Fig. 2.11: Simulated intrinsic current and voltage waveforms.](image)

To verify the high efficiency operation of the PA, it has been simulated and the intrinsic waveforms are shown in Fig. 2.11. These waveforms correspond to 75% simulated PAE. Investigation of the waveforms confirm that the voltage/current overlap is minimized which explains the high efficiency obtained. Finally, Fig. 2.12 shows a picture of the PA that has been implemented on the same substrate as the 3.5 GHz-PA.

The main difference of this design compared to the 3.5 GHz-PA is that the effect of the third harmonic was not taken into consideration. Comparing the intrinsic waveforms of the two PAs, we notice the squaring effect of the third harmonic on the drain current in Fig. 2.6, however, this effect is very small for the 5.5 GHz-PA in Fig. 2.11.

The performance of the implemented PA has been evaluated by means of large signal measurements. The PA has been characterized versus frequency between 5.2 GHz and 5.8 GHz with 25 dBm input power drive level. The results presented in Fig. 2.13(a), show that a maximum gain of 12.5 dB is located at 5.42 GHz with a corresponding 70% PAE. Fig. 2.13(b) shows measured gain and PAE versus output power at 5.42 GHz while the presented simulations are performed at 5.5 GHz. The output power compresses at 37.5 dBm and the PAE reaches 70% PAE.
2.5. PERFORMANCE COMPARISON

![Fabricated harmonically tuned 5.5 GHz PA. Size: 6 × 6cm².](image)

**Fig. 2.12:** Fabricated harmonically tuned 5.5 GHz PA. Size: 6 × 6cm².

![Simulated and measured (a) PAE and Gain vs. frequency for 25 dBm input power (b) PAE and gain vs. output power.](image)

**Fig. 2.13:** Simulated and measured (a) PAE and Gain vs. frequency for 25 dBm input power (b) PAE and gain vs. output power.

2.5 Performance comparison

The performance of the PAs presented in [paper A] and [paper B] is compared to recently published highly efficient GaN-HEMT based PAs in S- and C-bands [28,51–55,60–77]. In Fig. 2.14(a) we notice that the PA in [paper A] outperforms all published S-band PAs in terms of PAE except for the ones published in [51, 61, 66]. However, as shown in Fig. 2.14(a), the operating frequency of the amplifier published in [51,61](2 GHz) is much lower than our operating frequency (3.5 GHz). [66] has same operating frequency of the PA in [paper A], slightly higher PAE but lower output power. Moreover, as depicted in Fig. 2.14(c), it has been published three years after the the PA in [paper A]. In Fig. 2.14(a), we notice that for similar frequency of operation in C-band, the PA in [paper B] has similar PAE performance as the one published in [77] but outperforms all the other published PAs.
In conclusion, the 3.5 GHz-PA presented in [paper A] and the 5.5 GHz-PA presented in [paper B] are among the best published PAs in S- and C-bands respectively. Therefore, these results demonstrate the success of the selected bare-die mounting, modeling, and circuit design methodologies used to implement PAs with high peak efficiency performance.
Chapter 3

High efficiency wideband power amplifier design

Due to the narrowband spectrum allocations, the design of PAs for wireless communications has traditionally been targeted for low RF bandwidths similar to the ones presented in Chapter 2. However, modern and future wireless systems will require larger spectrum allocations to support increased data rates [5]. Moreover, efficient wideband PAs are needed to reduce the operational costs of multi-standard transmitters. This makes wideband PAs that cover many frequency bands while maintaining high efficiency a hot research topic.

One of the important factors for designing wideband PAs is the device technology. The output impedance of the device is usually characterized by a shunt $R - C$ circuit. Using a lossless network as shown in Fig. 3.1, Fano [14] describes the best theoretical match that can be achieved across a bandwidth to a load. He demonstrated that the bandwidth, over which a good match of a complex load impedance can be obtained, is limited. A fundamental limitation, for a parallel $R - C$ network is derived in [14] and given below:

$$\int_0^\infty \frac{1}{|\Gamma|} d\omega \leq \frac{\pi}{RC}.$$  \hspace{1cm} (3.1)

Solving for the reflection coefficient $|\Gamma|$, we obtain [14]:

$$\Delta\omega \ln \frac{1}{|\Gamma|} \leq \frac{\pi}{RC}.$$  \hspace{1cm} (3.2)

This result shows that the bandwidth over which a good match is obtained is limited by the $RC$ product.
Since LDMOS RF power transistors, which are the devices currently used in base stations, have large output capacitance, according to (3.2), the design of wideband power amplifiers is very challenging. The impedance at the interface of the transistor die can be lower than 1 Ω. Thus, it is very difficult or impossible to achieve the necessary high $Q$ transformation to 50 Ω across a wide bandwidth. Referring to section 1.3.1, the impedances at the interface of the recently developed GaN RF power transistors are much larger which opens up possibilities for wideband designs. Compared to LDMOS, the output capacitance of a GaN-HEMT is reduced by almost an order of magnitude for a given output power [78]. Hence, according to (3.2), GaN with its lower capacitance is easier to match over a wider bandwidth.

In the remainder of this chapter, an overview of different conventional broadband PA topologies are reviewed. Then, a proposed design approach for wideband PAs and a systematic method for the design of suitable broadband matching networks is presented. They are validated through the design of a high efficiency 2-4 GHz octave bandwidth PA. Then, a novel push-pull harmonic load-pull measurement setup is proposed to investigate the potential of broadband push-pull PAs for microwave applications and a prototype 1-3 GHz push-pull PA has been implemented for this purpose.

## 3.1 Broadband power amplifiers

In this section, different techniques used for designing broadband amplifiers in hybrid or monolithic technologies will be reviewed. Traveling wave distributed circuit, lossy matched circuit, and feedback circuit are among the most popular techniques. Other approaches to design wideband high power and efficiency PAs that have been recently published will also be discussed.

### 3.1.1 Traveling wave amplifier

The problem of the input and output capacitances of the transistor that is limiting broadband match, is overcome in the Traveling Wave Amplifier (TWA), also referred to as distributed amplifier, by incorporating the input and output capacitances of several transistors into an artificial transmission-line structure as shown in Fig. 3.2. The amplifier consists of an input line incorporating the input capacitances of the transistors and an output line incorporating the output

![Fig. 3.2: Circuit topology of the traveling wave amplifier.](image)
capacitances. By amplifying the signal at the input line and feeding it to the output line, a broadband amplifier from low frequencies to the cut-off frequency of the artificial lines can be obtained [79].

The main advantages of the TWA are the simple circuit topology and the achievable wide bandwidth. Multi-octave and even multi-decade TWAs have been already demonstrated [80,81]. However, the disadvantages of this approach lie in the high number of active devices needed to achieve the same gain as of a single device which results in large size and high manufacturing cost. Moreover, its low output power results in low PAE performance [80–82].

### 3.1.2 Lossy matched amplifier

The lossy matched amplifier uses resistors within its input- and output-matching networks in order to guarantee flat gain over a wide bandwidth [83]. Fig. 3.3 illustrates the lossy matched amplifier. The resistors help increasing the impedance levels and thus according to (3.2) enable more wideband operation.

![Circuit topology of the lossy amplifier.](image)

A theoretical analysis of this configuration is presented in [83]. Simulations results show that the gain, up to 5 GHz, of a single stage lossy matched amplifier is the same as for a four-stage traveling wave amplifier. Moreover, its PAE is at least four times higher than the four stage TWA [83]. However, its moderate bandwidth compared to a TWA is its main disadvantage.

### 3.1.3 Feedback amplifier

The feedback amplifier, shown in Fig. 3.4, employs a negative feedback by connecting a resistor $R_{fb}$ between the gate and drain of the transistor [84]. This helps stabilizing the device and makes the input and output impedances much closer to the desired 50 $\Omega$ [79]. The value $R_{fb}$ controls the gain and bandwidth of the amplifier. $L_{fb}$ and $L_2$ can be optimized to extend the amplifiers bandwidth [85]. $L_1$, $C_1$, and $C_2$ are used to achieve very good input and output return loss [79]. In comparison with the TWA, the feedback amplifier is less complex and gives higher PAE. The main disadvantage of this type of amplifier is its low output power due to loss associated with the feedback resistor.

When implemented with discrete components, the frequency response of the feedback amplifier can be very sensitive, therefore it is mainly implemented in MMIC technology [85]. A recent attempt to design a hybrid wideband high
efficiency feedback power amplifier is presented in [38]. The results showed a decade bandwidth (0.3 GHz-3 GHz) but the obtained output power levels and PAE (20%-40%) are quite low.

3.1.4 Amplifiers with resistive harmonic terminations

Another approach used to design wideband PAs is based on the optimization of the fundamental impedance while resistive terminations are presented for high order harmonics. Using this approach, it is possible to achieve multioctave bandwidths, however, leading to low efficiency levels.

In [86], a 10 W octave bandwidth (0.7-1.5 GHz) PA designed using lumped matching networks is presented. However, the design approach does not involve any harmonic tuning, which explains the low PAE levels obtained (30-35%).

A 2 W, multi-octave (0.8-4.0 GHz) PA in GaN technology is presented in [87]. The design approach is similar to Class-AB using matching networks. The results show a gain and PAE less than 7 dB and 40% respectively.

In [88], a decade bandwidth (0.4-4.1 GHz) PA, using a Chebychev transformer to design the wideband matching networks, is presented. The gain and PAE are between 10-15 dB and 40-60%, respectively.

3.1.5 Wideband switched-mode power amplifiers

The techniques presented previously offer wide bandwidth but not the required high efficiency levels. To increase the efficiency, techniques like harmonic tuning [4, 43] or switching mode [44] should be used as discussed in Chapter 2.

In this context, many wideband class-E PAs are reported in literature. A wideband class-E PA using synthesized low-pass matching networks operating between 1.2-2.0 GHz is presented in [89]. Two Class-E power amplifiers, with moderate bandwidth (2.0-2.5 GHz), are presented in [18] and [19]. The design approach is similar to conventional Class-E PA but using a wideband matching network. The PAE levels obtained are approximately 50% and 70% respectively. The difference in performance is due to the technology, where the former is a MMIC PA while the latter is a hybrid design using a bare-die technique. As we notice, such amplifiers have modest bandwidth because the required harmonic terminations cannot be realized over large bandwidths due to the device parasitics and the required high quality factor matching networks.
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3.1.6 Continuous modes power amplifiers

Recently, continuous modes of operation have been explored for class-B/J [48], class-F [90] and inverse class-F [91] PAs. The investigations demonstrated that a continuum of PAs modes, with high constant efficiency over a continuous range of fundamental and harmonic terminations, exists. In [48], it has been demonstrated that starting from class-B mode, a continuum of solutions between class-B and class-B/J allow high efficiency performance when the fundamental and second harmonic impedances are manipulated. Similar study, conducted on class-F PAs [90], shows that controlling the fundamental and second harmonic impedances can lead to better performance than class-B/J mode in terms of output power, efficiency and bandwidth. Moreover, for inverse class-F [91] PAs, it is shown that changing simultaneously the susceptance of fundamental and the second harmonic termination, constant high efficiency and high output power levels can be maintained over wide bandwidth.

Circuit demonstrators of continuum class-B/J, -F modes have been implemented. However, this is not the case for continuum inverse class-F mode. In [20], a 10 W wideband Class-B/J PA demonstrates 60-70% efficiency across 1.35-2.25 GHz. Two Class-B/J PAs are presented in [92], where the first PA covers 1.6-2.2 GHz with 55-68% efficiency while the second covers 0.5-1.8 GHz with 50-69% drain efficiency. The practical behavior of continuous class-B/J modes for high power ranges is successfully investigated in [93], where 53-63% efficiency and 60-75 W output power are obtained across 0.9-2.3 GHz. A continuum class-F PA [94], demonstrated at low frequencies 0.55-1.1 GHz, achieves 9-13 W output power and 65-80% drain efficiency.

A mode-transferring technique for designing high-efficiency wideband PAs is presented in [95]. The adopted matching network provides wideband fundamental matching and proper tuning of the second and third harmonics that allow the PA to operate between inverse class-F and class-F modes. The implemented 1.3-3.3 GHz PA demonstrates high efficiency at 1.8 GHz and 2.8 GHz where the PA operates in inverse class-F and class-F modes. However, the efficiency drops by about 25% across the rest of the band.

3.2 Harmonically tuned wideband PA design approach

In this section, we present a design approach for high-efficiency PAs limited to one octave bandwidth. The approach, presented in [paper C], is based on realizing the optimal fundamental and second harmonic impedances derived from harmonic sourcepull/loadpull simulations. Moreover, a detailed method for the design of suitable broadband matching network solutions will be presented.

3.2.1 Design approach

The suggested approach can, in general, be used to design any wideband PA. However, the achieved bandwidth depends strongly on the type of device used as discussed in the introduction of this chapter. The main steps are enumerated hereafter:
Step 1 Perform a fundamental load-pull/source-pull simulation (or load-pull measurement) to find the optimum source and load impedances that maximize the device’s efficiency performance. Repeat for a number of frequencies spanning the bandwidth of interest.

Step 2 The effect of the second harmonic on the performance is very critical; therefore this step consists of varying the impedance of the second harmonic, at different frequencies, across the periphery of the Smith-chart while the device sees the optimum source and load impedances obtained in step 1 at the corresponding frequency. This step determines the region where the second harmonic maximizes the efficiency.

Step 3 The device output impedance can be approximated by a shunt $R - C$ circuit. This step consists of determining, from the optimum impedances found in step 1, the load line $R$ and the output capacitance of the transistor $C$. For simplicity, the values of $R$ and $C$ can be calculated from the optimum impedance at the center frequency of the band.

Step 4 A wideband matching network should be designed to match the determined $R - C$ circuit to 50$\Omega$ across the bandwidth.

Step 5 The second harmonic of the designed wideband matching network must be checked to verify that it is located in the region that maximize the efficiency as determined by step 2.

Step 6 In case the second harmonic is degrading the performance, the designed network must be modified so it can take care of the second harmonic impedance.

This procedure is illustrated with a practical design of a high efficiency GaN-HEMT octave bandwidth, 2-4 GHz, PA in [paper C]. Step 1 is performed by doing load-pull/source-pull simulations to find the optimum impedances at 2, 2.5, 3, 3.5, and 4 GHz. A typical example, of how the first step may look in practice, is illustrated in Fig. 3.5(a).

Step 2 of this procedure is performed by varying the impedance of the second harmonic, at different frequencies, across the periphery of the Smith-chart while the device sees the optimum source and load impedances at 3 GHz. A practical example of how the PAE of the device versus the phase variation of the unity magnitude second harmonic reflection coefficient may look is shown in Fig. 3.5(b). We notice that PAE is dramatically degraded when the phase of the second harmonic approaches the short circuit region (180$^\circ$). This means that there is no need for additional design efforts for the second harmonics if the matching network does not approach the short circuit region.

In the following section, Step 4 of the proposed procedure is addressed by presenting a systematic method to design a wideband matching network.

### 3.2.2 Wideband matching network design

Fano [14,96], derived exact simultaneous transcendental equations for the design of wideband matching networks. However, these equations appeared to need computer iteration for their solution. Fortunately, an analytic solution of these equations has been recently derived in [97]. Starting from the solutions of these
3.2. HARMONICALLY TUNED WIDEBAND PA DESIGN APPROACH

Fig. 3.5: (a) Efficiency optimized source and load impedances (b) Simulated PAE versus phase of the unity magnitude second harmonic reflection coefficient.

equations, a step-by-step derivation of a wideband lumped element network is presented. Then, the lumped network is approximated by a corresponding distributed network in realization of a practical circuit.

The output impedance of the device of a power transistor is typically a parallel $R-C$ circuit, where $R$ is much lower than 50 $\Omega$. The required equations for the design of the lumped network are given in detail in this section since they were not presented in [Paper C] due to lack of space. However, it is important to note that if the transistor impedance is modeled as a series $R-C$ circuit instead, similar approach can be also used. However, new equations must be derived.

The normalized admittances, $g$ elements, for the prototype low-pass matching network, Fig. 3.6(a), can be calculated using equations found in [97]. They represent a low-pass filter in a 1 $\Omega$ system with 1 rad/s corner frequency. The low-pass prototype network corner frequency is scaled from the nominal 1 rad/s to the design value ($\omega_c$) by dividing the elements by $2\pi(f_2-f_1)$ [97], where $f_1$ and $f_2$ are the lower and upper bandpass frequencies respectively. For impedance scaling, the series elements $g_0$, $g_2$, and $g_4$ are multiplied by $R$ while the shunt elements $g_1$ and $g_3$ are divided by $R$.

\[
C_1 = \frac{g_1}{2\pi(f_2-f_1)R_0}, \tag{3.3}
\]

\[
L_2 = \frac{g_2R_0}{2\pi(f_2-f_1)}, \tag{3.4}
\]


\[ C_3 = \frac{g_3}{2\pi} (f_2 - f_1) R_0, \]  
\[ R_L = g_4 R_0. \]  

Applying the above scaling formulas, the values \( C_1, L_2, C_3, \) and \( R_L \) can be obtained and hence, the low-pass network Fig. 3.6(a). The low-pass network is transformed into a bandpass network, by resonating each series or shunt element at the geometric mean frequency \( 2\pi \sqrt{f_1 f_2} \). The bandpass network is shown in Fig. 3.6(b) and the resonating elements are given by:

\[ L_1 = \frac{1}{4\pi^2 f_1 f_2} C_1, \]  
\[ C_2 = \frac{1}{4\pi^2 f_1 f_2} L_2, \]  
\[ L_3 = \frac{1}{4\pi^2 f_1 f_2} C_3. \]  

An ideal transformer with an impedance transformation ratio of \( 50/R_L \) is inserted at the output. By shifting the transformer to the left as shown in Fig. 3.6(c), \( R_L \) is transformed to \( 50 \Omega \) and \( L_3 \) is scaled upwards in impedance.

\[ R_{L,F} = n^2 R_L, \]  
\[ L_{3,F} = n^2 L_3. \]
A Norton transformation is then used to remove the ideal transformer by transforming it, together with the two capacitors $C_2$ and $C_3$, into a $\Pi$ arrangement of capacitors as shown in Fig. 3.6(d) [98]. The values of the resulting capacitors $C_{2F}$, $C_{3F}$, and $C_{4F}$ are given by the following formulas:

\begin{align}
C_{2F} &= C_2/n, \quad (3.12) \\
C_{3F} &= (C_3 + (1 - n)C_2)/n^2, \quad (3.13) \\
C_{4F} &= (n-1)C_2/n. \quad (3.14)
\end{align}

By applying equations (3.3)-(3.14), all the element values in Fig. 3.6(d) can be determined and therefore, matching to $50\,\Omega$ over a wide bandwidth can be achieved. The capacitor $C_1$ can be replaced by three parallel capacitors; $C_{11}$, $C_{12}$, and the transistor output capacitance $C_{out}$ as shown in Fig. 3.6(e). Finally, some transformations between lumped and distributed elements, well explained in [Paper C], have been used to transform the lumped elements matching network into the final distributed network shown Fig. 3.6(f).

### 3.3 Wideband power amplifier design example

The design approach of high efficiency wideband PA presented in previous sections, is validated through the design, manufacturing, and test of an octave bandwidth 2-4 GHz PA. The design is described in detail in [Paper C], but summarized below.

#### 3.3.1 2-4 GHz power amplifier design

By calculating the inverse of the conjugate value of the optimum fundamental load impedance obtained at 3 GHz, a load line of $R_0 = 32\,\Omega$ and a transistor output capacitance of $C_{out} = 2.4\,\text{pF}$ can be estimated. In summary, the matching network should therefore be designed to match $R_0$ and $C_{out}$ to $50\,\Omega$ across the 2-4 GHz bandwidth. Using the method presented in the previous section a wideband lumped element matching network have been derived for the output side and finally converted to a distributed matching network. An analogous procedure has been used for the input matching network.

Fig. 3.7 shows the impedance of the output matching network as well as the impedance of the second harmonic. We notice that the second harmonic is far away from short circuit and hence, according to the results in Section 3.2, high PAE performance is expected across the bandwidth.

The resulting PA topology is shown in Fig. 3.8(a). The input and output matching networks are surrounded by the dashed and solid boxes respectively. The output matching network is dominated by $TL_6 - TL_8$ and $C_5$, which are given by the network in Fig. 3.6(f). $TL_1$ and $TL_5$ are short transmission lines added to facilitate the physical connections to the transistor die. The input matching network has been slightly modified in order to stabilize the PA. The series resistance $R_{g2}$, and the parallel resistance $R_{g3}$, are added at the input of the amplifier to improve the stability in the high and low frequency bands, respectively. $L_{bwg}$ and $L_{bwd}$ are used to model the input and output bondwire
CHAPTER 3. HIGH EFFICIENCY WIDEBAND POWER AMPLIFIER DESIGN

Fig. 3.7: Simulated impedance of the distributed output matching network versus frequency. The fundamental and second harmonic impedance frequency ranges are given by 2-4 GHz, and 4-8 GHz, respectively.

The fundamental and second harmonic impedances are given by 2-4 GHz, and 4-8 GHz, respectively. Finally, the inductors \( L_g \) and \( L_d \) are used to prevent the leakage of RF into the DC supply lines. The PA was implemented on a Rogers 5870 substrate with \( \varepsilon_r = 2.33 \) and a thickness of 0.4 mm. Its size is 65 \( \times \) 65 mm\(^2\). Fig. 3.8(b) shows a picture of the fabricated PA using the bare-die GaN-HEMT device.

3.3.2 Static measurements

Large signal CW measurements have been performed in order to evaluate the PA performance under static conditions. In Fig. 3.9-(a) and Fig. 3.9-(b) the PA performance in terms of output power and drain efficiency is plotted versus frequency, for a fixed input power of 31 dBm. The results show an output power between 40 – 42 dBm in the frequency range of 1.9 GHz-4.3 GHz which means that less than 2 dB ripple in the output power, and hence in the power gain, is obtained across the band. Within the same band the drain-efficiency of the amplifier is between 57 % and 72 %. This corresponds to a PAE between 50 % and 63 % and a fractional bandwidth of 78 % about a center frequency of 3.1 GHz. It is important to note that the simulations and measurements agree well, which validates the models and design methods used.
3.3. WIDEBAND POWER AMPLIFIER DESIGN EXAMPLE

Fig. 3.9: Measured and simulated (a) output power versus frequency for a fixed input power of 31 dBm (b) drain efficiency versus frequency for a fixed input power of 31 dBm (c) PAE vs. output power at 2, 2.5, 3.5 and 4 GHz (d) gain vs. output power at 2, 2.5, 3.5 and 4 GHz.

Fig. 3.9-(c) and Fig. 3.9-(d) show the power gain and the PAE plotted versus output power for different frequencies 2, 2.5, 3.5, 4 GHz. We notice that in Fig. 3.9-(d), the gain decreases at low input power levels. The reason behind this behavior is that the gate bias voltage used in the measurements is selected slightly below the pinch-off voltage in order to maximize the peak efficiency. To get a constant back-off gain, the gate bias must be slightly increased. This will result in a small degradation in peak efficiency.

3.3.3 Performance comparison

The performance of the presented PA is compared to recently reported wideband amplifiers in Table 3.1. We notice that the PA in [19, 94] have higher efficiency than the PA in [Paper C]. However, the PA in [Paper C] has larger bandwidth and higher operating frequency.

In [38, 87, 88], the reported PAs have higher relative bandwidth compared to the PA reported in [Paper C]. However, the gain, the output power, and the efficiency in [Paper C] are much higher.

The PAs reported in [95,99] outperform the PA in [Paper C] in terms of band-
width and efficiency. However, their measurements were performed at variable drain bias voltage. At each frequency, the drain bias voltage was optimized to get the highest possible efficiency performance. Moreover, the variation in the efficiency performance across the bands of both PAs is exceeding 25%.

The PAs reported in [92, 93] outperforms the PA in [Paper C] in terms of bandwidth and output power. However, their efficiency and operating frequencies are lower. Regarding the other reported PAs, our PA outperforms all of them in terms of bandwidth, efficiency and operating frequencies. This comparison shows that the PA in [Paper C] has state-of-the-art efficiency, bandwidth and output power performance for GaN PAs covering the S-band.

<table>
<thead>
<tr>
<th>Reference</th>
<th>BW(GHz)</th>
<th>BW(%)</th>
<th>Pout(W)</th>
<th>Gain(dB)</th>
<th>Drain Eff(%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2006 [18]</td>
<td>1.9-2.4</td>
<td>23</td>
<td>5-7</td>
<td>9-10</td>
<td>57-62</td>
</tr>
<tr>
<td>2008 [87]</td>
<td>0.8-4.0</td>
<td>133</td>
<td>1-2</td>
<td>5-7</td>
<td>40-55</td>
</tr>
<tr>
<td>2008 [86]</td>
<td>0.7-1.5</td>
<td>73</td>
<td>9-10</td>
<td>10-11</td>
<td>33-38</td>
</tr>
<tr>
<td>2009 [19]</td>
<td>2.0-2.5</td>
<td>22</td>
<td>7-12</td>
<td>10-13</td>
<td>74-77</td>
</tr>
<tr>
<td>2009 [20]</td>
<td>1.3-2.2</td>
<td>50</td>
<td>9-11</td>
<td>11-12</td>
<td>60-70</td>
</tr>
<tr>
<td>2010 [38]</td>
<td>0.3-3.0</td>
<td>163</td>
<td>5-10</td>
<td>5-10</td>
<td>25-50</td>
</tr>
<tr>
<td>2010 [21]</td>
<td>1.9-2.9</td>
<td>42</td>
<td>35-50</td>
<td>10-12</td>
<td>60-65</td>
</tr>
<tr>
<td>2011 [100]</td>
<td>1.3-2.7</td>
<td>70</td>
<td>10-15</td>
<td>10-12</td>
<td>56-70</td>
</tr>
<tr>
<td>2011 [94]</td>
<td>0.55-1.1</td>
<td>67</td>
<td>9-13</td>
<td>9-12</td>
<td>65-80</td>
</tr>
<tr>
<td>2011 [101]</td>
<td>1.0-2.0</td>
<td>67</td>
<td>60-90</td>
<td>9-11</td>
<td>30-65</td>
</tr>
<tr>
<td>2011 [99]</td>
<td>0.9-2.2</td>
<td>84</td>
<td>10-20</td>
<td>10-13</td>
<td>63-89</td>
</tr>
<tr>
<td>2012 [95]</td>
<td>1.3-3.3</td>
<td>87</td>
<td>10-14</td>
<td>11-12</td>
<td>58-86</td>
</tr>
<tr>
<td>2012 [93]</td>
<td>0.9-2.3</td>
<td>87</td>
<td>60-75</td>
<td>11-12</td>
<td>53-63</td>
</tr>
<tr>
<td>2012 [88]</td>
<td>0.4-4.1</td>
<td>164</td>
<td>10-15</td>
<td>10-15</td>
<td>40-62</td>
</tr>
<tr>
<td>2012 <a href="a">92</a></td>
<td>1.6-2.2</td>
<td>33</td>
<td>10-13</td>
<td>10-12</td>
<td>55-68</td>
</tr>
<tr>
<td>2012 <a href="b">92</a></td>
<td>0.5-1.8</td>
<td>113</td>
<td>8-12</td>
<td>12-15</td>
<td>50-69</td>
</tr>
<tr>
<td>[Paper C]</td>
<td>1.9-4.3</td>
<td>78</td>
<td>10-15</td>
<td>9-11</td>
<td>57-72</td>
</tr>
</tbody>
</table>
In conclusion, the PA in [Paper C] shows an excellent performance in terms of output power, gain, efficiency and linearity. This performance demonstrates the success and the usefulness of the proposed approach for the design of wideband PAs for future wireless systems combining wide bandwidth and high efficiency.

### 3.4 Push-pull microwave power amplifiers

The design methodology presented above is valid for PAs with octave bandwidth or lower. It cannot be extended for more than one octave because the harmonics fall inside the required bandwidth and hence harmonic tuning will not possible. To overcome this problem, the push-pull design technique that allows second harmonic tuning over bandwidths exceeding one octave can be used. In the following, the principle of operation of push-pull PAs is therefore first reviewed.

#### 3.4.1 Principle of operation

The push-pull PA consists of two devices driven differentially so that the equivalent circuit shows the two devices being driven in antiphase [4]. To combine the branches of the two devices and to achieve the required phase shift, push-pull PAs require baluns to be connected at the input and output of the PA.

![Ideal Balun](https://via.placeholder.com/150)

**Fig. 3.10:** Push-pull with a T network load, (a) circuit topology, (b) equivalent circuit at fundamental and odd harmonics, (c) equivalent circuit at even harmonics.

To illustrate the principle of operation, consider a differential ideal T-section network connected between the two devices as shown in Fig. 3.10(a). The T-network is composed of a differential impedance $Z_D$ and a common-mode conductance $Y_C$. The behavior of the circuit at even harmonics will be different from its response at fundamental and odd harmonics. The fundamental and odd harmonics voltage components of each PA will be equal in amplitude, but opposite in phase. Consequently, a virtual ground develops at the line of symmetry.
at the center of the differential impedance so the devices share the impedance $Z_D$, and hence, the equivalent circuit in differential mode will be equivalent to the one shown in Fig. 3.10(b). However, at the even harmonics, the harmonic voltage components are equal in amplitude and phase. Therefore, the line of symmetry becomes a virtual open circuit and the devices share the conductance $Y_C$ as shown in Fig. 3.10(c).

Thus, the advantage of the presented push-pull topology comes from the different responses at even and odd harmonics. They add a degree of freedom that allows fundamental and second harmonic frequency impedances both to be optimized without the bandwidth restrictions in a single-ended design.

### 3.4.2 Push-pull microwave power amplifiers in literature

Generally, broadband push-pull PAs were mostly targeted for low frequency applications [102–105]. At microwave frequencies, different push-pull architectures have been proposed. A push-pull PA using periodic structures for harmonic tuning is proposed in [106] while a push-pull PA based on an extended resonance technique is presented in [107]. The benefit of separating the effects of the even and odd harmonic frequencies in push-pull configurations is used in [108] by the simple connection of a pair of inverse class-F PAs and in [109] by the connection of a pair of the newly introduced class-E/F PAs. However, the mentioned architectures were targeted for narrowband applications because the realization of broadband baluns at microwave frequencies is very challenging [4].

Recently, efforts have been put to design broadband balun suitable for common mode operation at microwave frequencies [110]. Moreover, using this latter balun, a decade bandwidth push-pull PA has been demonstrated in [22]. The PA operates between 250 MHz and 3.1 GHz with a drain efficiency higher than 45%. This result demonstrates the bandwidth potential of the push-pull configuration at microwave frequencies. However, in general, there is a lack in understanding the true operation and interaction between push-pull PAs and output baluns. In [Paper D], we propose a push-pull harmonic load-pull measurement setup that allows the influence of the balun on PA performance to be investigated in detail under realistic push-pull operating conditions.

### 3.4.3 Investigation of push-pull microwave power amplifiers

In the following, the proposed measurement setup, the implemented push-pull PA used in the experiments, and the results of the study that investigates the influence of the balun characteristics on the overall PA characteristics are presented.

#### 3.4.3.1 Proposed push-pull harmonic load-pull setup

The push-pull harmonic load-pull setup, developed for our experimental investigations and shown in Fig. 3.11, is based on an active load-pull technique [111–114]. It can provide, at the calibrated reference plane, any impedance for fundamental and second harmonic frequencies, as well as measuring the voltage and current waveforms at fundamental and all harmonics. A Large Signal Network Analyzer (LSNA, Maury/NMDG MT4463) is used to measure the
traveling voltage waves $a_1$, $b_1$, $a_2$ and $b_2$ at the calibrated reference plane. The fundamental ($f_0$) input signal to the PA is generated with a synthesized CW RF signal generator. Two automated mechanical tuners (Maury MT982) are used to present the required impedance for fundamental frequencies at the calibrated reference plane. Then, in order to set the load reflection coefficient at the second harmonic ($2f_0$), another synthesized CW RF signal generator is used. The amplitude and phase control of the injected signal at the second harmonic is achieved by using vector modulators.

The proposed setup will be used to emulate a balun at the output of a push-pull PA and to study the effect of the balun on the PA performance. This kind of measurement cannot be performed by measuring the output branches of the PA independently with a traditional harmonic load-pull setup because, according to Fig. 3.10, the matching networks seen at the fundamental and second harmonics look different and they are only different when the other branch is operated in a balanced mode.

Based on the measured voltage waveforms, the performance of the push-pull PA can be easily calculated

$$\begin{align*}
P_{out} &= \frac{|b_1|^2}{2Z_0} + \frac{|b_2|^2}{2Z_0} \quad \text{(3.15a)} \\
\eta &= \frac{P_{out}}{P_{dc}} \\
\text{Gain} &= \frac{P_{out}}{P_{avs}}
\end{align*}$$

where $Z_0$ is the impedance of the single-ended PA branch. $P_{dc}$ and $P_{avs}$ are the total DC power consumption and the available input power, respectively.
3.4.3.2 1-3 GHz push-pull power amplifier prototype

The prototype PA used in the investigation uses the same operational principle described in section 3.4.1. As shown in its topology depicted in Fig. 3.12, the push-pull PA consists of two identical PA branches and a balun. Each PA is a wideband single-ended PA, designed following the same approach used in Sec 3.2. The two PAs are connected at the input through a commercial balun [115]. However, the output is kept in balanced configuration to be able to study the effect of the balun on the performance of wideband PAs. The two, $TL_e$, output lines are added to facilitate the connection to the output; they are not a part of the matching networks and they will be de-embedded during the measurements.

![Proposed push-pull power amplifier topology.](image)

**Fig. 3.12:** Proposed push-pull power amplifier topology.

The push-pull PA was implemented on a Rogers 5870 substrate with $\varepsilon_r = 2.33$ and thickness of 0.8 mm. Its size is $65 \times 55 \text{ mm}^2$. Fig. 3.13 shows a photo of the fabricated push-pull PA using bare-die GaN-HEMT devices.

![Photo of the implemented wideband push-pull power amplifier.](image)

**Fig. 3.13:** Photo of the implemented wideband push-pull power amplifier.
3.4.3.3 Experimental results

The measurement setup presented above has been used to accomplish the push-pull load-pull measurements at the intrinsic reference plane indicated in Fig. 3.11.

![Graph](image)

Fig. 3.14: Measured performance for a fixed input power of 31 dBm (a) output power versus frequency (b) drain efficiency vs. frequency (c) output power and gain vs. frequency (d) PAE vs. frequency.

The PA was firstly characterized versus frequency between 1 GHz and 3.4 GHz. Three different terminations of the second harmonic impedance of the output balun have been used. The realized terminations for the second harmonic (common mode) impedance were: Open, 50Ω, and arbitrary impedances as shown in Fig. 3.14(a). The arbitrary impedances are obtained when no signal is injected at the second harmonic. Fig. 3.14(b), Fig. 3.14(c), and Fig. 3.14(d) show the measured frequency response of the push-pull PA for three different terminations. It is clear that the common mode second harmonic termination of the output balun has big impact on the performance of the PA, in particular for the lower frequencies where the second harmonic falls within the fundamental frequency range. The drain efficiency is improved at certain frequencies by 10% when open termination is used instead of 50Ω and about 5% when arbitrary termination is realized.
In case of the open second harmonic, the measured output power is between $38 - 41\,\text{dBm}$ in the frequency range of 1.3 GHz-3.3 GHz which means that the power gain, is between $7 - 10\,\text{dB}$. Within the same band the drain-efficiency of the PA is between 45\% and 63\%. This corresponds to a PAE between 40\% and 57\% and a fractional bandwidth of 87\% about a centre frequency of 2.3 GHz.

Many conclusions can be drawn from the results obtained in [Paper D]. The investigation shows that the setup allows the interaction between the push-pull PA and balun operation to be isolated from each other and is therefore an important tool for such investigations. Moreover, although the push-pull operation can separate the fundamental and second harmonic impedances, the problem is instead to design an output balun that avoids the common mode second harmonic reflection phases that degrade the efficiency. The common mode frequency response of the balun, like the one presented in [22], needs to be carefully mapped to the areas where high efficiency can be preserved. The fundamental bandwidth limitations imposed by the balun (or balanced antenna) common mode impedance response is still matter for future research where the setup proposed in [Paper D] can play an important role.
Chapter 4

High efficiency dual-band Doherty power amplifier design

In the previous chapters, the focus was on maximizing the high peak efficiency of single-band and wideband PAs. The peak efficiency of the PA is obtained close to its saturated output power. However, as shown in Fig. 1.3(b), the efficiency of the PA decreases dramatically as the signal power is backed-off.

In fact, the never-ending demand on increasing data traffic and achieving higher data rate transfer resulted in nonconstant envelope modulation schemes. The high PAPR of the involved signals causes the PA to operate at an average output power far below the saturation region resulting in low average efficiency levels. Among the different techniques proposed to increase the average efficiency, the Doherty PA has demonstrated to be a promising and effective solution [10]. It operates at a nearly constant efficiency for a targeted range of input and/or output power levels, typically of 6 dB [10, 12, 24, 27, 116–118].

So far, lot of work has been done on single-band DPAs [12, 23–32]. However, this does not satisfy the multi-band and multi-standard requirements of modern and future RBSs as discussed in section 1.1. Some efforts have been put to increase the bandwidth of the DPA by using reconfigurable matching networks [119] or by exploiting wideband matching networks [120–125]. However, the experimental results showed that the obtained bandwidths are still not wide enough to cover many bands at the same time. Moreover, another drawback is that, wideband DPAs do not always have ideal operation over the bandwidth of operation. This leads to significant degradation in the DPA performance compared to the case where DPAs are designed for single frequency operation.

To overcome these limitations, dual-band DPAs arise as a good candidate because the flexibility of choosing the operating bands. Moreover, the performance of the dual-band DPAs can be similar to single-band DPAs since the passive networks can be optimized simultaneously for the two operating bands. Recently, there have been some efforts to optimize a DPA for dual-band operation [33, 35, 89]. However, they present architectural overviews without any comprehensive or general design methodology. In the following, a detailed design methodology for high efficiency dual-band DPAs is presented.
4.1 Design approach

The DPA basic operational principle will be reviewed before thoroughly presenting the design approach of dual-band DPAs.

4.1.1 Conventional Doherty power amplifier

A simplified diagram of the conventional Doherty power amplifier is shown in Fig. 4.1. It consists of two current sources representing the Main amplifier and Auxiliary amplifier, and quarter-wavelength impedance transformer ($Z_T$). The load seen by each current source ($Z_M$ and $Z_A$) is controlled by the current level of the other one ($I_M$ and $I_A$). The quarter-wavelength impedance transformer acts as an impedance inverter. Thus, when the current supplied by the Auxiliary amplifier ($I_A$) increases, the load impedance of the Main amplifier, $Z_M$, decreases.

![Fig. 4.1: Simplified schematic of the Doherty power amplifier.](image)

Two different regions, according to the power level, can be distinguished in the DPA operation; the low power region and the Doherty region. At the low power region, the Main amplifier is only active, and hence the load modulation does not appear. When the Main amplifier reaches its maximum efficiency, the Auxiliary amplifier is turned on and the load impedances of the amplifiers are varied according to the current ratio. As the input power increases, $Z_M$ and $Z_A$ decrease respectively from $Z_L^2/Z_L$ and $\infty$ to both reach $R_{opt}$, which is the load impedance for the maximum output power. The theoretical expected behavior of drain efficiencies of the Main and Auxiliary amplifiers and the one of the DPA are shown in Fig. 4.2.

![Fig. 4.2: Efficiency behavior of Main, Auxiliary and Doherty amplifiers.](image)
4.1. DESIGN APPROACH

A general block diagram of the conventional DPA is shown in Fig. 4.3. It is composed of the Main and Auxiliary amplifiers that are connected through an Input Power Splitter (IPS), Phase Compensation Network (PCN), an Impedance Inverter Network (IIN), and an Impedance Transformer Network (ITN).

Fig. 4.3: Circuit topology of conventional Doherty power amplifier.

4.1.2 Dual-band design of the passive structures

To obtain a dual-band operation in a DPA, the passive structures, such as Main and Auxiliary matching networks, IPS, PCN, IIN, and ITN, must be designed to ensure Doherty behavior in both frequency bands.

4.1.2.1 Impedance inverter network

The IIN must function as a quarter wave impedance transformer, at the two frequency bands, independently of the termination impedance. Using a T- or a Π-network, shown in Fig. 4.4, an equivalent quarter-wave length TL of characteristic impedance $Z_0$ can be realized at two uncorrelated frequencies $f_1$ and $f_2$. Design equations for the T-network are derived in [126]. For the Π-network, a similar method to the one in [126] is used to derive the design equations. In the design equations for the T- and Π-networks, the integers $n$ and $m$ should be selected accounting for physical constraints, i.e. realizability and dimension of the resulting TLs. Moreover, depending on the chosen $n$ value, the phase response of the T- and Π-networks may be different at the two operating frequencies as shown in Table 4.1.

Fig. 4.4: Dual-Band impedance inverter network: a) T-network; b) Π-network.
Table 4.1: Phase shift introduced by the different structures of Fig. 4.4

<table>
<thead>
<tr>
<th></th>
<th>T - Shape n odd</th>
<th>T - Shape n even</th>
</tr>
</thead>
<tbody>
<tr>
<td>phase ((S_{21})@f_1)</td>
<td>-90°</td>
<td>-90°</td>
</tr>
<tr>
<td>phase ((S_{21})@f_2)</td>
<td>+90°</td>
<td>-90°</td>
</tr>
</tbody>
</table>

4.1.2.2 Impedance transformer network

The ITN is used to transform the output load (50 Ω) to the required resistance value, at the DPA common node (C.N.) as shown in Fig. 4.3. The T- and Π-networks used for the IIN can be used for the ITN as well. However, a much simpler transformer exists [127]. It is formed by two TLs, with characteristic impedances \(Z_1\), \(Z_2\) and electrical lengths \(\theta_1\), \(\theta_2\) as depicted in Fig. 4.5. It can achieve ideal impedance matching at any two arbitrary frequencies.

\[
\begin{align*}
& R_L' \\
& \downarrow \quad Z_1, \theta_1 \\
& Z_2, \theta_2 \\
& \uparrow & R_L \\
& \downarrow \quad R_0
\end{align*}
\]

Fig. 4.5: Dual-Band impedance transformer network. The load \(R_0\) is transformed to a resistance \(R_L\).

4.1.2.3 Input power splitter and phase compensation network

The Wilkinson divider [128] and the Branch-Line Coupler (BLC) [129] are the most used power dividers allowing an input power signal to be equally or unequally divided, to the output ports, while ensuring high isolation between the output ports. In principle, to create the dual-band dividers, the dual-band T- or Π-networks shown in Fig. 4.4 are used. The main difference between the two dividers is the phase relationship between the two output ports. The Wilkinson divides the output power in phase while the BLC introduces a 90° phase shift. The relative phase shifts between the signals of the two output ports of the different dual-band IPS are summarized in Table 4.2.

Table 4.2: Phase shift between the two output ports of the input power splitter

<table>
<thead>
<tr>
<th>Dual-Band IPS</th>
<th>Phase Difference</th>
<th>T - Shape n odd</th>
<th>T - Shape n even</th>
</tr>
</thead>
<tbody>
<tr>
<td>Wilkinson</td>
<td>Δϕ @ (f_1)</td>
<td>0°</td>
<td>0°</td>
</tr>
<tr>
<td></td>
<td>Δϕ @ (f_2)</td>
<td>0°</td>
<td>0°</td>
</tr>
<tr>
<td>Branch-Line</td>
<td>Δϕ @ (f_1)</td>
<td>-90°</td>
<td>-90°</td>
</tr>
<tr>
<td></td>
<td>Δϕ @ (f_2)</td>
<td>+90°</td>
<td>-90°</td>
</tr>
</tbody>
</table>
To ensure proper Doherty operation, the phase shift introduced at the two frequencies by the IIN has to be compensated by suitable IPS-PCN structure. If the IPS is realized through a BLC, then the PCN is directly integrated in this element, providing the correct output port connections. Conversely, if Wilkinson structure is adopted, then a suitable PCN is required at the input of the Auxiliary or Main amplifiers. In this case, the required PCN network can be realized by using one of the dual-band structures presented in Section 4.1.2.2.

4.1.2.4 Dual-Band DPA Topologies

In this section, the possible configurations to implement a dual-band DPA will be reviewed. Each configuration is selected so the structures adopted for the realization of the passive networks ensure in-phase addition of the output signals from the Main and Auxiliary amplifiers at the common node (C.N.). Referring to the data reported in Table 4.1 and Table 4.2, the possible configurations for realizing dual-band DPAs are summarized in Table 4.3.

<table>
<thead>
<tr>
<th>IPS</th>
<th>PCN</th>
<th>IIN</th>
</tr>
</thead>
<tbody>
<tr>
<td>Wilkinson</td>
<td>$T$, $\Pi$, or Wideband</td>
<td>$T$</td>
</tr>
<tr>
<td></td>
<td>$\Pi$ $(n$-odd$)$</td>
<td>$\Pi$ $(n$-odd$)$</td>
</tr>
<tr>
<td></td>
<td>$\Pi$ $(n$-even$)$</td>
<td>$\Pi$ $(n$-odd$)$</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Branch-Line</th>
<th>$T$</th>
<th>-</th>
<th>$T$</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$\Pi$ $(n$-odd$)$</td>
<td>-</td>
<td>$\Pi$ $(n$-even$)$</td>
</tr>
<tr>
<td></td>
<td>$\Pi$ $(n$-even$)$</td>
<td>-</td>
<td>$T$</td>
</tr>
<tr>
<td></td>
<td>Wideband</td>
<td>-</td>
<td>$\Pi$ $(n$-odd$)$</td>
</tr>
</tbody>
</table>

The configurations that most closely resembles the general topology shown in Fig. 4.3, are certainly the ones that require the presence of a dual-band Wilkinson input divider, two dual-band quarter-wave TLs to realize the IIN and the PCN, and a two-section transformer to realize the ITN. However, in this case the overall structure of the DPA is very cumbersome, due to the simultaneous presence of a dual-band Wilkinson divider and two impedance inverters. A more compact solution can be obtained by selecting the configurations adopting a Branch-Line splitter, since the phase relation of the outgoing signals from the Branch-Line avoids the need of the PCN at the input of the Auxiliary amplifier.

4.1.3 Multi-band branch-line couplers

To extend the presented dual-band approach into multi-band approach, the passive structures must be designed to operate simultaneously at multiple bands. In this thesis, we have made a step towards the design of multi-band DPAs in
the future by proposing a new design approach for multi-band BLCs. The single-band BLC is made of four quarter-wave TLs. Therefore, to obtain multi-band BLCs, the design of multi-band quarter-wave TLs must be considered first. These multi-band TLs can be used as well to realize the IIN and ITN in multi-band DPAs.

In [paper F], a closed-form design approach for multi-band BLCs for arbitrary operating at incommensurate frequencies is presented. The proposed method, presented hereafter, is validated by the design and implementation of dual-band, triple-band, and quad-band microstrip BLCs.

### 4.1.3.1 Design approach

The approach starts from the dual-band quarter-wave TL topology then it is extended to any number of arbitrary incommensurate bands. The Π-network, shown in Fig. 4.6, can reproduce, simultaneously at two arbitrary frequencies ($f_1$ and $f_2$), the behavior of a $\lambda/4$-TL having characteristic impedance $Z_T$ if [130]:

1. The electrical length of the series TL is $90^\circ$ at the center frequency, $f_c = (f_1 + f_2)/2$.

2. Its characteristic impedance ($Z_c$) and the shunting elements ($B_i$) match the following conditions:

$$Z_{c,i} = \frac{Z_T \sin \left( \frac{\pi}{2} \cdot \frac{f_i}{f_c} \right)}{\sin \left( \frac{\pi}{2} \cdot \frac{f_i}{f_c} \right)} \quad (4.1)$$

$$B_i = \frac{1}{Z_c \tan \left( \frac{\pi}{2} \cdot \frac{f_i}{f_c} \right)} \quad (4.2)$$

Since $Z_{c,1} = Z_{c,2}$ in (4.1), the parameter $Z_c$ in Fig. 4.6 is unique.

In case of three arbitrary frequencies ($f_1 < f_2 < f_3$), it is not possible to obtain a unique value for $Z_c$ from (4.1). For $f_c = (f_1 + f_3)/2$; the following values for $Z_c$ will be obtained:

$$Z_{c,1&3} = \frac{Z_T \sin \left( \frac{\pi}{2} \cdot \frac{f_1 + f_3}{f_c} \right)}{\sin \left( \frac{\pi}{2} \cdot \frac{f_1 + f_3}{f_c} \right)} \quad (4.3a)$$

$$Z_{c,2} = \frac{Z_T}{\sin \left( \frac{\pi}{2} \cdot \frac{f_2}{f_c} \right)} \quad (4.3b)$$
The best choice for $Z_c$ is an optimum value between $Z_{c,1&3}$ and $Z_{c,2}$ that allows equal scattering parameter magnitudes to be obtained for the network in Fig. 4.6 at the three frequencies. Therefore, the optimum value of $Z_c$ should verify the condition $|S_{11}(f_{1&3})| = |S_{11}(f_2)|$ for the network in Fig. 4.6. The derivation of the optimum value of $Z_c$, demonstrated in [paper F], leads to the following solution,

$$Z_c = \sqrt{Z_{c,1&3} \cdot Z_{c,2}} \quad (4.4)$$

The approach can be easily generalized for an arbitrary number, $N$, of uncorrelated frequencies (i.e. $f_1 < f_2 < \cdots < f_m < \cdots < f_N$). Selecting $f_c = (f_1 + f_N)/2$, $N - 1$ different values for $Z_c$ are obtained from 4.1: $\{Z_{c,1} = Z_{c,N}$, $Z_{c,2}$, $Z_{c,3}$, $\ldots$, $Z_{c,m}$, $\ldots$, $Z_{c,N-1}\}$ where $Z_{c,N}$ and $Z_{c,m}$ are the largest and smallest values among the available $Z_{c,i}$ values. By applying the same analysis applied in the case of three frequency bands, $Z_c$ becomes $Z_c = \sqrt{Z_{c,1&N} \cdot Z_{c,m}}$ and the same matching condition, $|S_{11}(f_{1&N})| = |S_{11}(f_m)|$, will be obtained at $f_1$, $f_N$ and $f_m$, where $f_m$ is the frequency corresponding to $Z_{c,m}$. The resulting value from $Z_c = \sqrt{Z_{c,1&N} \cdot Z_{c,m}}$ is closer to the remaining $Z_{c,i}$ at the other frequencies, hence, the expected matching condition at the other frequencies is better than the one achieved at $f_1$, $f_m$ and $f_N$.

In our design, we use the impedance buffer approach [87, 131], shown in Fig. 4.7, to realize the obtained susceptances $B_i$. Starting from the input port of the network (P1 in Fig. 4.7), the operating frequencies are controlled in descending order, i.e., from $f_N$ to $f_1$. The impedance buffers at $f_N$ ... $f_2$ are realized by quarter-wave open circuit stubs, while the one at $f_1$ is obtained with a ground connection to reduce the size of the structure.

The single-band BLC is obtained by properly combining four single-band quarter-wave TLs. To achieve the multi-band BLC topology, each quarter-wave TL of the single-band BLC has to be replaced with the multi-band equivalent one, following the design methodology described above.

### BLC circuit demonstrators

To verify the approach described above, the design of dual-, triple-, and quadband BLCs has been carried out. The realized multi-band BLCs are shown in Fig. 4.8, while their performance in terms of simulated (schematic and EM simulations) and measured S-parameters is reported in Fig. 4.9.

![Fig. 4.7: Ladder network obtained applying the Impedance Buffer Methodology to synthesize the $B_i$ susceptances for a multi-band quarter-wave transmission line.](image-url)
Fig. 4.8: Photos of the realized (a) dual-band, (b) triple-band and (c) quad-band branch line couplers, whose sizes are $65 \times 51 \text{ mm}^2$, $75 \times 82 \text{ mm}^2$ and $73 \times 70 \text{ mm}^2$, respectively. The network based on the Impedance Buffer Methodology that synthesizes the desired values of $B_i$ is highlighted in each figure by means of a white frame.

The performance of the three BLCs is degraded when passing from simulations with ideal elements to simulations with real elements. This can be attributed to the losses in microstrip lines and non-predicted behavior of actual cross/tee junctions. The measured results for the three BLCs, well in agreement with the theoretical and simulated ones, show satisfactory levels of matching, balance, and isolation at each of the operating bands. The results confirm the feasibility of the proposed design approach and highlights its usefulness for multi-band circuits and in particular for multi-band DPAs.

Fig. 4.9: Measured and simulated results of the (a) dual-band, (b) triple-band, and (c) quad-band branch line couplers.

A design example of dual-band DPA based on the proposed approach in section 4.1.2 is presented in the following.
4.2 Dual-band DPA circuit demonstrator

The design approach of dual-band DPAs is demonstrated through the design and implementation of a dual-band DPA operating at 1.8 GHz and 2.4 GHz. The DPA parameters have been theoretically inferred from the DC-IV curves of the device by applying the design approach in [24].

4.2.1 Dual-band Main PA design

The first step was to design the dual-band Main PA. Several concurrent dual-band PA architectures have been investigated and reported in recent years [132–136]. However, the design approach we use in our design is similar to the one proposed in section 2.2, but applied at the two operating frequencies. Load-pull/source-pull simulations were performed to find the optimum load and source impedances fulfilling the intrinsic load conditions at 1.8 GHz and 2.4 GHz, respectively. Harmonic load-pull/source-pull simulations were also performed to further improve the efficiency performance. The latter simulations showed that only the second harmonic at the output has big influence on the performance. Therefore, in the design of the input matching network, only the fundamental frequencies have been considered, while the fundamental and the second harmonic have been considered in the design of the output matching network. The Main PA, shown in Fig. 4.10, has been implemented and tested in [Paper E]. It has been characterized versus frequency for a fixed input power of 30 dBm. The measured peak PAE, shown in Fig. 4.11(a), is 64% in the two bands, with a measured output power of 42.3 dBm at 1.8 GHz and 42 dBm at 2.4 GHz. Fig. 4.11(b)

Fig. 4.10: Photo of the realized dual-band Main PA.

Fig. 4.11: Performance of the dual-band PA (a) Measured and simulated PAE and gain vs. frequency (b) Measured PAE and gain versus output power.
shows measured gain and PAE versus input power at 1.8 GHz and 2.4 GHz, respectively. It can be noticed the performance and behavior of the PA are similar in the two operating bands. The performance is in general very well predicted by the simulations, which is important when considering the use of this design in the more complex design of a dual-band DPA.

4.2.2 Dual-band DPA design

The same structure of the Main PA has been replicated for the Auxiliary PA and the remaining passive networks of the DPA have been designed. For the IIN, a Π-network with \( n = 3 \) has been adopted. For the IPS, a wideband topology [137] has been used to reduce the design sensitivity related to practical frequency shifts occurring in the realization of other passive networks. Moreover, the selected topology provides the same phase-shift introduced by the IIN at the two operating frequencies. Finally, the two section dual-band impedance transformer discussed in Sec. 4.1.2.1 is adopted for the ITN. A photo of the manufactured dual-band DPA is shown in Fig. 4.12.

![Photo of the implemented dual-band Doherty power amplifier.](image)

The simulated and measured drain efficiency and output power versus frequency of the DPA under a constant input power of 33 dBm, corresponding to saturated operation, are shown in Fig. 4.13(a). The measured measured drain

![Performance of the dual-band DPA (a) Measured and simulated drain efficiency and gain vs. frequency; (b) Measured PAE and gain versus output power at the two operating bands.](image)
efficiency is 69% at 1.8 GHz, 61% at 2.4 GHz while the output power is slightly higher than 43 dBm in the two bands. The measured power gain and PAE versus output power at the two operating bands are shown in Fig. 4.13(b). A correct Doherty behavior can be easily noticed at the two operating bands, where an almost constant high efficiency across OBO range of 6 dB is observed, in particular for the 1.8 GHz band. For the 1.8 GHz band, the measured PAE is 64% at an output power of 43 dBm, and 60% at an output power of 37 dBm (6 dB OBO). Similarly, for the 2.4 GHz band, 54% PAE is measured at 43 dBm output power, and 44% at 6 dB OBO. The gain compression in the Doherty region is limited to 1 dB for 1.8 GHz and 1.2 dB for 2.4 GHz.

4.2.3 Concurrent modulated measurements

Linearized concurrent dual-band modulated measurements were performed on both PAs. The linearization was performed with the 2-D-DPD presented in [89] and the memory polynomial model with nonlinear order 7 and memory depth 3 [57]. The concurrent signal used in the measurements consisted of 10 MHz LTE signal with 7 dB PAPR, and 10 MHz WiMAX signal with 8.5 dB PAPR.

In the experiment, the LTE signal is applied at 1.8 GHz band while the WiMAX signal is applied at the 2.4 GHz band. The measured output spectrum

![Fig. 4.14](image-url): Output signal spectrum in concurrent mode, without (w/o) and with (w) DPD, of (a) PA, 10MHz LTE at 1.8GHz, (b) PA, 10MHz WiMAX at 2.4GHz, (c) DPA, 10MHz LTE at 1.8GHz, (d) DPA, 10MHz WiMAX at 2.4GHz.
for both PAs at 1.8GHz and 2.4GHz, before and after DPD are shown in Fig. 4.14. Average output power, PAE, and ACLR, with and without DPD, are summarized in Table 4.4. These results are obtained for an average input power of 19dBm and 22dBm for the PA and the DPA, respectively.

Table 4.4: Measured average output power, average PAE and minimum ACLR level.

<table>
<thead>
<tr>
<th>Pout(dBm)</th>
<th>PAE(%)</th>
<th>ACLR(dBC)</th>
</tr>
</thead>
<tbody>
<tr>
<td>w/o DPD</td>
<td>w DPD</td>
<td>w/o DPD</td>
</tr>
<tr>
<td>PA</td>
<td>33.0</td>
<td>24.5</td>
</tr>
<tr>
<td>DPA</td>
<td>33.4</td>
<td>34.4</td>
</tr>
</tbody>
</table>

"w" and "w/o" refer to with and without, respectively.

4.2.4 Dual-band PA versus dual-band DPA

The advantages and the drawbacks of the DPA architecture compared to the single-ended dual-band PA are discussed in this section. This discussion is based on both continuous wave and modulated signal measurements performed on both PAs. The frequency response of the two PAs in terms of output power, gain, and PAE is compared in Fig. 4.15(a), while the performance of the two PAs at the two operating frequencies versus output power is compared in Fig. 4.15(b).

Fig. 4.15: Performance comparison of dual-band PA and dual-band DPA (a) Frequency sweep measurement (b) Power sweep measurement.
As expected, the output power of the DPA is higher than the one of the PA, due to the doubled active periphery. However, the gain of the DPA is lower because of the unequal division of the input power. Moreover, it can be noticed that the PA has similar performance in terms of output power and PAE at both operating bands, while the DPA presents a performance reduction at the higher band. This reduction can be attributed to the input/output combining networks of the DPA. The input/output combining networks of the DPA introduce greater complexity to the circuit and makes it more sensitive to the variations in the practical circuit realization. It is also important to note that despite that performance reduction, the bandwidth is not affected. In fact, similar levels of 1 dB gain ripple bandwidths have been registered at both bands for both PAs.

From the results summarized in Table 4.4, it can be noticed that standard DPD methods can be used to linearize the two PAs, and that the achieved linearity is independent from the architecture of the amplifier since similar ACLR levels have been registered from both PAs. However, the advantage of the DPA with respect to the PA can be noticed in terms of average PAE, where an improvement of 40% is registered for the same operating conditions.

### 4.2.5 Dual-band DPA performance comparison

Comparison between the performance of the presented DPA with recently published dual-band DPAs is summarized in Table 4.5.

<table>
<thead>
<tr>
<th>Reference</th>
<th>Freq(GHz)</th>
<th>Pout(dBm)</th>
<th>Gain(dB)</th>
<th>PAE(%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2010 [33]</td>
<td>2.14</td>
<td>33/39</td>
<td>6/5</td>
<td>33/35</td>
</tr>
<tr>
<td>2011 [89]</td>
<td>0.88</td>
<td>35/41</td>
<td>8/6</td>
<td>33/40</td>
</tr>
<tr>
<td>2011 [35]</td>
<td>2.00</td>
<td>36/42</td>
<td>10/5</td>
<td>44/48</td>
</tr>
<tr>
<td>2011 [138]</td>
<td>1.96</td>
<td>36/42</td>
<td>8/9</td>
<td>33/50</td>
</tr>
<tr>
<td>2012 [139]</td>
<td>0.92</td>
<td>35/41</td>
<td>8/9</td>
<td>33/41</td>
</tr>
<tr>
<td>[Paper G]</td>
<td>1.80</td>
<td>37/43</td>
<td>11/10</td>
<td>60/64</td>
</tr>
<tr>
<td>2010 [33]</td>
<td>3.50</td>
<td>–</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>2011 [89]</td>
<td>1.96</td>
<td>34/40</td>
<td>8/7</td>
<td>30/38</td>
</tr>
<tr>
<td>2011 [35]</td>
<td>2.72</td>
<td>36/42</td>
<td>10/5</td>
<td>40/30</td>
</tr>
<tr>
<td>2011 [138]</td>
<td>3.50</td>
<td>35/41</td>
<td>8/9</td>
<td>25/33</td>
</tr>
<tr>
<td>2012 [139]</td>
<td>1.99</td>
<td>34/41</td>
<td>6/5</td>
<td>29/32</td>
</tr>
<tr>
<td>[Paper G]</td>
<td>2.40</td>
<td>37/43</td>
<td>10/9</td>
<td>44/54</td>
</tr>
</tbody>
</table>

The presented dual-band DPA shows state-of-the-art results since it outperforms all the other published dual-and DPAs in terms of output power, gain, and PAE. These results demonstrate the usefulness of the proposed approach to implement highly efficient multi-band/multi-mode transmitters for current and future wireless communication systems.
Chapter 5

Conclusions and future work

5.1 Conclusions

This thesis presents various design techniques that improve bandwidth and efficiency characteristics of PAs used in wireless communication systems.

The design of high peak efficiency single-ended PAs is considered by proposing a new design procedure. The procedure is based on using a bare-die technique that eliminates the parasitics associated with the package of the transistor and an in-house model optimized for high efficiency switched-mode and harmonically tuned PAs. Moreover, MC and EM simulations are performed to ensure first-pass design. This procedure has been demonstrated by designing high efficiency PAs for S-band and C-band. The excellent results obtained demonstrate the success of the selected bare-die mounting, modeling, and circuit design methodologies used.

Then, two design techniques that extend the bandwidth of high efficiency PAs are presented. The first design technique is for single-ended PAs with octave bandwidth, while the second one is for push-pull PAs with bandwidth exceeding one octave. For the single-ended PA, the approach is based on a harmonically tuned approach to ensure high efficiency performance. Moreover, unlike most published work where matching networks are designed using optimization in a non linear circuit simulator, an extensive and systematic design procedure for broadband matching networks is explained and presented. The procedure has been demonstrated by implementing a hybrid high-efficiency octave bandwidth PA covering S-band. To extend the bandwidth to more than one octave, we investigated the potential of push-pull technique and in particular, we studied the influence of the even mode second harmonic impedance of the output balun on the push-pull PA performance. A prototype push-pull PA has been implemented with a balanced output and the output balun operation has been emulated by using a novel push-pull harmonic load-pull measurement setup that allows arbitrary balanced fundamental and second harmonic loads to be presented to the push-pull PA. The study shows that the performance of the PA is very dependent on the second harmonic even mode impedance of the output balun. The efficiency may be degraded up to 25% if improper
common mode harmonic impedances are presented by the balun. The approach
presented allows the PA and balun properties to be isolated from another and is
therefore an important tool for further understanding and optimization of PAs
and baluns for broadband push-pull microwave PAs.

The dual-band amplification of signals with high PAPR is considered by
proposing an extensive design procedure for highly efficient dual-band DPAs.
In particular, the procedure concentrates on the design of the passive structures,
presenting several possible topologies for the dual-band DPA. The procedure is
demonstrated by implementing a state-of-the-art dual-band DPA. The proposed
approach allows the design of efficient dual-band DPAs which can be very useful
in future wireless transmitters.

A step towards designing multi-band DPAs has been made in this thesis by
proposing a new method to design Multi-band BLCs. The complete theo-
retical analysis of the topology is derived, leading to a closed form equations
system for its design. Three couplers are implemented for dual-, triple-, and quad-
band operation to validate the methodology. The proposed couplers can be also
used in any multi-band microwave and millimeter-wave applications due to their
simple structure and the possibility to select arbitrary operating bands.

The proposed design techniques in this thesis provide the designers of PAs
with new concepts and thus lead to build new PAs with improved perfor-
mance in terms efficiency, energy consumption, and bandwidth for current and future
wireless systems. Finally, it is important to note that even though the focus
has been put on wireless communications, this work is very generic and can be
used for many other applications where high efficiency and/or wide bandwidth
is demanded.

5.2 Future work

The work presented in this thesis is in need of continued research. Here follows
a few ideas that can be subject to further research in the future:

**High efficiency power amplifiers** So far, the proposed approach, the
mounting technique and the optimized model of the transistor are tested up to
C-band. Therefore, it would be interesting to test the (frequency) limitations of
these techniques by designing and implementing hybrid and integrated PAs at
higher frequencies, i.e, X-band, for radar and microwave radio link applications.

**Wideband baluns** The design of broadband baluns is a significant chal-
lenge at microwave frequencies. In [Paper D], it is shown that baluns and in
particular their common mode response have big importance on the perfor-
mance of push-pull PAs. Therefore, it would be interesting to investigate and
design new broadband baluns with high common mode impedance to be used
in broadband push-pull PAs.

**Multi-band branch-line couplers** The theory presented in [Paper F] is
valid for equal amplitude coupler for all bands. Therefore, this work can be ex-
tended to find more generalized coupler design closed-form that allow un-equal
amplitude coupling for different bands.
Multi-band and wideband Doherty power amplifiers [Paper G] presents a general design approach for dual-band DPAs. This work can be extended to investigate the possibilities to design multi-band DPAs. However, if the number of bands increases, beyond three, the passive networks become very complicated and the design may not be practical. Therefore, designing wideband DPAs is also very important in order to know their limitations and hence, to realize when multiband versus wideband DPAs are giving the best performance.
Chapter 6

Summary of appended papers

Paper A

A Highly Efficient 3.5 GHz Inverse Class-F GaN-HEMT Power Amplifier

This paper presents the design of a highly efficient inverse class-F PA using bare-die GaN-HEMT device. A detailed circuit design methodology for inverse class-F PAs is presented and validated.

My contributions are: Design, simulations, implementation, measurement of the PA and writing of the paper.

Paper B

Highly efficient GaN-HEMT power amplifiers at 3.5 GHz and 5.5 GHz

This paper presents the design of two highly efficient harmonically tuned PAs using bare-die GaN-HEMT devices. The first PA is designed at 3.5 GHz while the second is designed at 5.5 GHz. This work was accomplished together with Hossein Mashad Nemati. The goal of this work was to explore the capabilities of the circuit design methodology presented in [Paper A] for high frequencies and to win the ‘High Efficiency Power Amplifier Design Competition’ of the IEEE Microwave Theory and Techniques Society (IEEE MTT-S).

My contributions are: Device modeling, design of the 5.5 GHz-PA, simulations, implementation, measurement of the 5.5 GHz-PA and writing of the paper.
CHAPTER 6. SUMMARY OF APPENDED PAPERS

Paper C

Design of a Highly Efficient 2-4 GHz Octave Bandwidth GaN-HEMT Power Amplifier

A design methodology for high-efficiency octave bandwidth PAs is presented. Moreover, a detailed method for the design of suitable broadband matching network solutions is derived analytically. The design approach is demonstrated by the design and implementation of a highly efficient 2-4 GHz octave bandwidth PA using bare-die GaN-HEMT device.

My contributions are: Circuit design technique, design, simulations, implementation, measurement of the PA and writing of the paper.

Paper D

Investigation of push-pull microwave power amplifiers using an advanced measurement setup

In this paper, we propose a push-pull harmonic load-pull measurement setup that allows the influence of the balun on push-pull PA performance to be investigated in detail under realistic operating conditions. A prototype wideband 1-3 GHz push-pull PA has been developed to investigate the influence of the balun characteristics on the overall PA characteristics.

My contributions are: Circuit design technique, design, simulations, implementation, measurement of the PA and writing of the paper.

Paper E

Concurrent Dual-Band GaN-HEMT Power Amplifier at 1.8 GHz and 2.4 GHz

The capabilities of the design methodology presented in Papers A and B are explored for dual-band PAs. This is demonstrated by the design of an efficient dual-band harmonically tuned GaN-HEMT PA at 1.8 GHz and 2.4 GHz.

This research was performed in close collaboration with the group of Prof. Paolo Colantonio at University of Rome Tor Vergata, where I spent six months during 2011.

My contributions are: Circuit design technique, design, simulations, implementation, measurement of the PA and writing of the paper.

Paper F

Design Method For Quasi-Optimal Multi-Band Branch-Line Couplers

In this paper, a closed form design approach for multi-band BLCs for arbitrary operating frequencies is presented. The circuit theory, including design equations and limitations of the approach are presented. The design approach is validated through the practical implementation of dual-, triple-, and quad-band microstrip BLCs.
This research was performed in close collaboration with the group of Prof. Paolo Colantonio at University of Rome Tor Vergata, where I spent six months during 2011.

My contributions are: Participation in theory and circuit analysis, design, simulations, implementation, and participation in the writing of the paper.

Paper G

Design of a Concurrent Dual-Band 1.8 GHz-2.4 GHz GaN-HEMT Doherty Power Amplifier

In this paper, a detailed design procedure for high efficiency dual-band DPA is presented. In particular, the design procedure concentrates on the design of the passive structures, presenting several possible topologies for the dual-band DPA. This is validated by successfully state-of-the-art experimental results of a dual-band DPA operating simultaneously at 1.8 GHz and 2.4 GHz.

This research was performed in close collaboration with the group of Prof. Paolo Colantonio at University of Rome Tor Vergata, where I spent six months during 2011.

My contributions are: Circuit design technique, design, simulations, implementation, measurement of the PA and writing of the paper.
Acknowledgment

I would like to thank all people who have helped and inspired me to make this thesis possible.

First I would like to thank my examiner Professor Herbert Zirath for giving me the opportunity to pursue my Ph.D study at the Microwave Electronics Laboratory. I would also like to thank my supervisors Docent Christian Fager and Dr. Kristoffer Andersson for their support, guidance, advices, encouragement, and the best of vision that they have provided me. The knowledge that I gained from them during lectures and during discussions is invaluable. In addition, a thank you to Professor Jan Grahn for all his support and for creating an amazing research environment within the GigaHertz Centre.

Thanks to Prof. Paolo Colantonio for hosting me in his group at the MIMEG Laboratory, University of Rome - Tor Vergata, as a visiting researcher in 2011. I really appreciate his support and guidance during the six-months period spent there. Many thanks also to researchers at the MIMEG Laboratory, especially Elisa Cipriani, Luca Piazzon, and Rocco Giofre for their help and hospitality during this period.

Thanks to my colleagues at the microwave electronics laboratory, especially to Hossein Mashad Nemati and Mattias Thorsell for their help and their support during my research. A special thank to Carl-Magnus Kihiman for manufacturing the mechanical fixtures for my circuits. Also, special thanks for Christer Andersson, David Gustafsson, Giuseppe Moschetti, Junghwan Moon, Mustafa Özen, Olle Axelsson, and Pirooz Chehrenegar for being good friends.

Most of all, I would like to thank my parents, my brothers, and my sisters who have shown great love and continuous support in every step of my life, I appreciate everything they have done for me.

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This research has been carried out in GigaHertz Centre in a joint project financed by the Swedish Governmental Agency for Innovation Systems (VINNOVA), Chalmers University of Technology, ComHeat Microwave AB, Ericsson AB, Infineon Technologies Austria AG, Mitsubishi Electric Corporation, NXP Semiconductors BV, Saab AB, and SP Technical Research Institute of Sweden.
Bibliography


Paper A

A Highly Efficient 3.5 GHz Inverse Class-F GaN HEMT Power Amplifier

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A highly efficient 3.5 GHz inverse class-F GaN HEMT power amplifier

PAUL SAAD, CHRISTIAN FAGER, HOSSEIN MASHAD NEMATI, HAIYING CAO, HERBERT ZIRATH AND KRISTOFFER ANDERSSON

This paper presents the design and implementation of an inverse class-F power amplifier (PA) using a high power gallium nitride high electron mobility transistor (GaN HEMT). For a 3.5 GHz continuous wave signal, the measurement results show state-of-the-art power-added efficiency (PAE) of 78%, a drain efficiency of 82%, a gain of 12 dB, and an output power of 12 W. Moreover, over a 300 MHz bandwidth, the PAE and output power are maintained at 60% and 10 W, respectively. Linearized modulated measurements using 20 MHz bandwidth long-term evolution (LTE) signal with 11.5 dB peak-to-average ratio show that $-42$ dBc adjacent channel power ratio (ACLR) is achieved, with an average PAE of 30%. $-47$ dBc ACLR with an average PAE of 40% are obtained when using a WCDMA signal with 6.6 dB peak-to-average ratio (PAR).

Keywords: Power amplifier, Inverse-F, GaN HEMT, Wideband, High efficiency

Received 16 December 2009; Revised 23 March 2010

1. INTRODUCTION

Due to the fast growing popularity of the wireless communication systems, high efficiency power amplifiers (PAs) have become one of the most important components in modern RF transmitters. Since high efficiency leads to lower power consumption, smaller battery size, and reduced cooling requirements, the efficiency has become one of the most important design parameters, not only for hand-held terminals where the power is generated from a limited power supply, but also for base station applications where it can reduce the amount of wasted energy [1].

By careful design of the transistor load network in the PA, it is possible to produce voltage and current waveforms that do not overlap. As a result, in these so-called switched mode power amplifiers (SMPAs), there is no power dissipation across the transistor and theoretically 100% efficiency is achieved [2]. In practical high-frequency SMPAs, however, the efficiency is degraded from 100% due to non-idealities of the components. Typical non-idealities are parasitic elements, finite on-resistance, non-zero transition time, and non-zero knee voltage.

Regarding the active device, silicon laterally diffused metal oxide semiconductor (Si LDMOS) has been the best candidate at frequencies around 1 GHz. However, its performance limited in the high-frequency region due to its relatively large output capacitance. Wide-bandgap devices such as gallium nitride high electron mobility transistor (GaN HEMT) overcome this problem and provide high electron mobility, high current density, and high breakdown voltage. The GaN HEMT has been addressed as a substitute for Si LDMOS [3, 4].

One specific type of SMPA that has recently attracted a lot of attention in high-frequency applications is the inverse class-F. Analysis and experiments, which demonstrated advantages of the inverse class-F amplifier, have been reported in [5–8].

Recently, we have presented in [9] state-of-the-art high-efficiency microwave PA which is based on the inverse class-F configuration. The design is based on a harmonic load-pull simulation approach and the design of a suitable matching network.

In this paper we present an extension of [9], where the model used has been presented and evaluated by comparing simulations with the measurement results. Moreover, the PA performance has been more investigated by performing more measurements like large signal return-loss and modulated measurements using different types of signals.

Comparisons between the performance of the presented PA with state-of-the-art results for GaN PAs are summarized in Table 1. The outstanding performance of the PA presented verifies the success of the design procedure adopted.

This paper is organized as follows. Section II gives a brief overview of inverse class-F PAs. An overview of the transistor model and the design procedure used for the PA is given in Section III. The implementation of the PA and the measurement results are presented in Section IV and finally conclusions are given in Section V.

II. INVERSE CLASS-F PAS

All high-efficiency PAs are based on careful control of the harmonic content of the voltage and current waveforms at the transistor intrinsic terminals. The construction of an ideal inverse class-F PA consists in imposing a square and half-sinusoidal waveform for drain-current and drain-to-source voltage, respectively. Figure 1 presents the drain-current and drain-to-source voltage waveforms.
These idealized waveforms are obtained by control of the transistor load impedance at different harmonics. The optimum resistive load impedance must be matched to the system impedance ($Z_c$) at the fundamental frequency. Moreover, the output impedance seen by the device at even harmonics has to be open circuited because the half sine voltage wave only consists of even harmonics. On the other hand, all odd harmonic impedances must be short circuited in order to approximate a square drain current. According to \cite{17}, the second, $2f_0$, and third, $3f_0$, harmonics are most important for high-efficiency operation. In \cite{18}, it is shown that controlling these two harmonics is usually enough in practical microwave PAs. Furthermore, controlling more harmonics increases circuit complexity without necessarily improving the performance \cite{19}. On the contrary, manipulation of excessive harmonics may reduce the bandwidth of the PA. Thus, close to optimal, load impedances are given by:

\begin{align}
Z_L(f_0) &= Z_{opt}, \quad (1) \\
Z_L(2f_0) &= \infty, \quad (2) \\
Z_L(3f_0) &= 0, \quad (3)
\end{align}

where $f_0$ is the fundamental frequency and $Z_{opt}$ is the optimal load impedance at the fundamental frequency.

### III. DESIGN METHODOLOGY

In order to reduce the parasitics of the package and facilitate harmonic impedance optimization at the transistor output reference plane, a bare-die, Cree CGH60015DE GaN HEMT is used. In SMPAs and harmonically tuned amplifiers, the transistor operates in the on- and off-regions. A simplified transistor model optimized for this type of operation is developed and used in the PA design. The model is based on simplified expressions for the nonlinear currents and capacitances where focus is put on accurately predicting the high efficiency, on- and off-regions of the transistor characteristics. The model allows the intrinsic waveforms to be studied in the PA design and therefore allows a careful investigation of the transistor operation. More details about the modeling approach used are given in \cite{20}. In contrast to the model in \cite{20}, where an LDMOS model was used, diode models are added in this case to accurately predict forward gate voltage and negative drain voltage conditions of a GaN transistor. The topology of this model is shown in Fig. 2.

![Fig. 1. Current and voltage waveforms for an ideal inverse class F PA.](image1)

![Fig. 2. Large signal GaN HEMT equivalent circuit model.](image2)
The first step to design the PA was to find the optimum input and output load conditions to maximize the output power and efficiency of the transistor. The procedure for optimization of the fundamental and harmonic impedances is summarized as below:

1) Perform a fundamental load-pull/source-pull simulation to find the optimum fundamental load and source impedances for efficiency and output power.

2) Using the impedances found in the previous step, a harmonic load-pull simulation was performed to find the optimum second and third harmonic load and source impedances for high-efficiency operation. The obtained optimum source and load impedances at fundamental, second, and third harmonics that maximize the power-added efficiency (PAE) are shown in Fig. 3.

Figure 4 shows the simulated intrinsic drain voltage and current waveforms of the transistor, corresponding to 80% PAE. The drain voltage waveform is a half-sinusoid whereas the drain current waveform is close to a square wave, which corresponds to the inverse class-F waveforms shown in Fig. 1.

The circuit diagram of the designed inverse class-F PA is depicted in Fig. 5. The space between the bonding pads on the chip and the PCB lines is reduced as much as possible in order to avoid narrow-band and therefore sensitive harmonic matching. $L_{bwg}$ and $L_{bwd}$ are used in the circuit design to model the input and output bondwire inductances, respectively. Their values are estimated to 0.15 nH.

The input matching network consists of transmission lines $T_{Li}$, $i = 1...5$, which are optimized to provide, at the input of the device, the optimum impedances obtained from the source/load pull simulations, see Fig. 3.

The input matching network has been slightly modified in order to stabilize the PA. The Rollet stability factor ($k$) of the amplifier can be improved by increasing the real part of $Z_{11}$ [21]:

$$k = \frac{2\text{Re}(Z_{11})\text{Re}(Z_{12}) - \text{Re}(Z_{12}Z_{11})}{|Z_{12}Z_{11}|}.$$ 

A 39 Ω series resistance $R_g$ is therefore added at the input of the amplifier to improve the stability in the high-frequency band. Further improvement in the amplifier stability in the low-frequency band can be achieved by reducing the low-
frequency gain. The parallel resistance $R_{g3}$, set to 400 $\Omega$, increases low-frequency stability by reducing the input impedance.

The output matching network consists of transmission lines $T_{Li}$; $i=6...11$, which provides the optimum fundamental, second and third harmonics load impedances at the output of the device.

The values of the inductors $L_g$ and $L_d$ are equal to 28 and 8 nH, respectively. They are used to prevent the leakage of RF into the DC supply lines. The circuit was optimized for wideband operation to minimize the impact of mounting and manufacturing tolerances. It is important to note that the original design did not change significantly after the optimization.

Finally, Monte-Carlo simulations have been used to study the impact of components variability and uncertainty on the PA performance. Uncertainties introduced by the manufacturing process and the lumped components have been considered. The Monte-Carlo simulations have shown that the design is robust and not very sensitive to these variations.

IV. IMPLEMENTATION AND MEASUREMENT RESULTS

The inverse class-F PA was implemented on a Rogers 5870 substrate with $\varepsilon_r = 2.33$ and thickness of 0.8 mm. Figure 6 shows a picture of the fabricated inverse class-F amplifier using the bare-die GaN HEMT device.

The implemented PA has been characterized by large signal and modulated measurements to study its performance.

A) Large signal measurements

All measurements were made using a continuous wave input signal generated by an Agilent E4438C microwave synthesized source boosted by a microwave driver amplifier and the relevant power levels were measured by a power meter (Agilent E4419B). A low-pass filter with cut-off frequency of 6 GHz has been added at the output of the PA to filter out the power at the harmonics. Hence, only the power at the fundamental frequency have been measured and used in evaluating the PA performance.

First the bias sensitivity was investigated by a gate bias, $V_{GS}$ sweep. Figure 7 shows simulated and measured output power, $P_{out}$ and PAE versus $V_{GS}$. The measurements show that the performance of the PA is not very sensitive to the gate voltage. Results of the drain voltage, $V_{DS}$, sweep using 29 dBm input power are shown in Fig. 8. It can be noticed that the output power can be further increased by increasing $V_{DS}$. The measured results agree well with simulations when the input drive level is high enough. From Figs 7 and 8 we conclude that the optimum bias for the PA is $V_{DS} = 28$ V and $V_{GS} = -2.5$ V.

A power sweep measurement has been performed at 3.5 GHz. The simulated and measured output powers versus input power are shown in Fig. 9. As expected, good agreement between simulation and measurement results is obtained at high power levels, where the transistor is operated in a high-efficiency mode that the model was optimized for. The peak power level at the output of this amplifier is about 41 dBm or 12 W. Figure 10 shows the simulated and measured gain and PAE versus input power. A peak PAE of 78% is measured for an input drive level of 29 dBm. There is a good agreement between the simulated and measured results close to the peak efficiency operation.

The poor agreement between simulations and measurements at low input powers in Figs 9 and 10 is due to the fact that as the input power is reduced and the device is less overdriven, the harmonic contents of its output waveforms...
are no longer strong enough to be able to form high-efficiency switching conditions. Therefore, the device operation extends outside of the region where the model is optimized and the simulation results start to deviate from measurements. This is a fact that the PA designer should be aware of. The model is mainly optimized for switched mode or harmonically tuned overdriven operations where conventional models lack accuracy and fail to provide convergence in simulations.

The PA has been characterized versus frequency from 3 to 4 GHz, with a 29 dBm fixed input power drive level. The PAE and gain of the PA are plotted in Fig. 11 and compared with simulations. A good agreement between simulation and measurements is observed at the PA operation frequency. A maximum gain and PAE of 12 dB and 78%, respectively, are located at 3.5 GHz corresponding to a drain efficiency of 82% at this frequency. The amplifier exhibits higher than 50% PAE between 3.32 and 3.72 GHz, which corresponds to greater than 10% fractional bandwidth.

Input return loss have finally been measured under large signal conditions using 29 dBm input power, in the frequency band 3 – 4 GHz. Simulated and measured input return loss are shown in Fig. 12, a return loss of 14 dB is obtained at 3.5 GHz and agrees well with simulations.

B) Modulated measurements

Modulated measurements are used to evaluate the performance of the PA and show that the PA is linearizable to meet modern wireless communication system standards. In the experiment, a 20 MHz long-term evolution (LTE) signal with 11.2 dB peak-to-average ratio (PAR) and a 5 MHz WCDMA signal with 6.6 dB PAR are used. A relatively low average efficiency is expected when such signals with high PAR are used since the PA has to operate at large back-off most of the time.

The digital-predistortion (DPD) used, for both LTE and WCDMA signals, is the memory polynomial model with non-linear 11 and memory depth 5 [22]. The measured output spectrum at 3.5 GHz of the LTE signal, before and after DPD for an average input power of 18 dBm, is shown in Fig. 13.
The adjacent channel power ratio (ACLR) of the PA without DPD reaches $-32$ dBc with an average PAE of 35% whereas the ACLR of the PA with the DPD applied reaches $-42$ dBc at an average PAE of 30%.

Figure 14 shows the measured output spectrum at 3.5 GHz of the WCDMA signal before and after DPD. In this measurement the average input power used is 19.4 dBm, so the PA was operating at 9.6 dB back-off. When the DPD is applied, the average PAE is decreased from 45 to 40% while 13 dB improvement in ACLR, from $-34$ to $-47$ dBc, is obtained.

Average PAE and ACLR without DPD for WCDMA and LTE signals are displayed versus average output power in Fig. 15.

V. CONCLUSIONS

In this paper, a high-efficiency inverse class-F PA using a GaN HEMT has been presented. The design methodology is based on load-pull/source-pull and harmonic load-pull simulations. A bare-die device, instead of a packaged transistor, is used to minimize the influence of parasitics and therefore take full advantage of recent device technology improvements. The peak PAE of 78% with a power gain of 12 dB was achieved at an output power of 41 dBm at 3.5 GHz. A very broadband performance, with a power gain over 10 dB and PAE over 60%, was maintained over 300 MHz bandwidth. When DPD is used, modulated measurements demonstrate an average PAE of 30% and ACLR of $-42$ dBc for LTE signal. For WCDMA signal ACLR of $-47$ dBc and average PAE of 40% were obtained. These results represent state-of-the art for GaN PAs in this frequency range and demonstrate the success of the selected bare-die mounting, modeling, and circuit design methodologies used.

ACKNOWLEDGEMENTS

This research has been carried out in GigaHertz Centre in a joint project financed by the Swedish Governmental Agency for Innovation Systems (VINNOVA), Chalmers University of Technology, ComHeat Microwave AB, Ericsson AB, Infineon Technologies Austria AG, Mitsubishi Electric Corporation, NXP Semiconductors BV, Saab AB, and SP Technical Research Institute of Sweden.

REFERENCES


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Hossein Mashad Nemati was born in Tehran, Iran, in 1980. He received his B.Sc. degree in telecommunication engineering from Amirkabir University of Technology, Tehran, Iran, in 2004, the M.Sc. degree in microwave electronics from Chalmers University of Technology, Gothenburg, Sweden, in 2006, and is currently working toward the Ph.D. degree at the Microwave Electronics Laboratory, Chalmers University of Technology. His research interests are high-efficiency PAs and transmitter architectures. Mr. Nemati was the recipient of the 2008 Outstanding Achievement Award of the Student High Efficiency Power Amplifier Design Competition of the IEEE Microwave Theory and Techniques Society (IEEE MTT-S) International Microwave Symposium (IMS).

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Kristoffer Andersson (S’03–M’06) received the M.Sc. and Ph.D. degrees in electrical engineering from Chalmers University of Technology, Göteborg, Sweden, in 2001 and 2006, respectively. His research interests are in the area of characterization and modeling of wide-bandgap transistors.
Paper B

Highly efficient GaN-HEMT power amplifiers at 3.5 GHz and 5.5 GHz

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*IEEE Wireless and Microwave Technology Conference (WAMICON), April, 2011.*
Highly Efficient GaN-HEMT Power Amplifiers at 3.5 GHz and 5.5 GHz

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Abstract—This paper reports the design, implementation, and characterization of two high efficiency GaN-HEMT power amplifiers (PAs) at 3.5 GHz and 5.5 GHz. A bare-die approach is used to eliminate package parasitics in conjunction with an in-house transistor model that enables investigation of the transistor intrinsic waveforms. With this as a basis, harmonic source-pull/load-pull simulations have been used to design and implement two state-of-the-art highly efficient harmonically tuned PAs. For the 3.5-GHz PA, large-signal measurement results show a PAE of 80%, a power gain of 15.5 dB, and an output power of 7 W, while for the 5.5-GHz PA, 5.6 W output power, 12.5 dB power gain, and 70% PAE are achieved.

Keywords—power amplifier (PA); gallium nitride (GaN); high electron mobility transistor (HEMT); power-added efficiency (PAE); harmonic termination.

I. INTRODUCTION

Power amplifiers are typically the most power consuming circuit blocks in wireless systems. Improvement of power amplifier efficiency is therefore very important since it translates into lower power consumption, less cooling requirements, and reduced cost in RF front-ends. Harmonically tuned and switched-mode PAs (SMPAs) such as class-E, -D, -F, -F, -J, have been presented in literature in order to achieve theoretical efficiencies of up to 100%. They are based on careful control of the harmonic content of the voltage and current waveforms at the transistor intrinsic terminals. Thus, the load network at the output terminal of the transistor is designed to minimize the intrinsic voltage/current overlap [1]–[3].

Several factors are crucial for a successful practical design of high-efficiency PAs at high frequencies. One key factor is the power transistor technology. Recently, GaN-HEMT transistors are attracting much attention due to their high breakdown voltage and high power density. They offer an order of magnitude improved RF output power compared to traditional devices based on silicon (Si) and gallium arsenide (GaAs) [4]. Moreover, the low output capacitance of GaN devices offer possibility for high frequency designs [5]; in contrast with LDMOS devices which are limited at frequencies around 1 GHz due to their large output capacitances. Other factors which are particular critical for simulation-based design of hybrid PAs are the transistor mounting technique, transistor modeling, and the circuit design methodology [6], [7].

All these requirements make the PA design challenging at high frequencies and explain why very few results have been presented with discrete, high power devices, for frequencies higher than 3 GHz.

Recently, we have presented in [6] and [7] a successful design methodology for the design of high efficiency microwave PAs. In this paper, we are exploring the high frequency capabilities of the design methodology using better devices. This is demonstrated by the design of two harmonically tuned GaN-HEMT PAs at 3.5 GHz and 5.5 GHz. The performance of the PAs is summarized in Table I, where they are compared with other recently published results at similar frequencies. The state-of-the-art performances achieved in this paper demonstrate that the dedicated transistor mounting, modeling, and design techniques employed in this paper allow the potential of high performance GaN transistors to be fully exploited in design of high efficiency PAs.

II. DESIGN METHODOLOGY

In both PA designs, the 2.5mm GaN bare-die device, TGF2023-02 from Triquint Semiconductors, Inc. has been used. The drain-source breakdown voltage of the device is around 120V, the pinch-off voltage around -3.6V, and the saturation drain current is approximately 2.5A.

The design procedure will be presented only for the 5.5-GHz PA, but is analogous for the 3.5-GHz PA. The high frequencies used in these designs make any parasitics detrimental to the performance and must therefore be minimized.

<table>
<thead>
<tr>
<th>Reference</th>
<th>Freq(GHz)</th>
<th>Pout(W)</th>
<th>Gain(dB)</th>
<th>PAE(%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2008 [8]</td>
<td>3.5</td>
<td>11</td>
<td>10</td>
<td>72</td>
</tr>
<tr>
<td>2009 [9]</td>
<td>3.5</td>
<td>4</td>
<td>10</td>
<td>58</td>
</tr>
<tr>
<td>2009 [7]</td>
<td>3.5</td>
<td>12</td>
<td>12</td>
<td>78</td>
</tr>
<tr>
<td>This work</td>
<td>3.5</td>
<td>7</td>
<td>16</td>
<td>80</td>
</tr>
<tr>
<td>2006 [10]</td>
<td>5.5</td>
<td>3</td>
<td>6</td>
<td>45</td>
</tr>
<tr>
<td>2010 [12]</td>
<td>5.7</td>
<td>4</td>
<td>6</td>
<td>30</td>
</tr>
<tr>
<td>This work</td>
<td>5.4</td>
<td>4</td>
<td>13</td>
<td>70</td>
</tr>
</tbody>
</table>
Two of the most important transistor parasitics, the lead inductances and tab capacitances associated with transistor packages have in our work been eliminated by using a bare-die mounting approach. The bare-die transistor chip is mounted to the PA fixture and connected directly to the printed circuit boards (PCBs) using wire bonding. The chip and PCB surfaces have been carefully aligned to minimize the bond wire lengths [6], [7].

In SMPAs and harmonically tuned amplifiers, the transistor operates in the on- and off-regions. An in-house model optimized for high efficiency operation is developed for the bare-die transistor. The extracted model is based on simplified expressions for the nonlinear currents and capacitances where focus is put on accurately predicting the high efficiency regions of the transistor characteristics [6]. The model has been extracted from DC- and S-parameter measurements referred to the die surface reference plane using methods in [6]. Moreover, the model permits the intrinsic waveforms to be inspected during simulations and therefore allows a careful study of the transistor operation which is usually not possible with commercial models.

The same model topology has been successfully used for the design of high efficiency LDMOS [6] and GaN [7] PAs. The large signal GaN-HEMT equivalent circuit model is shown in Fig. 1. Using the developed model and the bare-die design method, the first step to design the PA is to perform load-pull/source-pull simulations at the die reference plane in order to find the fundamental load and source impedances maximizing the efficiency. Using these impedances, harmonic load-pull simulations were performed to find the second and third harmonic load and source impedances that further improve the efficiency. The simulations verified that the effect of the third harmonic on the efficiency is very small. The obtained optimum source and load impedances at fundamental and second harmonic that maximize the PAE are shown in Fig. 2.

The circuit diagram of the designed 5.5GHz power amplifier is shown in Fig. 3. The input matching network consists of transmission lines TL_i; i = 1..5; designed to provide the optimum fundamental and second harmonic impedance to the device input. The series resistance R_g2 is added at the input of the amplifier to improve the stability in the high frequency band while the parallel resistance R_g3 and R_g4 are added to reduce the low frequency gain and therefore improve the stability in the low frequency band. The output matching network consists of transmission lines TL; i = 6..11, which provides the optimum fundamental and second harmonic load impedance at the output of the device. L_bwg and L_bwd model the input and output bondwire inductances respectively. Their values are estimated to 0.15 nH. The inductors L_g and L_d are used to prevent the leakage of RF into the DC supply lines.

The simulated intrinsic waveforms of the 3.5-GHz and 5.5-GHz PA are shown in Fig. 4 and Fig. 5 respectively. These waveforms correspond to 83% and 75% simulated PAE for the 3.5-GHz and 5.5-GHz PAs respectively. Investigation of the waveforms confirm that the voltage/current overlap is minimized which explains the high efficiency obtained. Moreover, the simulations verify that the peak voltage is below the breakdown of the device.

![Figure 1. Large signal GaN-HEMT equivalent circuit model.](image1)

![Figure 2. Simulated optimum impedances at the transistor reference plane for maximum PAE.](image2)

![Figure 3. Circuit topology of the 5.5-GHz PA.](image3)
The PAs were implemented on a Rogers 5870 substrate with \( \varepsilon_r = 2.33 \) and thickness of 31mil. Fig. 6 shows a picture of the fabricated PAs using the bare-die GaN-HEMT device. Please note the aluminum fixture ridge, onto which the bare die device was attached. The gold plated input and output PCBs were attached separately on each side of the ridge and connected to the device using multiple bond wires. Moreover, no post-production tuning was used. The performance of the implemented PAs has been evaluated by means of large signal measurements. Continuous wave (CW) input signals have been generated by a microwave synthesized source (Agilent E4438C) boosted by a microwave driver amplifier and the output power levels were measured by a power meter (Agilent E4419B). A 6 GHz low-pass filter was connected at the output of the PAs to prevent harmonics from affecting the power measurements. The chosen dc bias for the gate is \( V_{GS} = -3.8 \text{ V} \) and the drain bias is set to \( V_{DS} = 34 \text{ V} \).

The 3.5-GHz PA has been characterized versus frequency between 3.3 GHz and 3.66 GHz, with a 22 dBm fixed input power drive level. The frequency sweep measurement results, depicted in Fig. 7, show that 15.5 dB gain and 80% PAE are obtained at 3.5 GHz. The amplifier exhibits higher than 50% PAE between 3.35 GHz and 3.65 GHz, which corresponds to 9% fractional bandwidth. The same characterization has been performed for the 5.5-GHz PA between 5.2 GHz and 5.8 GHz with 25 dBm input power drive level. The results, presented in Fig. 8, show that a maximum gain of 12.5 dB is located at 5.42 GHz with a corresponding 70% PAE and 6% fractional bandwidth is obtained around 5.45 GHz.

For both PAs we notice that the agreement between simulations and measurements is good and the center frequency is accurately predicted by the simulations. Fig. 9 shows measured gain and PAE versus output power for the 3.5-GHz and the 5.5-GHz PAs. The power sweep measurement is done at 3.5GHz for the former and at 5.4 GHz for the latter. The output power compresses at 39 dBm and the PAE reaches 80% for the 3.5-GHz PA while 70% PAE and 38 dBm compressed output power are obtained for the 5.5-GHz PA.
IV. CONCLUSION

In this paper, two high efficiency harmonically tuned power amplifiers using a GaN-HEMT have been presented. Using bare-die devices, the in-house optimized transistor model for harmonically tuned PAs and the design approach based on harmonic load-pull/source-pull simulations have allowed the realization of high performance PAs at 3.5 GHz and 5.5 GHz. The former showed a power gain of 15.5 dB, peak PAE of 80% and an output power of 38.7 dBm, while the latter showed 12.5 dB gain, 80% peak PAE and 37.5 dBm output power. These results represent state-of-the art for GaN PAs in S- and C-bands and demonstrate the success of the selected bare-die technique, modeling, and circuit design methodologies used.

ACKNOWLEDGMENT

This research has been carried out in GigaHertz Centre in a joint project financed by the Swedish Governmental Agency for Innovation Systems (VINNOVA), Chalmers University of Technology, ComHeat Microwave AB, Ericsson AB, Infineon Technologies Austria AG, Mitsubishi Electric Corporation, NXP Semiconductors BV, Saab AB, and SP Technical Research Institute of Sweden.

REFERENCES

Paper C

Design of a Highly Efficient 2-4 GHz Octave Bandwidth GaN-HEMT Power Amplifier

Paul Saad, Christian Fager, Haiying Cao, Herbert Zirath and Kristoffer Andersson

Design of a Highly Efficient 2–4-GHz Octave Bandwidth GaN-HEMT Power Amplifier

Paul Saad, Student Member, IEEE, Christian Fager, Member, IEEE, Haiying Cao, Student Member, IEEE, Herbert Zirath, Senior Member, IEEE, and Kristoffer Andersson, Member, IEEE

Abstract—In this paper, the design, implementation, and experimental results of a high-efficiency wideband GaN-HEMT power amplifier are presented. A method based on source–pull/load–pull simulation has been used to find optimum source and load impedances across the bandwidth and then used with a systematic approach to design wideband matching networks. Large-signal measurement results show that, across 1.9–4.3 GHz, 9–11-dB power gain and 57%–72% drain efficiency are obtained while the corresponding power-added efficiency (PAE) is 50%–62%. Moreover, an output power higher than 10 W is maintained over the band. Linearized modulated measurements using a 20-MHz long-term evolution signal with 11.2-dB peak-to-average ratio show an average PAE of 27% and 25%, an adjacent channel leakage ratio of $-44$ and $-42$ dBc at 2.5 and 3.5 GHz, respectively.

Index Terms—GaN HEMT, high efficiency, octave bandwidth, power amplifier (PA), wideband matching networks.

I. INTRODUCTION

In modern and future wireless communications systems, the increasing number of frequency bands and spectrum fragmentation require the development of circuits and subsystems having broadband capabilities. From the transmitter point of view, the power amplifier (PA) is the most critical component since its performance strongly influence the overall system features in terms of bandwidth, output power, efficiency, and operating temperature. This makes wideband PAs that cover many frequency bands while maintaining high efficiency an important research topic.

Thus far, the most popular technique to design broadband amplifiers is the distributed or traveling-wave amplifier approach [1]–[3]. In this case, a linear design method is used that ensures linearity, flat gain, and high return loss over the whole band [4], [5]. However, the drawback of this approach lies in the high number of devices used to achieve the same gain as a single device, and therefore, it results in high cost, large size, and low-efficiency levels.

The efficiency may be improved by using harmonically tuned PAs such as class J or F [6], [7] or switched-mode power amplifiers (SMAs) like class E, D, or inverse-F [6], [8]. However, such amplifiers are commonly used for narrowband applications with up to 10% fractional bandwidth. For wideband PAs, with octave or larger bandwidths [9], the harmonic tuning approach cannot be used because harmonics fall inside the required bandwidth.

Therefore, high-efficiency wideband PAs reported in the literature have a bandwidth of less than one octave [10]–[12]. Their designs are based on approximated switch mode and harmonics tuning strategies. However, they do not present any general method or analytical derivation for the design of the wideband matching networks used.

In this paper, the design of a high-efficiency octave bandwidth PA is presented. The design is based on a source–pull/load–pull simulation approach together with a detailed method for the design of suitable broadband matching network solutions. Comparison between the performance of the presented PA with state-of-the-art results for high-efficiency wideband PAs are summarized in Table I. The comparison shows the excellent performance of the designed PA and thereby demonstrates the usefulness of the proposed approach for the design of wideband PAs for future wireless systems combining wide bandwidth with high efficiency and linearity.

This paper is organized as follows. In Section II, the characterization and modeling of the bare-die device is presented together with the PA design strategy. An extensive design procedure for the wideband matching networks is presented in Section III. The PA topology and its implementation are presented in Section IV, while experimental results in terms of bandwidth, output power, and efficiency are shown in Section V. Conclusions are then given in Section VI.
II. DEVICE MODEL AND PA DESIGN APPROACH

A. Device Model

A 3.6-mm GaN bare-die device, Cree CGH60015DE, has been used for the PA design. The device has a breakdown voltage of around 100 V, a pinch-off voltage around −3 V, and the saturation drain current is approximately 2.3 A.

In order to minimize the effects of package and mounting parasitics, a bare-die mounting technique has been used. The transistor has been characterized with dc and bias-dependent S-parameters using the procedure in [15]. A switch mode optimized transistor model has been extracted from these measurements [15]. The model is based on simplified expressions for the nonlinear currents and capacitances where focus is put on accurately predicting the high-efficiency regions of the transistor characteristics. In contrast to most commercial models that only offer terminal voltages and currents, the model allows the intrinsic waveforms to be studied directly in a computer-aided design (CAD) tool, and therefore, allows a careful investigation of the transistor operation. Details about the modeling approach are given in [15]. In the model, diode models (D1 and D2) are added to accurately predict forward gate voltage and negative gate–drain voltage conditions. The model has been successfully used for the design of high-efficiency narrowband LDMOS [15] and GaN [16] PAs.

B. PA Design Approach

The first step to design the 2–4-GHz wideband PA was to find the optimum source and load impedances that maximize the performance of the device in terms of efficiency in the required bandwidth. Load–pull/source–pull simulations have therefore been performed using the large-signal transistor model developed. Fig. 1 shows the optimum impedances at several frequencies within the required bandwidth. The associated maximum PAE at each of those frequencies is listed in Table II.

A challenging task resides in the design of broadband matching networks that present those impedances at input and output of the device for each frequency. Noticing that the optimum impedances for this device are relatively close to each other across the band, new load–pull/source–pull simulations have been performed at 2, 2.5, 3.5, and 4 GHz. In this case, the source and load impedances that were optimum at 3 GHz were fixed and used for all frequencies. The simulation results listed in Table II show an acceptable degradation of less than 8% in power-added efficiency (PAE). The task can therefore be simplified to make the device see $Z_{S,3 \text{ GHz}} = 11.6 + j6.7 \Omega$ and $Z_{L,3 \text{ GHz}} = 10.4 + j15 \Omega$ at its input and output, respectively, across the entire bandwidth.

C. Influence of Second Harmonic Impedance

A careful control of the second-harmonic termination at the output of the device is critical for the resulting efficiency. However, second harmonic tuning requires additional design efforts. In the previous simulations of the PAE, the second harmonic was not optimized and it was assumed to be open circuit. While the device see the optimum impedances $Z_{S,3 \text{ GHz}}$ and $Z_{L,3 \text{ GHz}}$ at the fundamental, the impedance of the second harmonic has been varied across the periphery of the Smith chart in order to study its influence on the performance of the PA. Fig. 2 shows the PAE of the device versus the phase of the unity magnitude second harmonic reflection coefficient.

### Table II

<table>
<thead>
<tr>
<th>Freq</th>
<th>$\text{PAE}_{Z(f)}$ (%)</th>
<th>$\text{PAE}_{Z(f=3\text{GHz})}$ (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.0 GHz</td>
<td>80%</td>
<td>73%</td>
</tr>
<tr>
<td>2.5 GHz</td>
<td>70%</td>
<td>75%</td>
</tr>
<tr>
<td>3.0 GHz</td>
<td>78%</td>
<td>78%</td>
</tr>
<tr>
<td>3.5 GHz</td>
<td>80%</td>
<td>76%</td>
</tr>
<tr>
<td>4.0 GHz</td>
<td>80%</td>
<td>72%</td>
</tr>
</tbody>
</table>

![Fig. 1. Efficiency optimized source and load impedances.](image1)

![Fig. 2. Simulated PAE versus phase of the unity magnitude second harmonic reflection coefficient.](image2)
III. DESIGN OF BROADBAND MATCHING NETWORKS

From the output, the transistor can be approximated by an ideal current source with a parallel $R - C$ network, where $R$ is the source resistance corresponding to the PA load line resistance and the capacitance is the total drain–source capacitance. The main goal of the matching network is to resonate the transistor output capacitance over a bandwidth. Ideally the active device internal current source will then see a purely resistive impedance equal to $R$ over the band, thus producing a wideband PA frequency response. The design procedure for the output matching network is explained below. An analogous procedure has been used for the input matching network.

A. Matching Network Design Approach

By calculating the inverse of the conjugate value of the optimum load impedance $Z_{L, 3\text{ GHz}}$, a load line of $R_0 = 32\Omega$ and a transistor output capacitance of $C_{\text{out}} = 2.4$ pF can be estimated. In summary, the matching network should therefore be designed to match $R_0$ and $C_{\text{out}}$ to 50 $\Omega$ across the 2–4-GHz bandwidth.

The prototype low-pass matching network is shown in Fig. 3(a). The normalized admittances, $g$ elements, for the prototype low-pass matching network can be calculated using equations found in [17] and [18]. These networks have been derived to have an optimum minimum-loss characteristic across a given bandwidth. The calculation of $g$ elements involve the $Q$ factor, $Q = \frac{R_0 \omega_1 C_{\text{out}}}{R_0 + \omega_1^2 C_{\text{out}}}$, where $\omega_1 = \sqrt{\omega_1 \omega_2}$ with $\omega_1$ and $\omega_2$ being the lower and upper band edge angular frequencies. Note that a value of $C_1 = 2.85$ pF have been used instead of $C_{\text{out}} = 2.4$ pF. The reason is that a value of $C_1 = 2.85$ pF will make it easier to convert the lumped network to a corresponding distributed network, as will explained in Section III-B.

The $g$ elements represent a low-pass filter in a 1-$\Omega$ system with 1-rad/s corner frequency [18]. The low-pass prototype network corner frequency is scaled from the nominal 1 rad/s to the design value ($\omega_0$) by dividing the elements $g_1$, $g_2$, and $g_3$ by $\omega_2/\omega_1$. The impedance scaling is then applied by multiplying the shunt elements $g_1$ and $g_2$ by $1/R_0$, and the series elements $g_0$, $g_2$, and $g_4$ by $R_0$.

The low-pass network is thereafter transformed into a bandpass version by resonating each series or shunt element at $\omega_0$. Fig. 3(b) shows the final values of the elements of the bandpass network after frequency and impedance scaling.

In order to scale the terminating resistor upwards to 50 $\Omega$, a Norton transformation have been used because of its ability to insert an ideal transformer into the network without affecting the bandwidth [18]. An ideal transformer with a transformation ratio of $n = 1.173$ is inserted at the output. The inductor $L_3$ and the terminating resistor are scaled upwards in impedance by a factor $n^2$, as shown in Fig. 3(c). Using Norton transformation, the transformer together with the two series-shunt capacitors are transformed to a $\Pi$ arrangement of capacitors, as shown in Fig. 3(d).
B. Distributed Matching Network

As shown in Fig. 3(e), the capacitor $C_1 = 2.85 \text{ pF}$ can be replaced by three parallel capacitors, the transistor output capacitance $C_{\text{out}} = 2.4 \text{ pF}$, $C_{11} = 0.1 \text{ pF}$, and $C_{12} = 0.35 \text{ pF}$. Based on transforms between lumped and distributed elements, the lumped network is transformed into the distributed network shown in Fig. 3(f).

A resonant parallel $L-C$ to ground can be approximated by a grounded quarter-wavelength transmission line stub [19]. The characteristic impedance of the transmission line stub is equal to the reactance of the inductor or capacitor multiplied by a factor $\pi/4$. Based on this transformation, the resonators $L_1-C_{11}$ and $L_3-C_{3}$ in Fig. 3(e) have been replaced by shunt stubs $T_{L_1}$ and $T_{L_3}$, respectively.

Moreover, based on that the model of a transmission line is approximated by a lumped II-network, $C_{12}$, $L_2$, and $C_4$ have been replaced by a transmission line $T_{L_2}$ [19].

Finally, the complete distributed network is shown Fig. 3(f). The capacitor $C_2$, which is a part of the matching network, is kept lumped because it can also serve as a dc-block capacitor.

The impedances of the TLs are obtained by those transforms and their physical sizes are computed in simulator. Since the calculations are based on approximate formulas, a slight modification on the physical sizes of the transmission lines have been made by fine tuning in simulator. Fig. 4 compares the insertion loss and return loss of the lumped-element matching network and the corresponding distributed network. They show similar response versus frequency, but, as expected, with more losses for the distributed network due to the losses of the substrate and the conductor metal.

Fig. 5 shows the impedance of the output matching network, as well as the impedance of the second harmonic. We notice that the second harmonic is far away from short circuit, and hence, according to the results in Section II-C, high PAE performance is expected across the bandwidth.

![Insertion loss and return loss for the lumped output matching network (thick) and its corresponding distributed network (thin). The simulations use port 1 and port 2 impedances of 32 and 50 $\Omega$, respectively.](image)

![Simulated impedance of the distributed output matching network versus frequency. The fundamental and second harmonic impedance frequency ranges are given by 2–4 and 4–8 GHz, respectively.](image)

IV. PA DESIGN AND IMPLEMENTATION

The circuit diagram of the designed PA is depicted in Fig. 6. The space between the transistor and printed circuit board (PCB) lines is reduced as much as possible by careful alignment in order to avoid undesirable parasitics that will reduce the bandwidth. $L_{\text{bond}}$ and $L_{\text{bond}}$ are used to model the input and output bondwire inductances, respectively. Their values are estimated to be 0.15 nH each.

The output matching network consists of the distributed network determined in Section III. It is surrounded by the solid rectangle in Fig. 6. The only difference is that the capacitor $C_4$ is used to short circuit the stub in order to apply the drain bias. The input matching network, surrounded by the dashed box, was derived using the same approach used for the output matching network. Two tapers $T_{L_1}$ and $T_{L_2}$ have been added at the input and output of the device. Without adding them, the practical implementation of the PA would be very difficult because $T_{L_2}$ and $T_{L_4}$ would be at the edges of the PCBs.

The input matching network has been slightly modified in order to stabilize the PA. The Rollet stability factor ($k$) of the amplifier is given by [20]

$$k = \frac{2 \cdot \text{Re}(Z_{11}) \cdot \text{Re}(Z_{22}) - \text{Re}(Z_{12} \cdot Z_{21})}{|Z_{12} \cdot Z_{21}|}.$$  

The expression above clearly shows that $k$, i.e., the stability, can be improved by increasing the real part of $Z_{11}$. Therefore, a 27-$\Omega$ series resistance $R_{g1}$ is added at the input of the amplifier.
to improve the stability in the high-frequency band. Further improvement in the amplifier stability in the low-frequency band can be achieved by reducing the gain in this range. The parallel resistance $R_{g3}$, set to 400 $\Omega$, improves the low-frequency stability margin by reducing the input impedance further.

The inductors $L_g$ and $L_d$ are equal to 8 nH and are used to prevent the leakage of RF into the dc supply lines. $L_2$ and $L_6$ have been bent away from the metal ridge on which the active device is mounted in order to reduce the electromagnetic coupling. Electromagnetic simulations were performed on the transmission line parts of the input and output matching networks to study the effects of the bends in the final layout. A fine tuning on the matching networks has been made to overcome their effects. The circuit was finally optimized for high-efficiency and wideband operation to minimize the impact of mounting and manufacturing tolerances. It is important to note that the optimization did not significantly change the original design derived in Section II.

Finally, Monte Carlo simulations have been used to study the impact of components variability and uncertainty on the PA performance. Uncertainties introduced by the manufacturing process and the lumped components have been considered. The Monte Carlo simulations have shown that the design is robust and not very sensitive to these variations.

The PA was implemented on a Rogers 5870 substrate with $\varepsilon_r = 2.33$ and thickness of 0.4 mm. Its size is $65 \times 65$ mm$^2$. Fig. 7 is a photograph of the fabricated PA using the bare-die GaN-HEMT device.

V. MEASUREMENT RESULTS

The implemented wideband PA has been characterized by large-signal and modulated measurements to evaluate its performance.

A. Large-Signal Measurements

Measurements were made using a continuous wave (CW) input signal generated by a microwave synthesized source (Agilent E4438C) boosted by a microwave driver amplifier, and the relevant power levels were measured by a power meter (Agilent E4419B). Filtering was indeed used to ensure high-accuracy power measurements. A low-pass filter with 4-GHz cutoff frequency has been placed at the output of the amplifier while measuring the PA performance between 1.75–3.5 GHz. The 4-GHz low-pass filter has been replaced by another low-pass filter with 6-GHz cutoff frequency to measure the PA performance between 3.5–4.5 GHz.

In order to check the sensitivity of the PA performance versus gate bias $V_{GS}$, a gate-bias sweep was first performed. Output power $P_{out}$ and PAE were therefore measured versus gate voltage at different frequencies. The results showed that the PA performance at peak output power was insensitive to the gate voltage. Hence, for the large-signal measurements the chosen dc bias for the gate is similar to the one used in simulations $V_{GS} = -3.2$ V and the drain bias is set, as in simulations, to $V_{DS} = 28$ V.

The PA were characterized versus frequency between 1.75–4.45 GHz using a constant input power of 31 dBm. Figs. 8 and 9 show the measured frequency response of the wideband PA. The measured output power is between 40–42 dBm in the frequency range of 1.9–4.3 GHz, which means that less than 2-dB ripple in the output power, and hence, in the power gain, is obtained across the band. Within the same band, the drain efficiency of the amplifier is between 57%–72%. This corresponds to a PAE between 50%–63% and a fractional bandwidth of 78% about a center frequency of 3.1 GHz.

In Figs. 8 and 9, a reasonable agreement between simulation and measurement results can be noted up to 3.2 GHz. At higher frequencies, simulations and measurements diverge, but the difference is still acceptable as the maximum difference between simulated and measured output power and drain efficiency are less than 2 dB and 10%, respectively.

Figs. 10 and 11 show the power gain and PAE plotted versus output power for different frequencies 2, 2.5, 3.5, and 4 GHz. This set of frequencies has been chosen because 2 and 4 GHz...
Fig. 9. Measured and simulated drain efficiency of the PA versus frequency at a fixed input power of 31 dBm.

Fig. 10. Measured PAE versus output power at 2, 2.5, 3.5, and 4 GHz. The gate bias voltage used in the measurements is slightly below the pinch-off voltage, which was selected to maximize the peak efficiency. This explains the gain decrease at low input power levels in Fig. 10. By a slight increase of the gate bias, a more constant back-off gain can be achieved with a just small degradation in peak efficiency performance.

Fig. 11. Measured gain versus output power at 2, 2.5, 3.5, and 4 GHz.

Fig. 12. Measured and simulated PAE and gain versus output power at 2.5 GHz. A very good agreement between simulation and measurement results is obtained at high power levels. The disagreement at lower power levels may be explained by the fact that the model was identified assuming a switched high-power mode of operation, therefore sacrificing the accuracy in backed-off operation [15].

Fig. 12. Comparison between measured and simulated PAE and gain versus output power at 2.5 GHz.

are at the band edges, while 2.5 and 3.5 GHz are the frequencies having the highest and lowest efficiency, respectively. The gate bias voltage used in the measurements is slightly below the pinch-off voltage, which was selected to maximize the peak efficiency. This explains the gain decrease at low input power levels in Fig. 10. By a slight increase of the gate bias, a more constant back-off gain can be achieved with a just small degradation in peak efficiency performance.

Fig. 12 shows measured and simulated gain and PAE versus output power at 2.5 GHz. The output power compresses at 41 dBm where the maximum efficiency reaches 60%. The measured gain is 10 dB. A very good agreement between simulation and measurement results is obtained at high power levels. The disagreement at lower power levels may be explained by the fact that the model was identified assuming a switched high-power mode of operation, therefore sacrificing the accuracy in backed-off operation [15].

The PA was characterized versus drain-bias voltage in order to evaluate the potential of the PA for use in polar envelope tracking transmitters and to see if the maximum output power can be increased (see Fig. 13). The results show that the maximum output power can be increased to 42 dBm if drain voltage is increased to $V_{DS} = 35$ V. Moreover, the drain efficiency is maintained higher than 64% over a 9-dB dynamic range of output power.

Fig. 14 shows simulated and measured second and third harmonic distortion power levels relative to the fundamental frequency output power. The harmonic output power ranges from $-13$ to $-40$ dBc across the band. Note that the second harmonic at the lowest input frequency is within the operating frequency of the wideband PA.

The large-signal input return loss has been measured using 31-dBm input power, and compared to the simulated one, as shown in Fig. 15. A return loss of better than $-4$ dB is obtained across the band with a minimum of $-5$ dB around 3 GHz. The relatively large input return loss is mainly due to the fact that the input matching network was designed to maximize the PAE,
rather than the gain, across the bandwidth. As a consequence, the return loss is not necessarily minimized in this design.

B. Modulated Measurements

Linearized modulated measurements have been performed to evaluate the performance of the PA when used with modern wireless communication signals.

In the experiment, a 20-MHz long-term evolution (LTE) signal with 11.2-dB peak-to-average ratio (PAR) is used. The high PAR implies that the PA will operate in a highly backed off state, which results in relatively low average efficiency. Measurements were performed at two different frequencies: 2.5 and 3.5 GHz. These frequencies have been chosen because of their position in the middle of the band and because of the peak PA efficiency that is highest at 2.5 GHz (60% PAE) and lowest at 3.5 GHz (50% PAE). The digital pre-distortion (DPD) used, at both frequencies, is based on a memory polynomial model with nonlinear order 11 and memory depth 6 [21].

Fig. 16 shows the measured output spectrum at 2.5 GHz, with and without DPD, at an average input power of 18.8 dBm for the LTE signal described above. The adjacent channel leakage ratio (ACLR) of the PA without DPD reaches $-38.5$ dBc with an average PAE of 30%, whereas the ACLR of the PA with the DPD reaches $-44$ dBc at an average PAE of 27%.

The output spectrum was also measured with the same LTE input signal at 3.5 GHz. The ACLR is improved from $-37$ to $-42$ dBc when DPD is applied resulting in a linearized average efficiency of 25%. These results show that the presented PA can be used in wireless communications applications for a wide range of frequencies. Finally, it is important to state that, as in all modulated measurements, the absolute values for the average efficiency depend on the statistics of the signal and could easily be improved if a signal with lower PAR power level was used.

![Fig. 13. Comparison between measured and simulated drain efficiency and output power versus drain voltage at 2.5 GHz.](image)

![Fig. 14. Measured and simulated second and third relative harmonic level.](image)

![Fig. 15. Measured and simulated large-signal input return loss using 31-dBm input power.](image)

![Fig. 16. PA output signal spectrum of a 20-MHz LTE signal at center frequency of 2.5 GHz before and after digital predistortion.](image)
VI. CONCLUSION

In this paper, an extensive design procedure for wideband highly efficient PAs has been presented. The procedure is based on a load/source–pull methodology combined with a systematic design of broadband matching networks. The proposed procedure has been demonstrated by implementing a hybrid high-efficiency wideband PA based on a 15-W bare-die GaN HEMT device. Experimental results verify the success of the presented method. Large-signal measurement results show 78% fractional bandwidth around 3.1-GHz center frequency, less than 2-dB ripple in the gain across the band resulting in an output power between 40–42 dBm and PAE between 50%–62%. Linearized modulated measurements using a 20-MHz LTE signal demonstrate an average PAE of 27% and 25%, and an ACLR of −43.7 and −42 dBc at 2.5 and 3.5 GHz, respectively. The excellent results obtained show that the approach is suitable for the design of broadband PAs for future wireless systems where wide-bandwidth needs to be combined with high efficiency and linearity.

REFERENCES


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Paper D

Investigation of push-pull microwave power amplifiers using an advanced measurement setup

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Submitted to IEEE Transactions on Microwave Theory and Techniques.
Investigation of push-pull microwave power amplifiers using an advanced measurement setup

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Abstract—In this paper, we investigate the influence of the output balun for realization of wideband and efficient microwave push-pull power amplifiers (PAs). Therefore, a novel push-pull harmonic load-pull measurement setup that allows arbitrary balanced fundamental and second harmonic loads to be presented to a push-pull PA is proposed. Moreover, a push-pull GaN-HEMT PA operating between 1-3 GHz has been developed and implemented without a balun at the output side. By using this prototype together with the proposed measurement setup, we demonstrate the importance of the even mode second harmonic response of the output balun. The measurement results illustrate that the efficiency may be degraded up to 25% if improper common mode harmonic impedances are presented by the balun. The approach presented in this paper allows the PA and balun to be investigated separately and is therefore expected to be an important tool for further research on balun and PA structures suitable for high efficiency and wideband push-pull applications at microwave frequencies.

Index Terms—Broadband, GaN-HEMT, high efficiency, power amplifier, push-pull.

I. INTRODUCTION

THE never-ending demand for increasing communication speed and data rates in wireless communication systems results in the emergence of new standards such as, wideband code division multiple access (WCDMA), mobile world wide interoperability for microwave access (m-WiMAX), and long-term evolution (LTE). Therefore, wider channel bandwidths, larger spectrum allocations and larger number of frequency bands are required. Consequently, the PAs, which are one of the most critical component in wireless transmitters, must be highly efficient and must have broadband capabilities to cover many frequency bands operating at different standards at the same time.

Design techniques for high efficiency PAs, like harmonic tuning and switching mode are already presented and thoroughly discussed in literature [1]–[4]. However, such PAs are commonly limited to narrowband applications. To enable high efficiency wideband PAs, harmonic tuning is needed. Recently, many wideband PAs, with octave bandwidth or lower, have been published in literature [5]–[11]. To extend the bandwidth to more than one octave, harmonic tuning cannot be used since harmonics will fall inside the required bandwidth [12].

Therefore, design techniques, like push-pull, that allow second harmonic tuning over wider bandwidth must be used.

Push-pull is an old design technique used for PAs to provide high efficiency and linearity [2]. This kind of PAs were targeted mostly for broadband low frequency applications [13]–[16]. However, they also have a big potential for applications at microwave frequencies due to their wide bandwidth, high power, high efficiency, and their capability to directly drive wideband antennas requiring balanced feeds [17].

Many push-pull architectures have been introduced at microwave frequencies. A push-pull PA based on an extended resonance technique is presented in [18], while a push-pull PA using periodic structures for harmonic tuning is proposed in [19]. The benefit of separating the effects of the even and odd harmonic frequencies in push-pull configurations is used in [20] by the simple connection of a pair of inverse class-F PAs and in [21] by the connection of a pair of the newly introduced class-E/F PAs. However, the mentioned architectures were not targeted for broadband applications.

Push-Pull PAs require baluns, at the input and output of the PA, to combine the branches of the two amplifiers and to achieve the required 180° phase shift. These latter have important impact on push-pull PAs performance and it is very challenging to realize broadband baluns at microwave frequencies [2]. This explains why, up to date, broadband push-pull PAs at microwave frequencies have not been widespread.

Recently, the design of broadband balun suitable for common mode operation at microwave frequencies has been addressed [22]. Based on the balun in [22], a push-pull PA of decade bandwidth is presented in [23]. Even though the bandwidth potential of the push-pull configuration has been demonstrated [23], there is no possibility to investigate or verify the true operation and interaction between PA and balun.

In this paper, we propose a push-pull harmonic load-pull measurement setup that allows the influence of the balun on PA performance to be investigated in detail under realistic push-pull operating conditions. A prototype wideband 1-3 GHz push-pull PA has been developed to investigate the influence of the balun characteristics on the overall PA characteristics. This approach allows the PA and balun properties to be isolated from another and is therefore an important tool for further understanding and optimization of PAs and baluns for wideband push-pull microwave PAs.

This paper is organized as follows. In section II, the design of a wideband push-pull PA prototype is presented. In section III, a novel experimental setup is proposed to be used in the investigation while the experimental results showing the effect...
of the balun on the PA performance are shown in Section IV. Conclusions are given in Section V.

II. PUSH PULL PA PROTOTYPE

An overview about the device used, the adopted topology of the designed push-pull PA and its simulated performance will be presented hereafter.

A. Device Model

At microwave frequencies, and in particular for wideband designs, the parasitics are detrimental to the performance and therefore the effects of package parasitics were eliminated by using a bare-die device. In the design, the 2.5 mm GaN bare-die device, TGF2023-02 from Triquint Semiconductors, has been used. The device has a saturation drain current of around 2.5 A, a drain-source breakdown voltage of around 100 V, and a pinch-off voltage around -3.8 V.

An in-house model optimized for high efficiency operation was developed for the bare-die transistor. A description of the model can be found in [24], [25]. The same model topology has been successfully used for the design of high efficiency single-ended LDMOS [24] and GaN [26]–[28] PAs.

B. Device analysis

The first step to design the 1-3 GHz push-pull PA was to study the behavior of the device by performing load-pull/source-pull simulations. Using the large signal transistor model developed, we located the fundamental load and source impedances, at the die reference plane, that maximize the efficiency of the PA in the required bandwidth. The optimum source and load impedances, shown in Fig. 1, are obtained while the input and output second harmonic impedances are open.

The effect of the output second harmonic on the efficiency performance has been studied by varying their impedances across the periphery of the Smith chart while the device sees, at each fundamental frequency, the corresponding optimum impedances depicted in Fig. 1. The power-added efficiency (PAE) of the device versus the phase variation of the output second harmonic reflection coefficient, while the input second is set to open, is shown in Fig. 2. It is noticed that the efficiency is strongly dependent on the second harmonic phase and the best performance is achieved within ±90° around the open circuit region.

Then, the same investigation is made for the input second harmonic, input and output third harmonics while the output second harmonic is set to open. The results have showed that their effect is negligible compared to the one of the output second harmonic. Moreover, the PAE is almost constant and independent of the phase termination of these harmonics. These results are in agreement with results in [9], although a different device was used.

It is very challenging to design a matching network for wide bandwidth that takes care of second harmonic terminations. This latter task becomes even impossible to solve when the bandwidth extends for more than one octave because the second harmonic will fall inside the band. In the following, a push-pull configuration is proposed to overcome this problem.

C. Matching network topology

In Section II-B, it has been shown that the required second harmonic termination for the device, to provide high efficiency conditions, is open. The push-pull PA topology, that will be proposed later, uses the differential and even mode responses of the transistor load network to provide the required fundamental and second harmonic terminations beyond the octave limit of a traditional single-ended design approach. Therefore, it is sufficient that the input and output matching networks provide the matching at the fundamental frequencies.

The design of the fundamental input and output matching networks is based on the systematic design approach presented in [9]. In this approach, the matching network is firstly derived for a lumped network then it is transformed to distributed network. The lumped network and its corresponding distributed network are shown in Fig. 3.

D. Push-Pull PA topology

The proposed PA topology, shown in Fig. 4, consists of two PAs and a balun. Each PA is a wideband single-ended
PA, using the distributed matching network topology shown in Fig. 3(b). The two PAs are connected at the input through a commercial balun. The latter transforms the unbalanced input signal into two, 180° out of phase, signals with equal magnitude. These differential signals are fed to the two PAs and collected at the balanced output.

The response of the matching network at even harmonics will be different from its response at fundamental and odd harmonics. Assuming an ideal input balun, the fundamental and odd harmonics voltage components of each PA will be equal in amplitude, but opposite in phase. Consequently, a virtual ground develops at the line of symmetry at the center of the differential impedance and the equivalent half circuit in differential mode will be equivalent to the one shown in Fig. 5(a). However, at the even harmonics, the harmonic voltage components are equal in amplitude and phase. Thus, the line of symmetry becomes a virtual open circuit and the equivalent half circuit in common mode will be equivalent to the one shown in Fig. 5(b).

Usually, the output signals from the PAs are recombined at the output with a balun. However, in this design we kept a balanced output to be able to study the effect of the even mode impedance of the balun on the performance of wideband PAs. Therefore, the two, $T_{Le}$, output lines are added to facilitate the connection to the output world. They are not a part of the matching networks and they will be de-embedded during the measurements.

**E. Simulation results and implementation**

The simulated even mode impedance of the output matching network is shown in Fig. 6. According to the simulation results in Fig. 2, we notice that the second harmonic impedance is away from the inadequate region, and hence high efficiency performance is expected across the entire 1-3 GHz bandwidth.

The simulated performance of the designed PA, including the commercial input balun used (Anaren, B0430J50100A00)
is presented in Fig. 7. For a constant input power of 31 dBm, the simulated output power is between 41-44 dBm and the drain efficiency is between 55-75% in the frequency range of 1-3 GHz. This corresponds to 100% fractional bandwidth around a center frequency of 2 GHz.

The push-pull PA was implemented on a Rogers 5870 substrate with $\varepsilon_r = 2.33$ and thickness of 0.8 mm. Its size is $65 \times 55$ mm$^2$. Fig. 8 shows a photo of the fabricated push-pull PA using bare-die GaN-HEMT devices.

III. EXPERIMENTAL SETUP

Single-ended configurations can be characterized using a traditional load-pull system [31]. The load-pull can either be performed by using passive impedance tuners [32] or by active injection [31]. To control the injected signal, two different methods are usually used, the open loop approach [31] or the closed loop approach [33]. However, in these standard systems only one input and one output are considered.

For push-pull configurations however, traditional load-pull does not provide the real performance of the device working at differential and common modes. A Differential Load-Pull System is proposed in [34]. However, it measures only the differential mode using differential tuners. A system that is able to measure both differential and common-mode loads independently, is presented in [35]. It uses two active loops along with two $0 - 180^\circ$ hybrids which decouple the differential and common modes.

In the following, we propose a push-pull harmonic load-pull setup, using a Large Signal Network Analyzer (LSNA) and the open loop approach, that is capable of setting, and tuning any balanced load at fundamental and second harmonic as well as measuring the voltage and current waveforms at fundamental and all harmonics.

A. Push-pull harmonic load-pull setup

To evaluate the performance of the push-pull PA, a balanced load has to be connected at the output of the PA in order to convert the balanced output signal into an unbalanced one as shown in Fig. 9. The load is typically a balun [2] but could also be a balanced antenna [17]. Unfortunately, ideal broadband balanced loads are not easy to implement at microwave frequencies [2]. Although they might present wideband fundamental impedance, it has recently been recognized that their even mode impedance might degrade the performance of the PA [22]. Therefore, an advanced measurement setup that allows balun and PA designs to be investigated separately is required.

The measurement setup, which is based on an active load-pull techniques [31], [36]–[38], will be used to emulate a balun at the output of the PA and to study the effect of the balun on the PA performance. The setup has to provide, at the intrinsic reference plane, any impedance for the fundamental frequencies and higher order harmonics. It is important to note here that the two output branches of the PA cannot be measured independently because, as mentioned in Section II-D, the matching networks seen at the fundamental and second harmonics look different (Fig. 5) and they are only different when the other branch is operated in a balanced mode. Therefore, if the other branch is not loaded with the same impedance, the symmetry is lost and hence, the measured even mode impedance is incorrect.

The push-pull harmonic load-pull setup developed for our experimental investigations is shown in Fig. 10. The fundamental ($f_0$) input signal to the PA is generated with a synthesized continuous wave (CW) RF signal generator. A Large Signal Network Analyzer (LSNA, Maury/NMDG MT4463) is used to measure the traveling voltage waves $a_1$, $b_1$, $a_2$.
and $b_2$ at the calibrated reference plane. The LSNA measures the traveling voltage waves at fundamental and higher order harmonics with absolute magnitude and phase information. This enables reconstruction of the time domain waveforms at the calibrated reference plane (Fig. 10). In order to get the intrinsic traveling voltage waves $a_{1i}, b_{1i}, a_{2i}$ and $b_{2i}$, the access transmission lines (TLe) are de-embedded.

Two automated mechanical tuners (Maury MT982) are used in this experiment to present $50 \Omega$ for fundamental frequencies at the intrinsic reference plane. The settings of the tuners at each fundamental frequency were determined before building the setup. This was done by measuring the S-parameters of each reflectometer and the TLe, using a Vector Network Analyzer. Based on these measurements, the reflection coefficients, $\Gamma_{T1}$ and $\Gamma_{T2}$, that have to be presented by the tuners at each fundamental frequency were determined.

Then, in order to set the intrinsic load reflection coefficient at the second harmonic ($2f_0$), another synthesized CW RF signal generator is used. The intrinsic load reflection coefficient is given by (1). Therefore, by controlling the amplitudes ($A_j$) and phase ($\phi_j$) of $a_{1i}(2f_0)$ and $a_{2i}(2f_0)$, any reflection coefficient can be realized according to

$$
\Gamma_{L1}(2f_0) = \frac{a_{1i}(2f_0)}{b_{1i}(2f_0)} = \frac{A_1e^{j(2\pi(2f_0)+\phi_1)}}{b_{1i}(2f_0)}
$$

$$
\Gamma_{L2}(2f_0) = \frac{a_{2i}(2f_0)}{b_{2i}(2f_0)} = \frac{A_2e^{j(2\pi(2f_0)+\phi_2)}}{b_{2i}(2f_0)}
$$

The amplitude and phase control of the injected signal at the second harmonic is achieved by using vector modulators. The second harmonics are injected at the output of the PA through the tuners as shown in Fig. 10. No pre-characterization of the vector modulators is needed since they are placed outside the reflectometers, and hence, the injected wave is measured at the calibrated reference plane. It is important to note that tuners are used for the fundamental because of the limited available number of vector modulators. Moreover, it is also because the fundamental impedance is kept constant, while load-pull measurements are to be performed at the second harmonic.

The performance of the push-pull PA is calculated based on the measured voltage waves. The total delivered output power, the drain efficiency and gain of the PA are given by

$$
P_{\text{out}} = \frac{|b_{1i}|^2}{2Z_0} + \frac{|b_{2i}|^2}{2Z_0}
$$

$$
\eta = \frac{P_{\text{out}}}{P_{\text{dc}}}
$$

$$
\text{Gain} = \frac{P_{\text{out}}}{P_{\text{avs}}}
$$

where $Z_0$ is the system impedance and is equal to $50 \Omega$. $P_{\text{dc}}$ and $P_{\text{avs}}$ are the total DC power consumption and the available input power, respectively.

IV. EXPERIMENTAL RESULTS

The measurement setup presented above has been used to accomplish the push-pull load-pull measurements at the intrinsic reference plane indicated in Fig. 10. To evaluate the performance of the realized broadband push-pull PA under steady-state conditions, large-signal CW measurements have been performed. A drain bias of $V_{DS} = 28V$ and a gate voltage of $V_{GS} = -3.7V$, corresponding to $50\text{mA}$ quiescent drain current per device, were used.

The measurements were carried out using a constant input power of 31 dBm. In simulations this input power level corresponds to about 3-dB compression. However, in measurements the gain was lower than the simulated one and 31 dBm input power was only enough to drive the PA slightly below the 1-dB compression point. The power handling of the input balun used limited us from applying higher input power and therefore not allowing us to achieve the maximum peak efficiency of the PA. However, this will not prevent us from investigating the effect of the even mode impedance of the idealized balun emulated by the measurement setup.
A. Frequency sweep

The PA was firstly characterized versus frequency between 1 GHz and 3.4 GHz. Fig. 11 and Fig. 12 show the measured frequency response of the push-pull PA for two different terminations of the second harmonic impedance of the output balun open and 50 Ω. The latter is chosen since for a single-ended wideband PA the normal termination would be 50 Ω.

Fig. 11 shows the total output power for the two different terminations, as well as the output power of each output branch of the PA for the case of open termination. The measurements show that the two PAs provide at most frequencies same output power within ±0.8 dB except for frequencies beyond 3 GHz where the amplitude imbalance reaches 2.5 dB. The amplitude imbalance can be attributed to the non ideal balun used at the input that is designed to operate up to 3 GHz [30]. Fig. 12 shows as well the measured drain efficiency of the push-pull PA for the two different terminations.

It is obvious from Fig. 11 and Fig. 12 that the even mode second harmonic termination of the output balun has big impact on the performance of the PA, in particular for the lower frequencies where the second harmonic falls within the fundamental frequency range. Even considering that we could not drive the PA into saturation in the experiments, the drain efficiency is improved at certain frequencies by 10 % when open termination is used instead of 50 Ω. In case of the open second harmonic, the measured output power is between 38 – 41dBm in the frequency range of 1.3 GHz-3.3 GHz which means that the power gain, is between 7 – 10dB. Within the same band the drain-efficiency of the PA is between 45 % and 63 %. This corresponds to a PAE between 40 % and 57 % and a fractional bandwidth of 87 % about a centre frequency of 2.3 GHz.

B. Push-pull waveforms

Fig. 13 shows the measured phase difference between the two outputs of the PA at fundamental and second harmonic. The measured data confirms the correct behavior of the PA since the fundamental output signals are out of phase (180°±10°) and the second harmonic output signals are in phase(0°±8°). Assuming that the matching networks and transistors are identical, these results give important information about the input balun phase imbalance characteristics that otherwise not could be observed in a finalized circuit with an output balun connected.

Comparing the measurement results with the simulations presented in Fig. 7, we notice that the measurements are shifted up in frequency by about 200 MHz. This frequency shift could be associated with the transistor model, and the uncertainties in the lumped element models. The measured drain efficiency is lower than the simulated one by around 12 %. The agreement, could be further improved if the power handling of the input balun did not prevent us from driving the PA into saturation.
However, the differential output, which is the difference of the two output waveforms, approximates a sinusoidal signal well across the frequency range tested.

C. Even mode second harmonic investigation

The influence of the balun is further investigated by studying the sensitivity of the performance of the PA as a function of the phase of unity magnitude second harmonic reflection coefficient. Fig. 15 shows the measured efficiency performance of the push-pull PA at 1.5 GHz and 2.0 GHz. The results show that the efficiency performance of the PA is very sensitive to the phase of the even mode impedance. It can be degraded up to 25% compared to the optimum case when the termination of the second harmonic is open. This measurement reveals the importance of the even mode impedance of the balun to design efficient PAs having similar performance over wide bandwidth.

Although the push-pull operation can separate the fundamental and second harmonic impedances, the problem is instead to design an output balun that avoids the second harmonic reflection phases that degrade the efficiency. The even mode frequency response of the balun, like the one presented in [23] therefore needs to be carefully mapped to the areas where high efficiency can be preserved. The fundamental bandwidth limitations imposed by the balun (or balanced antenna) even mode impedance response is still matter for future research.

The measurements show that the setup allows the interaction between the push-pull PA and balun operation to be isolated from each other and hence allows the influence of the balun on the push-pull PA to be investigated which would not be possible otherwise.

V. Conclusions

In this paper, a study on the capabilities of broadband push-pull PAs for microwave applications has been carried out. In particular, the true operation and interaction between push-pull PA and balun has been addressed. A push-pull PA prototype, having a balanced output, has been designed and the even mode impedance effect on the push-pull PA performance, has been investigated using novel push-pull harmonic load-pull setup.

When the second harmonic of the balun is open circuit, large-signal measurement results show 84% fractional bandwidth around 2.4 GHz center frequency, an output power between 38 dBm and 41 dBm and drain efficiency between 50% and 62%. However, when 50Ω termination for the even mode second harmonic is used, the efficiency was degraded by about 10% for the lower frequencies of the band. Further investigations, presenting an arbitrary reflective even-mode second harmonic balun impedance, shows that the efficiency differ more than 25% between optimum and worst case settings.

The methodology presented demonstrates the capabilities of the setup to enable isolation between push-pull PA and balun, and provides an essential tool for future investigations of baluns and balanced antenna structures that could enable high efficiency harmonically tuned amplifier modes with more than one octave bandwidth.

REFERENCES


Paper E

Concurrent Dual-Band GaN-HEMT Power Amplifier at 1.8 GHz and 2.4 GHz

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IEEE Wireless and Microwave Technology Conference (WAMICON), April, 2012.
Concurrent Dual-Band GaN-HEMT Power Amplifier at 1.8 GHz and 2.4 GHz


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**Abstract**—This paper presents the design, implementation, and experimental results of a highly efficient concurrent dual-band GaN-HEMT power amplifier at 1.8 GHz and 2.4 GHz. A bare-die approach, in conjunction with a harmonic source-pull/load-pull simulation approach, are used in order to design and implement the harmonically tuned dual-band PA. For a continuous wave output power of 42.3 dBm the measured gain is 12 dB in the two frequency bands; while the power added efficiency is 64% in both bands. Linearized modulated measurements, using concurrently 10MHz LTE and WiMAX signals, show an average PAE of 25% and an adjacent channel leakage ratio of -48 dBc and -47 dBc at 1.8 GHz and 2.4 GHz, respectively.

**Keywords**—power amplifier (PA); dual-band, gallium nitride (GaN); high electron mobility transistor (HEMT); harmonic termination, digital predistortion (DPD)

**I. INTRODUCTION**

The fast evolution of wireless communication systems and the roll-out of new communication standards increase the need for multi-band transceivers that can manage simultaneously different standards [1]. Software Defined Radio is recently introduced to implement wireless radios capable of dealing with these requirements through software reprogramming [2]. However, the major issues reside in the RF front-end stage that requires the development of multi-band/multi-standard circuits and subsystems. A critical component for multi-band or multi-standard operation is the power amplifier (PA). In fact, it should simultaneously satisfy low-distortion and high-efficiency requirements, accounting for the amplifying signal features in terms of amplitude variation and bandwidth [3]-[5]. Successful design methodology for the design of single-band high efficiency microwave PAs has been presented in [6]-[7]. In this paper, the capabilities of this methodology for dual-band applications are explored. This is demonstrated by the design of a dual-band harmonically tuned GaN-HEMT PA at 1.8 GHz and 2.4 GHz.

This paper is organized as follows. In Sec. II, a description of the design approach and the implementation of the dual-band PA is presented. The experimental results are presented in Sec. III, while conclusions are given in Sec. IV.

**II. DUAL-BAND PA DESIGN AND IMPLEMENTATION**

In the design, the 3.6 mm GaN bare-die device, Cree CGH60015DE, has been used. The device has a breakdown voltage of 100V, a pinch-off voltage of -3.2 V, and a saturation drain current of 2.3 A, approximately. An optimized Class-AB nonlinear model of the device, supplied by the manufacturer, has been used for the design. The parasitics deteriorate the PA performance. By using a bare-die mounting approach, the most important parasitics associated with the package, such as the lead inductances and tab capacitances, have been minimized. The bare-die transistor chip is mounted to the PA fixture and connected directly to the printed circuit boards (PCBs) using wire bonding. The chip and PCB surfaces have been carefully aligned to minimize the bond wire lengths.

The first step to design the PA was to perform load-pull/source-pull simulations, at 1.8 GHz and 2.4 GHz, at the die reference plane in order to find the fundamental load and source impedances that maximize the output power of the PA. The obtained optimum fundamental impedances were used to perform harmonic load-pull simulations to study the effect of the harmonics on the efficiency performance.

![Figure 1. Simulated optimum impedances, at the transistor reference plane for maximum output power.](image-url)
The simulations verified that terminations of the second harmonic at the input and the third harmonic at the output have negligible impact on the efficiency. Consequently, to reduce the complexity of the matching networks, such harmonics have been neglected in the design of the respective network. The resulting optimum source and load impedances at fundamentals that maximize the output power and the load impedances at the second harmonic that maximize the PAE are shown in Fig. 1. The filled symbols are the loads identified by load-pull/source-pull simulations, while the empty symbols are the final impedances synthesized by a distributed approach [8].

The circuit diagram of the designed dual-band PA is shown in Fig. 2. The inductances $L_{\text{bwg}}$ and $L_{\text{bwd}}$ are used in the circuit design to model the input and output bond-wire inductances, respectively. Their estimated values are 0.15 nH each.

The output matching network consists of two sub-networks, used to control the 2nd harmonic loading conditions (the distributed network surrounded by the solid rectangle in Fig. 2) and the two fundamental impedances (dashed rectangle). For the harmonics, the parallel quarter-wave TL at $f_2$, shorted by the $C_t$ capacitor, provides a short circuit for the second harmonic of $f_2$ at node A. Similarly, the parallel eighth-wave at $f_1$ open-circuited stub provides a short circuit forth second harmonic of $f_1$ at node B. The matching at the two fundamental frequencies, $f_1$ and $f_2$, is provided by the remaining TLs and short-circuited stubs.

The input matching network consists of the distributed network surrounded by the solid rectangle that provides the input matching simultaneously at the two fundamental frequencies $f_1$ and $f_2$. The network surrounded by dashed box, is a stabilization network that provides the stability of the dual-band PA in-band and at low frequencies. This network was included in the load-pull/source-pull simulations. Monte-Carlo (MC) and Electromagnetic (EM) simulations were performed to study the reliability and the robustness of the designed dual-band PA. EM simulations were performed on the transmission line parts of the input and output matching networks. MC simulations studied the uncertainties introduced by the lumped components and the manufacturing process. The EM and MC simulations have shown that the design is robust, not very sensitive to these effects and therefore no tuning or modifications were required.

The dual-band PA was implemented on a Rogers 5870 substrate with $\varepsilon_r = 2.33$ and thickness of 0.8 mm. To facilitate wire bonding the PCBs were gold plated. Fig. 3 shows a picture of the implemented dual-band PA using the bare-die GaN-HEMT device. The bare-die device was attached to the aluminum fixture ridge. From each side of the ridge, the input and output PCBs were attached separately and connected to the device using three bond wires from each side. Moreover, no post-production tuning was used after the implementation of the PA.
III. Measurement Results

The implemented PA has been characterized by small-signal, large-signal and modulated-signals measurements to verify its performance.

A. Small-Signal Measurements

The scattering-parameters of the realized dual-band PA were measured using Agilent E8361A PNA. A drain bias of \( V_{DD} = 30 \) V, and a quiescent drain current of 150 mA (gate voltage of \(-3\) V) were used for this measurement. The measured S-parameters, presented in Fig. 4, show a very good agreement with simulations and therefore, it demonstrates the correct behavior of the PA in the proximity of 1.8 GHz and 2.4 GHz. The input match (S11) is better than 20 dB at 1.8 GHz and better than \(13\) dB at 2.4 GHz while the output match (S22) is better than 15 dB at both bands. The small-signal gain (S21) is around 16 dB in the two bands.

![Figure 4. Measured and simulated S-parameters of the dual-band PA.](image)

B. Large-Signal Measurements

Continuous wave (CW) input signals have been generated by a microwave synthesized source (Agilent E4438C) boosted by a microwave driver amplifier and the output power levels were measured by a power meter (Agilent E4419B). The chosen dc bias is the same as for the S-parameter measurement. The dual-band PA has been characterized versus frequency between 1.6 GHz and 2.6 GHz, with a 30 dBm fixed input power drive level. From Fig. 5, it can be noted that the agreement between simulations and measurements is very good and the center frequency is accurately predicted by the simulations. The measured peak PAE is 64% in the two bands, with a measured output power of 42.3 dBm at 1.8 GHz and 42 dBm at 2.4 GHz.

![Figure 5. Measured and simulated PAE and output power vs. frequency, of the dual-band PA, for 30 dBm input power.](image)

The amplifier exhibits a PAE higher than 50% between 1.67 GHz and 1.87 GHz and between 2.34 GHz and 2.48 GHz. This corresponds to 11% and 6% fractional bandwidth around 1.8 GHz and 2.4 GHz bands, respectively.

![Figure 6. Measured PAE and power gain vs. input power, of the dual-band PA, at 1.8GHz and 2.4GHz.](image)

C. Modulated Measurements

To demonstrate that the dual-band PA is linearizable and able to meet modern wireless communication system standards, modulated measurements have been performed. The digital-predistortion (DPD) used, is the memory polynomial model with nonlinear 7 and memory depth 3 [9]. The PA has been tested first using one modulated signal
(non-concurrent mode). The signals used are 5 MHz WCDMA, 10 MHz LTE signals both with 7 dB Peak-to-Average-Ratio (PAR), and WiMAX signal with 8.5 dB PAR. Average output power, PAE, and ACLR, with and without DPD are summarized in Table I.

<table>
<thead>
<tr>
<th></th>
<th>Pout (dBm)</th>
<th>PAE (%)</th>
<th>ACLR (dBc)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>w/o DPD w DPD</td>
<td>w/o DPD w DPD</td>
<td>w/o DPD w DPD</td>
</tr>
<tr>
<td>WCDMA @ 1.8GHz</td>
<td>35.5 35.4</td>
<td>34.7 34.5</td>
<td>-36.6 -53.1</td>
</tr>
<tr>
<td>WiMax @ 2.4GHz</td>
<td>34.5 34.7</td>
<td>29.9 30.3</td>
<td>-37.4 -51.7</td>
</tr>
<tr>
<td>LTE @ 1.8GHz</td>
<td>35.5 35.6</td>
<td>34.6 35.5</td>
<td>-35.2 -52.6</td>
</tr>
<tr>
<td>LTE @ 2.4GHz</td>
<td>35.5 35.5</td>
<td>32.7 33.3</td>
<td>-33.3 -49</td>
</tr>
</tbody>
</table>

Then the PA has been tested in concurrent mode. The linearization was performed with the 2-D-DPD technique presented in [10]. In the first experiment, the WCDMA and the LTE signal were used at 1.8 GHz and 2.4 GHz bands respectively. In the second experiment the LTE signal is used at 1.8 GHz band while the WiMAX signal is used at the 2.4 GHz band. The measured output spectrum at 1.8 GHz and 2.4 GHz (second experiment), before and after DPD, for an average input power of 19 dBm, are shown in Fig. 7 and Fig. 8, respectively. Average output power, PAE, and ACLR, with and without DPD of the two experiments, at the two operating bands, are summarized in Table II. We notice that the average PAE is degraded by 5-10% compared to the case where the PA is driven by one modulated signal at the time (Table I).

Yet, these results show that standard DPD methods can be used to linearize the DPA in concurrent modes to meet modern wireless communication system standards.

IV. CONCLUSION

In this paper, the design of a concurrent dual-band high efficiency harmonically tuned PA using a GaN-HEMT has been presented. Using bare-die devices and the design approach based on harmonic load-pull/source-pull simulations have allowed the realization of high performance dual-band PA at 1.8 GHz and 2.4 GHz. The CW measurement showed, in both bands, a power gain of 12 dB, peak PAE of 64% and an output power of 42.3 dBm. An average PAE of 25% was recorded when LTE and WiMAX signals were applied concurrently.

ACKNOWLEDGMENT

This research has been carried out in the University of Roma Tor Vergata and in the GigaHertz Centre in a joint project financed by the Swedish Governmental Agency for Innovation Systems(VINNOVA), Chalmers University of Technology, ComHeat Microwave AB, Ericsson AB, Infineon Technologies Austria AG, Mitsubishi Electric...
Corporation, NXP Semiconductors BV, Saab AB, and SP Technical Research Institute of Sweden.

REFERENCES


Design Method For Quasi-Optimal Multi-Band Branch-Line Couplers

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Submitted to International Journal of RF and Microwave Computer-Aided Engineering.
Design Method for Quasi-Optimal Multi-Band Branch-Line Couplers

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Abstract

In this paper, the design approach, the implementation, and experimental results of multi-band branch-line couplers operating at arbitrary frequencies are presented. The conventional branch-line coupler structure is adapted to multi-band operation by shunting its four ports with multi-band reactive networks. The performance of the proposed multi-band couplers is theoretically analyzed and optimized through the even-odd mode circuit analysis. Dual-band, triple-band, and quad-band microstrip branch-line couplers have been realized and tested in order to verify the design method. The obtained experimental results show excellent agreement with theoretical and simulated ones, thus validating the proposed approach.

Keywords: Balanced, branch-line, coupler, multi-band, passive.

I. INTRODUCTION

The fast development of wireless communication systems and the roll-out of new standards, such as GSM (800/900/1800 MHz), WCDMA (2.1 GHz), WLAN (2.45/5.25 GHz) and WiMAX (3.5 GHz), requires multi-band transceivers [1] in order to process several types of signals at the same time. Among different combining passive structures, the branch-line coupler is one of the most important components used in microwave and millimeter-wave applications because of its essential role in balanced [2] and Doherty [3, 4] amplifiers, mixers [5], modulators [6] and beam forming networks for circularly polarized antennas [7] due to its good directivity, and inherent $90^\circ$ phase shift between its output ports. As a consequence, a method for the design of multi-band branch-line couplers can be of key importance for the development of multi-band transceivers.

Recently, different configurations for the design of dual-band branch-line couplers have been proposed [8–19]. One of the most adopted solutions is based on the replacement of the quarter-wave transmission lines of the branch-line coupler with an equivalent dual-band network [8–11]. Alternative approaches are proposed in [12, 13], where the coupling between microstrip lines is successfully exploited, in [14], where the three-branch-line topology is proposed, in [15], where the concept of stub-loaded rectangular patch is introduced, and in [16], where the dual-band operation is obtained by adding a properly designed series transmission line section at the four ports of the single-band branch-line coupler. The capability of implementing dual-band branch-line couplers by means of composite right/left-handed transmission lines has also been demonstrated in [17–19]. However, all the mentioned configurations were developed only for dual-band operations.

Solutions to design branch-line couplers having more than two operating bands can be found in [20–24]. However, the methods proposed in [20–22] are not assisted with a full theoretical analysis that demonstrates the possibility to extend them for an arbitrary number of operating frequencies. Moreover, the approach presented in [23] is limited to correlated frequencies, while the one adopted in [24] exploits the composite

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right/left handed transmission line concept, resulting in degraded performance and high losses due to the complexity of the circuit and the critical dimensions of some of its constitutive semi-lumped elements.

In this paper, drastically extending [25], a closed form design approach for multi-band branch-line couplers for arbitrary operating frequencies is presented. Starting from the dual-band quarter-wave transmission line topology, an optimization technique is proposed to extend its behavior to three arbitrary bands. Later, the method is generalized for any number of arbitrary bands. The design approach is thereafter demonstrated through the practical implementation of dual-band, triple-band, and quad-band microstrip branch-line couplers. The experimental measurements validate the proposed design methodology, showing excellent results in terms of matching, directivity, phase quadrature and isolation at each operating frequency band.

II. THEORETICAL ANALYSIS AND DESIGN EQUATIONS

The conventional (single-band) branch-line coupler is composed of four quarter-wave transmission lines [26]. Hence, the design of the multi-band branch-line coupler starts from the investigation of a suitable topology to achieve multi-band quarter-wave transmission lines. Then, by combining four of such structures, the multi-band branch-line coupler is achieved.

2.1 Dual-band quarter-wave transmission line

The ABCD-matrix of a quarter-wave transmission line having characteristic impedance \( Z_T \) is given by [26]

\[
ABCD_{\lambda/4} = \begin{bmatrix}
0 & jZ_T \\
jZ_T & 0
\end{bmatrix}
\]  

(1)

The matrix in (1) can be simultaneously produced at two arbitrary frequencies \( f_i \) with \( i = 1, 2 \) by means of the network in Fig. 1 [8]. It consists of a series transmission line, having characteristic impedance \( Z_c \), and two purely reactive shunting elements \( (B_i) \). The ABCD-matrix of the topology in Fig. 1 at the two frequencies is given by:

\[
ABCD_{f_i} = \begin{bmatrix}
1 & 0 & jZ_c \sin \theta_i \\
0 & 1 & jZ_c \cos \theta_i
\end{bmatrix} \begin{bmatrix}
1 & 0 \\
0 & 1
\end{bmatrix}
\]  

(2)

where \( \theta_i = \frac{\pi}{2} \frac{f_i}{f_c} \). In [8] it has been demonstrated that by equating (2) to (1) leads to the following constraints for the topology in Fig. 1:

\[
f_c = \frac{f_1 + f_2}{2}
\]

(3)

\[
Z_{c,i} = \frac{Z_T}{\sin \left( \frac{\pi}{2} \cdot \frac{f_i}{f_c} \right)}
\]

(4)

\[
B_i = \frac{1}{Z_c \tan \left( \frac{\pi}{2} \frac{f_i}{f_c} \right)}
\]

(5)

Being \( Z_{c,1} = Z_{c,2} \) in (4), the design parameter \( Z_c \) of the network in Fig. 1 is unique, allowing the ABCD-matrix in (1) to be obtained at both frequencies without any compromise. It has to remark that (4) has valid solutions, i.e. positive values for \( Z_{c,i} \), only if \( 0 < f_i / f_c < 2 \). Accounting for (5), this condition is verified if both frequencies are greater than 0.
2.2 Triple-band quarter-wave transmission line

Assuming three arbitrary frequencies \(0 < f_1 < f_2 < f_3\), a unique \(Z_c\) solution is not derivable from (4), since the sine function allows a unique solution only for two angles symmetrically positioned with respect to \(90^\circ\). Therefore, it is not possible to exactly reproduce the ABCD-matrix in (1) at the three frequencies, simultaneously. However, by properly choosing the design parameters of the network in Fig. 1 it is possible to find a condition in which the resulting matrix at the three frequencies is as close as possible to (1).

To infer the optimum design parameters, it is useful to start performing the matrix products in (2). Moreover, the relation in (5) has to be adopted to define the proper \(B_i\) values in order to guarantee that the network in Fig. 1 behaves as a quarter-wave transmission line at all operating frequencies. The resulting ABCD-matrix is

\[
ABCD_{f_i} = \begin{bmatrix}
0 & jZ_c \sin \left(\frac{\pi f_i}{f_c}\right)
\end{bmatrix}
\]

(6)

From the ABCD-matrix in (6) the full two-ports scattering-parameters matrix can be derived. However, in order to reduce the scattering parameters to consider for the analysis, it is useful to account for the properties of the network in Fig. 1. In particular, due to the symmetry of the network, \(S_{11} = S_{22}\). Moreover, assuming passive and lossless elements, it follows that \(S_{21} = S_{12}\) and \(|S_{21}|^2 = 1 - |S_{11}|^2\) [26, Sec. 4.3]. Finally, one can consider that the condition \(\angle S_{21} = -90^\circ\) is guaranteed by using (5) to calculate the values of \(B_i\) [8]. The derived conditions are valid at each frequency, independent of the value selected for \(f_c\) and \(Z_c\). As a consequence, only the \(S_{11}\) parameter can be considered in the analysis. It is given by:

\[
S_{11} = \frac{B - CZ_0^2}{B + CZ_0^2}
\]

(7)

where \(Z_0\) is the reference impedance of input and output ports. Substituting (6) in (7) leads to

\[
S_{11,f_i} = \frac{Z_c^2 \sin^2 \left(\frac{\pi f_i}{f_c}\right) - Z_0^2}{Z_c^2 \sin^2 \left(\frac{\pi f_i}{f_c}\right) + Z_0^2}
\]

(8)

The aim is to find the values of \(Z_c\) and \(f_c\), if they exist, that allow to obtain from the network in Fig. 1 the same behavior at the three operating frequencies. This task is thus represented by the following condition:

\[
|S_{11,f_1}| = |S_{11,f_2}| = |S_{11,f_3}|
\]

(9)
By substituting (8) in (9), the following sets of possible solutions are derived:

\[
\sin \left( \frac{\pi f_1}{2 f_c} \right) = \sin \left( \frac{\pi f_2}{2 f_c} \right) \quad Z_c = \frac{Z_0}{\sqrt{\sin \left( \frac{\pi f_1}{2 f_c} \right) \sin \left( \frac{\pi f_2}{2 f_c} \right)}} \quad (10a)
\]

\[
\sin \left( \frac{\pi f_2}{2 f_c} \right) = \sin \left( \frac{\pi f_3}{2 f_c} \right) \quad Z_c = \frac{Z_0}{\sqrt{\sin \left( \frac{\pi f_2}{2 f_c} \right) \sin \left( \frac{\pi f_3}{2 f_c} \right)}} \quad (10b)
\]

\[
\sin \left( \frac{\pi f_3}{2 f_c} \right) = \sin \left( \frac{\pi f_1}{2 f_c} \right) \quad Z_c = \frac{Z_0}{\sqrt{\sin \left( \frac{\pi f_3}{2 f_c} \right) \sin \left( \frac{\pi f_1}{2 f_c} \right)}} \quad (10c)
\]

By assuming \( Z_0 = Z_T \) and by manipulating (4), the following relations are obtained:

\[
\sin \left( \frac{\pi f_1}{2 f_c} \right) = \frac{Z_0}{Z_{c,1}} \quad (11a)
\]

\[
\sin \left( \frac{\pi f_2}{2 f_c} \right) = \frac{Z_0}{Z_{c,2}} \quad (11b)
\]

\[
\sin \left( \frac{\pi f_3}{2 f_c} \right) = \frac{Z_0}{Z_{c,3}} \quad (11c)
\]

Finally, by replacing (11) in the right side equations in (10), the possible sets of solutions for \( f_c \) and \( Z_c \) that verify the condition (9) are

\[
f_c = \frac{f_1 + f_2}{2} \quad Z_c = \sqrt{Z_{c,3} \cdot Z_{c,2}} \quad (12a)
\]

\[
f_c = \frac{f_1 + f_3}{2} \quad Z_c = \sqrt{Z_{c,2} \cdot Z_{c,1}} \quad (12b)
\]

\[
f_c = \frac{f_2 + f_3}{2} \quad Z_c = \sqrt{Z_{c,1} \cdot Z_{c,2}} \quad (12c)
\]

Among the three possible solutions in (12), the optimum one is represented by the solution that minimizes the \(|S_{11}|\). By substituting (10) and (12) in (8) and selecting \( i = 1 \), the following relations are derived for the \( S_{11} \) in the three cases:

\[
S_{11} = \frac{\sin \left( \pi \frac{f_1}{f_1 + f_2} \right) - \sin \left( \pi \frac{f_3}{f_1 + f_3} \right)}{\sin \left( \pi \frac{f_1}{f_1 + f_2} \right) + \sin \left( \pi \frac{f_3}{f_1 + f_3} \right)} \quad (13a)
\]

\[
S_{11} = \frac{\sin \left( \pi \frac{f_1}{f_1 + f_3} \right) - \sin \left( \pi \frac{f_2}{f_1 + f_2} \right)}{\sin \left( \pi \frac{f_1}{f_1 + f_3} \right) + \sin \left( \pi \frac{f_2}{f_1 + f_2} \right)} \quad (13b)
\]

\[
S_{11} = \frac{\sin \left( \pi \frac{f_2}{f_2 + f_3} \right) - \sin \left( \pi \frac{f_1}{f_2 + f_1} \right)}{\sin \left( \pi \frac{f_2}{f_2 + f_3} \right) + \sin \left( \pi \frac{f_1}{f_2 + f_1} \right)} \quad (13c)
\]

In Appendix 6 it is demonstrated that the \(|S_{11}|\) obtained from (13b) is the minimum respect to (13a) and (13c), independently by the selected operating frequencies. As a consequence, the optimum choice for \( f_c \) and \( Z_c \) is represented by (12b).

A graphical example that clarifies the inferred solution is reported in Fig. 2. For this example \( f_1 = 0.6 \text{ GHz}, f_2 = 0.9 \text{ GHz} \) and \( f_3 = 1.4 \text{ GHz} \) are assumed. The solid line in all graphs of Fig. 2 depicts the function (4) normalized to \( Z_T \) and plotted versus the normalized frequency \( f / f_c \). Moreover, the discrete frequency variable \( f_i \) in (4) has been replaced with the continuous one \( f \) to present the continuous behavior of the function. The symbols in the graphs of Fig. 2 are \( Z_{c,1}, Z_{c,2} \) and \( Z_{c,3} \) derived by (4). Furthermore,
Figure 2: Behavior of $Z_c$ from \((a)\) and values of $Z_{c,i}$ for a triple-band quarter-wave transmission line case by assuming $f_c$ as defined in \((a)\) equation \((12a)\), \((b)\) equation \((12b)\) and \((c)\) equation \((12c)\). For this example $f_1 = 0.6$ GHz, $f_2 = 0.9$ GHz and $f_3 = 1.4$ GHz are assumed.
equations (12a), (12b) and (12c) have been used to define \( f_c \) in Fig. 2-a, Fig. 2-b and Fig. 2-c, respectively. It is possible to note that the case reported in Fig. 2-b is the one that minimizes the distance between the largest \( (Z_{c,max}) \) and smallest \( (Z_{c,min}) \) values of the three \( Z_{c,i} \). As a consequence, the value derived from (12b) for \( Z_c \) is as close as possible to all the ideal \( Z_{c,i} \), allowing to obtain a better \(|S_{11}|\) parameter for the network in Fig. 1.

Once we derived the optimum value for \( f_c \) and \( Z_c \), the shunted elements at each frequency \( (B_i) \) can be easily calculated by using (5). To synthesize the computed \( B_i \), many approaches could be addressed, based on both distributed and/or lumped elements [21, 24, 27–29]. An optimum solution cannot be generalized since it depends on application constraints like size, losses, repeatability, cost, easiness of realization, robustness, model availability and so on. Obviously, considering mass production, the repeatability is in general much more important than losses, while it could be the opposite for a single specialized design. As a consequence, one can consider the approach here adopted as one of the possible solutions and not necessarily the unique and/or the best one. In this work we have chosen to implement the Impedance Buffer Methodology, already proposed in [27, 30]. Such an approach allows arbitrary reactive loads to be synthesized at an unlimited number of arbitrary frequencies. Moreover, it has the advantages of being based on closed form design equations and to being easily implemented by using distributed planar elements. The structure obtained with the Impedance Buffer Methodology is the ladder network schematically shown in Fig. 3. Starting from the input port of the network \( (P_1) \) in Fig. 3, the operating frequencies are controlled in descending order, i.e., from \( f_3 \) to \( f_1 \). The impedance buffers at \( f_3 \) and \( f_2 \) are realized by means of a 90° open circuit stub, while the one at \( f_1 \) is obtained with a ground connection to reduce the size of the structure. Obviously, depending on the actual application, this may or may not be a desirable feature. The electrical length of each series transmission line \( (\theta_1, \theta_2 \text{ and } \theta_3) \) in Fig. 3 can be directly computed from the desired \( B_i \) values and the operating frequencies as described in [30].

### 2.3 Generalization for an arbitrary number of frequencies

The approach presented in the previous subsection can be easily generalized for an arbitrary number \( (N) \) of uncorrelated frequencies (i.e. \( f_1 < f_2 < \cdots < f_N \)). Increasing the number of frequencies, in fact, means increasing the values of \( Z_{c,i} \) obtained from (4), as graphically highlighted in Fig. 4. In such a graph each symbol indicates examples of hypothetical \( Z_{c,i} \) values for each normalized frequency.

Once again an optimum trade-off has to be adopted to select the design parameters, since only one value is usable for the actual implementation of \( Z_c \). However, the higher number of frequencies does not increase
Figure 4: Behavior of $Z_c$ from (4) and values of $Z_{c,i}$ for a multi-band quarter-wave transmission line case. For this example $f_1 = 0.5$ GHz, $f_2 = 0.6$ GHz, $f_3 = 0.7$ GHz, $f_4 = 1.15$ GHz, $f_5 = 1.25$ GHz and $f_N = 1.5$ GHz are assumed. Other arbitrary operating frequencies are supposed in the range 1.35-1.45 GHz as well.
the complexity of the problem. Looking at Fig. 4, it is possible to note that the general case can be traced to
the case of three frequencies. In fact, referring to Fig. 4, the design parameters $f_c$ and $Z_c$ can be selected as
demonstrated in the previous section, simply considering for the computation the frequencies $f_1$, $f_N$ and $f_4$.
Obtaining, thus, $|S_{11,f_1}| = |S_{11,f_4}| = |S_{11,f_N}|$. Moreover, the return loss at the other operating frequencies
is better than the one at $f_1$, $f_N$ and $f_4$, since the obtained value for $Z_c$ is closest to the ideal $Z_{c,i}$ of these
frequencies.

Thus, the generalized design equations for a multi-band quarter-wave transmission line derived by
applying this approach are the followings:

$$f_c = \frac{f_1 + f_N}{2}$$

(14a)

$$Z_{c,i} = \frac{Z_T}{\sin \left( \frac{\pi}{2} \cdot \frac{f_i}{f_c} \right)} \quad i = 1, 2 \ldots N$$

(14b)

$$Z_{c,m} = \min \{Z_{c,i} \} \quad i = 2, 3 \ldots N - 1$$

(14c)

$$Z_c = \sqrt{Z_{c,1} \cdot Z_{c,m}}$$

(14d)

$$B_i = \frac{1}{Z_c \cdot \tan \left( \frac{\pi}{2} \cdot \frac{f_i}{f_c} \right)} \quad i = 1, 2 \ldots N$$

(14e)

To synthesize the $B_i$ susceptances for an arbitrary number of operating frequencies, the Impedance Buffer
Methodology can be adopted also in this case. This is accomplished by adding an impedance buffer and a
series transmission line for each further frequency in Fig. 3.

2.4 Limitations of multi-band quarter-wave transmission lines

This subsection is focused on the analysis of the limitations of the multi-band quarter-wave transmission
line synthesis presented in the previous subsections. The synthesis method is oriented to identify the best
trade-off that equalizes the scattering parameters, and in particular the $|S_{11}|$ parameter, across all the operating
frequencies. However, the absolute $|S_{11}|$ value depends on the relation between the operating frequencies.
For example, Fig. 5 reports two hypothetical cases of $Z_{c,i}$. For sake of clarity, only the boundary values are
reported, i.e., $Z_{c,1}$, $Z_{c,N}$ and $Z_{c,m}$. In both cases the same $f_1$ and $f_N$ are assumed, resulting in the same $f_c$,
while the value of $f_m$ is different, resulting in a different value for the actual $Z_c$ from (14d). In particular,
the spread between $Z_{c,1}$ and $Z_{c,m}$ in Case-II is smaller than the one of Case-I. Consequently, the $|S_{11}|$
available in Case-II is better than the one resulted in Case-I, even if the optimum trade-off is adopted for
both.

From the designer point of view it is useful to establish the matching limitation of the structure directly
from the operating frequencies. Considering that the worst matching condition occurs simultaneously at $f_1$, $f_m$ and $f_N$, it is possible to estimate the achievable matching simply computing the $|S_{11}|$ at $f_1$ from (13):

$$|S_{11,f_1}| = \frac{\left| \sin \left( \frac{\pi}{2} \cdot \frac{f_1}{f_1 + f_N} \right) - \sin \left( \frac{\pi}{2} \cdot \frac{f_m}{f_1 + f_N} \right) \right|}{\left| \sin \left( \frac{\pi}{2} \cdot \frac{f_1}{f_1 + f_N} \right) + \sin \left( \frac{\pi}{2} \cdot \frac{f_m}{f_1 + f_N} \right) \right|}$$

(15)

To have an idea of the matching limitations, Fig. 6 reports the behavior of (15). For illustrative purposes, the
frequency axis has been normalized with the function

$$f_{\text{norm}} = \frac{2f - (f_1 + f_N)}{f_N - f_1}$$

(16)
Figure 5: Behavior of $Z_c$ from (4) and two cases of $Z_{c,i}$ having different matching limitations. For both cases $f_1 = 0.5$ GHz and $f_N = 1.5$ GHz are assumed, resulting in the same $f_c$, $Z_{c,1}$ and $Z_{c,N}$ values. $f_m = 0.85$ GHz and $f_m = 0.6$ GHz are assumed for Case-I and Case-II, respectively.

Consequently, the values $f_{norm} = -1$ and $f_{norm} = 1$ represent the frequencies $f_1$ and $f_N$, respectively, independent of their ratio and absolute value. Moreover, $f_m$ can assume any value between $-1$ and $1$, resulting in $f_{norm} = 0$ for the case $f_m = f_c$.

Referring to Fig. 6, the achievable matching degrades when the ratio between $f_N$ and $f_1$ increases. At the same time, it depends on the relative position of $f_m$, resulting in the worst condition for the case $f_m = f_c$, where also the spread between $Z_{c,1\&N}$ and $Z_{c,m}$ is largest.

2.5 From the multi-band quarter-wave transmission line to the multi-band branch-line coupler

The single-band branch-line coupler is obtained by properly combining four single-band quarter-wave transmission lines, as reported in Fig. 7-(a). To achieve the multi-band branch-line coupler topology, each single-band quarter-wave transmission line has to be replaced with the multi-band equivalent one, following the design methodology described above. Such a procedure leads to a structure similar to the one depicted in Fig. 7-(b). In particular, the values $Z_{c,a}$ and $Z_{c,b}$ are derived substituting $Z_T = Z_a$ and $Z_T = Z_b$ in (14b), respectively, where $Z_a = Z_0\sqrt{2}$ and $Z_b = Z_0$ are the characteristic impedances adopted in the single-band branch line coupler, as shown in Fig. 7-(a) [26]. Such operation allows the values of $B_{i,a}$ and $B_{i,b}$ to be calculated as well. Their shunt connection, i.e., algebraic sum, leads to the susceptances $B_i$ in Fig. 7-(b). Finally, adopting the Impedance Buffer Methodology, a multi-band network having the form depicted in Fig. 7-(c) is derived to synthesize the proper $B_i$ susceptance at each operating frequency.
2.6 Limitations of multi-band branch-line couplers

Previously, it has been demonstrated that selecting $Z_c = \sqrt{Z_{c,1} \cdot Z_{c,m}}$ allows the matching error in a multi-band quarter-wave transmission line to be equalized. However, the effect that such choice has on the branch-line coupler in terms of matching, balance and isolation conditions should be verified. The analytical demonstration is presented in Appendix E. The results show that, by applying the same trade-off for the characteristic impedances of the multi-band quarter-wave transmission lines also in the branch-line coupler, the error in the mismatch, imbalance and isolation performance is equally distributed between $f_1$, $f_m$ and $f_N$. At the same time, it is demonstrated that the phase relation between the signals at port 2 and port 3 is equal to $90^\circ$ at each operating frequency, allowing the desired quadrature relation to be obtained.

As was previously demonstrated for the multi-band quarter-wave transmission line, it is also possible to relate the limitations of the multi-band branch-line coupler directly to the operating frequencies. Referring to Appendix F the matching ($|S_{11}|$), balancing ($|S_{21}| / |S_{31}|$) and isolation ($|S_{41}|$) limitations are given by

\begin{align}
|S_{11}| &= \frac{\sin^2 \theta_1 - \sin^2 \theta_m}{\sin^2 \theta_1 + 6 \sin \theta_1 \sin \theta_m + \sin^2 \theta_m} \quad (17a) \\
|S_{21}| &= \frac{\sin \theta_1 + \sin \theta_m}{2 \sqrt{\sin \theta_1 \sin \theta_m}} \quad (17b) \\
|S_{31}| &= \frac{\sqrt{\sin \theta_1 \sin \theta_m (\sin \theta_1 - \sin \theta_m)}}{\sin^2 \theta_1 + 6 \sin \theta_1 \sin \theta_m + \sin^2 \theta_m} \quad (17c)
\end{align}

where $\theta_1 = \frac{\pi f_1}{f_1 + f_N}$ and $\theta_m = \frac{\pi f_m}{f_1 + f_N}$. Fig. 8 reports the behaviors of (17) as function of $f_m$ and the ratio $f_N / f_1$, applying the frequency normalization defined in (16).

The behaviors in Fig. 8 highlight that the worst condition for the multi-band branch-line coupler limitations occur for the case $f_m = f_1$, as was also obtained for the multi-band quarter-wave transmission line. However,
Figure 7: Topology of (a) single-band branch-line coupler, (b) multi-band branch-line coupler and (c) multi-band network for the synthesis of the $B_i$ susceptances.
Figure 8: Matching (a), balancing (b) and isolation (c) limitations for multi-band branch-line couplers versus normalized frequency $f_{\text{norm}}$ as defined in (16).

Comparing Fig. 8(a) and Fig. 8(b) it is evident that the branch-line coupler permits a better matching performance compared to the multi-band quarter-wave transmission line for the same $f_m$ and $f_N/f_1$ condition. Moreover, the imbalance performance, reported in Fig. 8(b), increases for higher ratio $f_N/f_1$. However, the balance performance is maintained lower than 0.5 dB up to $f_N/f_1 = 5$. Finally, referring to Fig. 8(c), it is possible to note that the behavior of the isolation between port 1 and port 4 is similar to the one of the matching.

III. IMPLEMENTATION OF TEST CIRCUITS

Dual-, triple-, and quad-band branch-line couplers were implemented to demonstrate the validity of the multi-band branch-line coupler synthesis approach. All the designed branch-line couplers were implemented on a Rogers 5870 substrate with $\varepsilon_r = 2.33$ and thickness of 0.787 mm.
3.1 Dual-band branch-line coupler

For the dual-band branch-line coupler, the selected operating frequencies are \( f_1 = 2.4 \) GHz and \( f_2 = 3.5 \) GHz, resulting in \( f_c = 2.95 \) GHz. The theoretical design parameters are summarized in Table 1. In particular, the column \( Z_a = 50/\sqrt{2} \) \( \Omega \) reports the design parameters derived by assuming \( Z_T = Z_a \) in (14b), while the column \( Z_b = 50 \) \( \Omega \) reports the design parameters derived by assuming \( Z_T = Z_b \) in (14b). The photo of the realized dual-band branch-line coupler is shown in Fig. 9(a).

Table 1: Design parameters of the dual-, triple-, and quad-band branch-line couplers

<table>
<thead>
<tr>
<th></th>
<th>( Z_a = 50/\sqrt{2} ) ( \Omega )</th>
<th>( Z_b = 50 ) ( \Omega )</th>
</tr>
</thead>
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<tr>
<td><strong>Dual-band branch-line coupler</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( Z_{c,1} = Z_{c,2} = Z_c ) (( \Omega ))</td>
<td>36.9</td>
<td>52.2</td>
</tr>
<tr>
<td>( B_1 = -B_2 ) (( mS ))</td>
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<td>5.8</td>
</tr>
<tr>
<td><strong>Triple-band branch-line coupler</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( Z_{c,1} = Z_{c,3} ) (( \Omega ))</td>
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<td>68.0</td>
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<tr>
<td>( Z_{c,2} ) (( \Omega ))</td>
<td>36.5</td>
<td>51.6</td>
</tr>
<tr>
<td>( Z_c ) (( \Omega ))</td>
<td>41.9</td>
<td>59.2</td>
</tr>
<tr>
<td>( B_1 = -B_3 ) (( mS ))</td>
<td>22.0</td>
<td>16.0</td>
</tr>
<tr>
<td>( B_2 ) (( mS ))</td>
<td>6.0</td>
<td>4.3</td>
</tr>
<tr>
<td><strong>Quad-band branch-line coupler</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( Z_{c,3} ) (( \Omega ))</td>
<td>37.8</td>
<td>53.4</td>
</tr>
<tr>
<td>( B_3 ) (( mS ))</td>
<td>-9.0</td>
<td>-6.3</td>
</tr>
</tbody>
</table>

Figure 9: Photos of the realized (a) dual-band, (b) triple-band and (c) quad-band branch line couplers, whose sizes are \( 65 \times 51 \) mm\(^2\), \( 75 \times 82 \) mm\(^2\) and \( 73 \times 70 \) mm\(^2\), respectively. The network based on the Impedance Buffer Methodology that synthesizes the desired values of \( B_i \) is highlighted in each figure by means of a white frame.
3.2 Triple-band branch-line coupler

For the triple-band branch-line coupler, the arbitrarily selected operating frequencies are \( f_1 = 1.5 \text{ GHz} \), \( f_2 = 2.4 \text{ GHz} \) and \( f_3 = 4.2 \text{ GHz} \), resulting in \( f_c = 2.85 \text{ GHz} \). The theoretical design parameters are summarized in Table 1.

For the triple-band branch-line coupler it is possible to estimate the performance limitations. In particular, selecting \( f_m = f_2 \) and \( f_N = f_3 \) in (17), it follows for the matching \( |S_{11}| = -23.2 \text{ dB} \), for the balance \( |S_{21}|/|S_{31}| = 0.082 \text{ dB} \) and for the isolation \( |S_{41}| = -23.3 \text{ dB} \). The photo of the realized triple-band branch-line coupler is shown in Fig. 9-(b).

3.3 Quad-band branch-line coupler

For the quad-band branch-line coupler, the selected operating frequencies are \( f_1 = 1.5 \text{ GHz} \), \( f_2 = 2.4 \text{ GHz} \), \( f_3 = 3.5 \text{ GHz} \) and \( f_4 = 4.2 \text{ GHz} \), resulting in \( f_c = 2.85 \text{ GHz} \), as for the triple-band branch-line coupler. \( f_1, f_2 \) and \( f_4 \) coincide with the triple-band coupler example, resulting in the same theoretical design parameters. The additional design parameters at \( f_3 \) are summarized in Table 1. Comparing the \( Z_c, i \) in Table 1 for the triple-band and quad-band couplers, the condition \( Z_{c,m} = Z_{c,2} \) is derived for the quad-band branch-line coupler, resulting in the same \( Z_c \) values as for the triple-band branch-line coupler.

Since the values of \( f_1, f_m = f_2 \) and \( f_N = f_4 \) for the quad-band branch-line coupler are the same of the triple-band one, the same performance limitations are obtained from (17). The photo of the realized quad-band branch-line coupler is shown in Fig. 9-(c).

Comparing the layouts of the three realized branch-line couplers in Fig. 9, it is possible to note that the increased number of operating frequencies, from the dual-band to the quad-band branch-line coupler, is achieved simply adding a further ladder cell (series transmission line and parallel stub) to the network based on the Impedance Buffer Methodology.

IV. EXPERIMENTAL RESULTS

Fig. 10 reports the simulated and measured scattering parameters of the designed branch-line couplers. In particular, the figure compares simulations based on ideal elements, from hereafter denoted ideal performance, with electromagnetic simulations of the structures.

The ideal performance of the dual-band branch-line coupler (Fig. 10-(a)) confirms the capability of the topology to behave as a perfect branch-line coupler at two frequencies simultaneously. The matching, balance and isolation performance are, in fact, fully satisfied.Passing from ideal to real elements, the performance of the branch-line coupler are degraded, due to the non-ideal behavior of actual microstrip lines and cross/tee junctions. Obviously, such an effect is more significant at the highest frequency. However, the measured behaviors are well predicted by the theory and simulations.

The ideal performance of the triple-band branch-line coupler (Fig. 10-(b)) verify the matching, balance and isolation limitations theoretically predicted. Also for this circuit, the greatest degradation has been registered at the highest band, 4.2 GHz, passing to actual elements. However, the measured results show satisfactory levels of matching, balance and isolation at each of the operating band.

The ideal performance of the quad-band branch-line coupler (Fig. 10-(c)) further verifies the theoretical analysis. For example, the ideal \( |S_{11}| \) level of the quad-band branch-line coupler at 1.5 GHz, 2.4 GHz and 4.2 GHz is the same obtained from the triple-band branch-line coupler, while the level at 3.5 GHz is better, as theoretically predicted by analyzing the performance limitations. Finally, the measured performance is well in agreement with the theoretical and simulated one.

Table 2 summarizes the measured performance for each realized branch-line coupler, reporting also the amplitude (\( \Delta A = |S_{21}/S_{31}| \)) and phase (\( \Delta \phi = \angle S_{21} - \angle S_{31} \)) balance at the center frequencies. The bandwidths (BW) at \( \Delta A = 1 \text{ dB} \) and \( \Delta \phi = 90^\circ \pm 5^\circ \) are also added in the table for completeness.
has to remark that the data reported in Table 2 exactly refer to the selected operating frequencies, neglecting the little frequency shift the realized prototypes have shown after due to the process variances. In particular, a bit higher frequency shift has been registered for the three-band branch-line coupler prototype.

V. CONCLUSIONS

A novel design approach for multi-band branch-line couplers is introduced. The main advantages of this approach are the arbitrary choice of the operating bands, the simple structure, and the ease of fabrication. The complete theoretical analysis of the topology is presented, leading to a closed form equations system for its design. Three couplers based on the proposed structure are implemented for dual-, triple-, and quad-band operation to validate the methodology. Measurement results, in terms of matching, isolation and amplitude and phase balance, show good agreement with simulated ones and demonstrate the desired behavior of the branch-line couplers.

VI. APPENDIX A: DERIVATION OF THE MINIMUM $|S_{11}|$

The aim of this appendix is to demonstrate that the magnitude of (13b) is lower than (13a) and (13c). To fulfill this result, one has to consider that each sine function in (13) has to produce a positive value to obtain positive, i.e. realistic, value for the $Z_{c,i}$ from (4). This condition imposes the limitation

$$f_3 < f_1 + f_2$$

(18)

due to the term

$$\sin \left( \pi \frac{f_3}{f_1 + f_2} \right)$$

in (13a). Obviously, the limitation in (18) has to be accounted for only if the possible solution in (12a) is adopted for the design.

To demonstrate that the magnitude of (13b) is lower than the one of (13a), one has to verify, regardless of the operating frequencies, the following inequality:

$$\left| \frac{\sin \alpha - \sin \beta}{\sin \alpha + \sin \beta} \right| > \left| \frac{\sin \gamma - \sin \delta}{\sin \gamma + \sin \delta} \right|$$

(19)

where

$$\alpha = \pi \frac{f_1}{f_1 + f_2}$$

(20a)

$$\beta = \pi \frac{f_3}{f_1 + f_2}$$

(20b)

$$\gamma = \pi \frac{f_1}{f_1 + f_3}$$

(20c)

$$\delta = \pi \frac{f_2}{f_1 + f_3}$$

(20d)

Accounting for (20) and (18), it is possible to note that

$$\sin \alpha > \sin \beta$$

(21a)

$$\sin \delta > \sin \gamma$$

(21b)
regardless of the operating frequencies. As a consequence, the magnitude in (19) can be removed, leading to
\[
\frac{\sin \alpha - \sin \beta}{\sin \alpha + \sin \beta} > \frac{\sin \delta - \sin \gamma}{\sin \delta + \sin \gamma}
\] (22)
that is equivalent to [31]
\[
\frac{\tan \left( \frac{\alpha - \beta}{2} \right)}{\tan \left( \frac{\alpha + \beta}{2} \right)} > \frac{\tan \left( \frac{\delta - \gamma}{2} \right)}{\tan \left( \frac{\delta + \gamma}{2} \right)}
\] (23)
Accounting for (20) and (18), the following constraints can be obtained:
\[
\begin{align*}
0 & > \frac{\alpha - \beta}{2} > -\frac{\pi}{2} \\
\frac{\pi}{2} & > \frac{\alpha + \beta}{2} > \pi \\
0 & > \frac{\delta - \gamma}{2} > \frac{\pi}{2} \\
0 & > \frac{\delta + \gamma}{2} > \frac{\pi}{2}
\end{align*}
\] (24a-d)
The inequality in (23) is definitely ascertained whether
\[
\begin{align*}
\left| \frac{\alpha - \beta}{2} \right| & > \left| \frac{\delta - \gamma}{2} \right| \\
\left| \frac{\alpha + \beta}{2} \right| & < \left| \frac{\delta + \gamma}{2} \right|
\end{align*}
\] (25a-b)
that, accounting for (24), can be verified by the following inequalities:
\[
\begin{align*}
\left| \frac{\alpha - \beta}{2} \right| & > \left| \frac{\delta - \gamma}{2} \right| \\
\pi - \left| \frac{\alpha + \beta}{2} \right| & < \left| \frac{\delta + \gamma}{2} \right|
\end{align*}
\] (26a-b)
By substituting (20) in (26), the following conditions are obtained:
\[
\begin{align*}
f_3 & > f_2 \\
(f_3 - f_2)^2 & > 0
\end{align*}
\] (27a-b)
Since the two conditions in (27) are always true, the inequality in (19) is verified. The same analysis can be adopted to compare (13b) and (13c). The result confirms that the magnitude of (13b) is lower than the one of (13a) and (13c) regardless of the operating frequencies.

VII. APPENDIX B: SCATTERING PARAMETERS DERIVATION

In Section 2 it has been demonstrated that the ABCD-matrix of the multi-band quarter-wave transmission line is equal for \( f_1 \) and \( f_3 \) or \( f_N \) in the general case. The multi-band branch-line coupler is a combination of multi-band quarter-wave transmission lines, consequently its behavior at \( f_1 \) is the same as the one at \( f_N \). Hence, the behavior at \( f_N \) can be omitted, considering only the one at \( f_1 \). At \( f_1 \) each branch of the branch-line coupler behaves as a quarter-wave transmission line, whose characteristic impedance is
\[
Z_{a,f_1} = Z_{c,a} \cdot \sin \theta_1
\] (28)
for the horizontal branches in Fig. 7(b) and

\[ Z_{b,f_1} = Z_{c,b} \cdot \sin \theta_1 \]  

(29)

for the vertical branches in Fig. 7(b), where \( \theta_1 = \frac{\pi}{2} \frac{f_1}{f_c} \). Assuming the definition of \( Z_{c,a} \) and \( Z_{c,b} \) in (14b) it follows

\[ Z_{a,f_1} = Z_a \cdot \sqrt{\frac{\sin \theta_1}{\sin \theta_m}} = Z_0 \cdot \sqrt{\frac{\sin \theta_1}{\sin \theta_m}} \]  

(30a)

\[ Z_{b,f_1} = Z_b \cdot \sqrt{\frac{\sin \theta_1}{\sin \theta_m}} = Z_0 \cdot \sqrt{\frac{\sin \theta_1}{\sin \theta_m}} \]  

(30b)

where \( \theta_m = \frac{\pi}{2} \frac{f_m}{f_c} \). The S-parameters of a branch-line coupler as function of the even/odd-mode S-parameters are [32]

\[ S_{11} = \frac{S_{11}^e + S_{11}^o}{2} \quad S_{21} = \frac{S_{11}^e - S_{11}^o}{2} \quad S_{31} = \frac{S_{31}^e - S_{31}^o}{2} \quad S_{41} = \frac{S_{31}^e + S_{31}^o}{2} \]  

(31)

where the even/odd-mode S-parameters are given by [32]

\[ S_{11}^e = -Y_0^2 + \frac{Y_A^2 - Y_B^2}{Y_0^2 + Y_A^2 - Y_B^2 + 2jY_BY_0} \]  

(32a)

\[ S_{11}^o = Y_0^2 + \frac{Y_A^2 - Y_B^2}{Y_0^2 + Y_A^2 - Y_B^2 + 2jY_BY_0} \]  

(32b)

\[ S_{21}^o = -j2Y_0^2 + \frac{Y_AY_0}{Y_A^2 - Y_B^2 + 2jY_BY_0} \]  

(32c)

\[ S_{21}^o = -j2Y_0^2 + \frac{Y_AY_0}{Y_A^2 - Y_B^2 + 2jY_BY_0} \]  

(32d)

where \( Y_0 = 1/Z_0 \) is the port admittance, \( Y_A \) and \( Y_B \) are the characteristic admittance of the series quarterwave transmission line and the admittance of the \( \lambda/8 \) open stub due to the even/odd-mode analysis, respectively. Applying (30) at \( f_1 \) yields

\[ Y_A = \frac{\sqrt{2}}{Z_0} \cdot \sqrt{\frac{\sin \theta_m}{\sin \theta_1}} \]  

(33a)

\[ Y_B = \frac{1}{Z_0} \cdot \sqrt{\frac{\sin \theta_m}{\sin \theta_1}} \]  

(33b)

Replacing (33) in (32) and, subsequently, in (31), the S-parameters of the multi-band branch-line coupler at \( f_1 \) are inferred:

\[ S_{11,f_1} = \frac{\sin^2 \theta_1 - \sin^2 \theta_m}{\sin^2 \theta_1 + 6 \sin \theta_1 \sin \theta_m + \sin^2 \theta_m} \]  

(34a)

\[ S_{21,f_1} = -2j\sqrt{2} Y_0 \cdot \frac{\sqrt{\sin \theta_1 \sin \theta_m (\sin \theta_1 + \sin \theta_m)}}{\sin^2 \theta_1 + 6 \sin \theta_1 \sin \theta_m + \sin^2 \theta_m} \]  

(34b)

\[ S_{31,f_1} = -4\sqrt{2} \cdot \frac{\sin \theta_1 \sin \theta_m}{\sin^2 \theta_1 + 6 \sin \theta_1 \sin \theta_m + \sin^2 \theta_m} \]  

(34c)

\[ S_{41,f_1} = -2j \cdot \frac{\sqrt{\sin \theta_1 \sin \theta_m (\sin \theta_1 - \sin \theta_m)}}{\sin^2 \theta_1 + 6 \sin \theta_1 \sin \theta_m + \sin^2 \theta_m} \]  

(34d)
Following the same procedure for $f_m$, it is possible to derive:

\[
Z_{a,f_m} = Z_a \cdot \sqrt{\frac{\sin \theta_m}{\sin \theta_1}} = Z_0 \cdot \sqrt{\frac{\sin \theta_m}{\sin \theta_1}}
\]

(35a)

\[
Z_{b,f_m} = Z_b \cdot \sqrt{\frac{\sin \theta_m}{\sin \theta_1}} = Z_0 \cdot \sqrt{\frac{\sin \theta_m}{\sin \theta_1}}
\]

(35b)

therefore

\[
Y_A = \frac{\sqrt{2}}{Z_0} \cdot \sqrt{\frac{\sin \theta_1}{\sin \theta_m}}
\]

(36a)

\[
Y_B = \frac{1}{Z_0} \cdot \sqrt{\frac{\sin \theta_1}{\sin \theta_m}}
\]

(36b)

and finally

\[
S_{11,f_m} = \frac{\sin^2 \theta_m - \sin^2 \theta_1}{\sin^2 \theta_1 + 6 \sin \theta_1 \sin \theta_m + \sin^2 \theta_m}
\]

(37a)

\[
S_{21,f_m} = -j2\sqrt{2} \cdot \frac{\sin \theta_1 \sin \theta_m (\sin \theta_1 + \sin \theta_m)}{\sin^2 \theta_1 + 6 \sin \theta_1 \sin \theta_m + \sin^2 \theta_m}
\]

(37b)

\[
S_{31,f_m} = -4\sqrt{2} \cdot \frac{\sin \theta_1 \sin \theta_m}{\sin^2 \theta_1 + 6 \sin \theta_1 \sin \theta_m + \sin^2 \theta_m}
\]

(37c)

\[
S_{41,f_m} = -j2 \cdot \frac{\sin \theta_1 \sin \theta_m (\sin \theta_m - \sin \theta_1)}{\sin^2 \theta_1 + 6 \sin \theta_1 \sin \theta_m + \sin^2 \theta_m}
\]

(37d)

Comparing (34) and (37), one can easily show that these expressions lead to identical matching, balance and isolation properties at $f_1$ and $f_m$. Moreover, (34b)-(34c) and (37b)-(37c) demonstrate that the adopted topology satisfies the quadrature condition for both $f_1$ and $f_m$, i.e. 90° of phase shift between $S_{21}$ and $S_{31}$.

\section*{VII. References}


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<th>Parameter</th>
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<th>3.5 GHz</th>
<th>4.2 GHz</th>
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<td>$</td>
<td>S_{11}</td>
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<tr>
<td>$</td>
<td>S_{21}</td>
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<td>-</td>
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<td>&gt;1000</td>
<td>-</td>
</tr>
<tr>
<td><strong>Triple-band branch-line coupler</strong></td>
<td></td>
<td></td>
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<tr>
<td>$</td>
<td>S_{11}</td>
<td>$ (dB)</td>
<td>-15.54</td>
<td>-17.29</td>
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<tr>
<td>$</td>
<td>S_{21}</td>
<td>$ (dB)</td>
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<td>-3.46</td>
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<td>$</td>
<td>S_{31}</td>
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<td>-3.39</td>
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<td>$</td>
<td>S_{41}</td>
<td>$ (dB)</td>
<td>-17.12</td>
<td>-16.53</td>
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<tr>
<td>$\Delta A$ (dB)</td>
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<td>0.07</td>
<td>-</td>
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<tr>
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<td>88.45</td>
<td>-</td>
<td>92.89</td>
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<tr>
<td>BW at $\Delta A = 1$ dB (MHz)</td>
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<td>250</td>
<td>-</td>
<td>300</td>
</tr>
<tr>
<td>BW at $\Delta \phi = 90^\circ \pm 5^\circ$ (MHz)</td>
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<td>160</td>
<td>-</td>
<td>190</td>
</tr>
<tr>
<td><strong>Quad-band branch-line coupler</strong></td>
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<td></td>
<td></td>
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<tr>
<td>$</td>
<td>S_{11}</td>
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<td>$ (dB)</td>
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<tr>
<td>$\Delta A$ (dB)</td>
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<tr>
<td>$\Delta \phi$ (degree)</td>
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<td>BW at $\Delta A = 1$ dB (MHz)</td>
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<td>390</td>
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<tr>
<td>BW at $\Delta \phi = 90^\circ \pm 5^\circ$ (MHz)</td>
<td>110</td>
<td>210</td>
<td>410</td>
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Figure 10: Measured and simulated results of the (a) dual-band, (b) triple-band and (c) quad-band branch line couplers.
Paper G

Design of a Concurrent Dual-Band 1.8 GHz-2.4 GHz GaN-HEMT Doherty Power Amplifier

Paul Saad, Paolo Colantonio, Luca Piazzon, Franco Giannini, Kristoffer Andersson, and Christian Fager

Abstract—In this paper, the design, implementation and experimental results of a high efficiency dual-band GaN-HEMT Doherty power amplifier (DPA) are presented. An extensive discussion about the design of the passive structures is presented showing different possible topologies of the dual-band DPA. One of the proposed topologies is used to design a dual-band DPA in hybrid technology for the frequency bands 1.8 GHz and 2.4 GHz with the second efficiency peak at 6 dB output power back-off (OBO). For a continuous wave output power of 20 W, the measured power added efficiency is 64 % and 54 % at 1.8 GHz and 2.4 GHz, respectively. At 6 dB OBO, the resulting measured Power-Added Efficiency (PAE) were 60 % and 44 % in the two frequency bands. Linearized concurrent modulated measurement using 10 MHz LTE signal with 7 dB Peak-to-Average-Ratio (PAR) at 1.8 GHz and 10 MHz WiMAX signal with 8.5 dB PAR at 2.4 GHz shows an average PAE of 34 %, at an adjacent channel leakage ratio of -48 dBc and -46 dBc at 1.8 GHz and 2.4 GHz, respectively.

Index Terms—Doherty power amplifier, dual-band amplifier, dual-band matching networks, GaN-HEMT, high efficiency, power amplifier.

I. INTRODUCTION

The fast development of wireless communication systems and the roll-out of new standards, such as Worldwide Interoperability for Microwave Access (WiMAX) and 4G Long Term Evolution (LTE), requires that the mobile radio base stations support multiple bands and process several types of standards [1]. Consequently there is an increasing demand of multi-band, multi-standard wireless transceivers able to simultaneously manage different types of signals. In this context, Software Defined Radio (SDR) is a feasible solution for reconfigurable radios, which can perform the same functions at different frequencies/modulations using the same hardware [2]. However, it is at the RF front-end stage that it becomes problematic to satisfy the multiband/multistandard features. The power amplifier (PA) is a key component in multi-band or multi-standard solutions, since its performance strongly influence the overall system performance in terms of bandwidth, output power, and efficiency [3], [4].

Modulated signals in modern wireless communication systems have large amplitude variations, which results in high peak-to-average ratios (PAR), sometimes exceeding 10 dB. To prevent clipping of the signal peaks and thereby strong distortion of the transmitted information, the PA has to operate at an average output power far from the saturation region and hence, at low efficiency levels.

Different techniques have been proposed to increase the average efficiency of power amplifiers for signals having high PAR. Envelope elimination and restoration (EER) [5], envelope tracking (ET) [6], Doherty amplifiers [7], and varactor based dynamic load modulation [8] are the most common. The ease of configuration and the circuit simplicity give the DPA many advantages over the other techniques. In DPA, high average efficiency is achieved by dynamically adapting the PA load impedance to keep the amplifier in compression during modulation [7], [9]–[11].

So far, a lot of work has been done on narrow-bandDPAs, where the efficiency was improved at back-off operation and high linearity performance was achieved with the help of digital predistortion techniques or by utilizing the intermodulation cancellation [4], [11]–[20]. However, most of the published Doherty PAs were designed to work in a single band and therefore they do not satisfy the multi-band, multi-standard requirements of the modern radio base-stations.

To overcome this major limitation, new design techniques have been used to increase the bandwidth of the DPA [21]– [24]. The drawback is that wide-band DPAs do not always have ideal operation over the bandwidth of operation. This leads to significant degradation in the DPA performance compared to the case where DPAs are designed and optimized for single frequency operation.

Recently, there have been some efforts to optimize a DPA for dual-band operation. Unfortunately, the first prototype of dual band DPA reported in [25] was working in the first band only, due to intrinsic effects of device packaging in the second band. A working dual-band DPA, operating at 880 MHz and 1.96 GHz, was proposed in [26] and recently a linearization solution for such amplifier was proposed in [27].

In this paper, a detailed design methodology for high efficiency dual-band DPA is reported and validated by successfully state-of-the-art experimental results. The procedure is based on load-pull/source-pull simulation approach together with a comprehensive design of the passive structures of the DPA. Comparison between the performance of the presented...
DPA with recently published single-band and dual-band DPAs are summarized in Table I. The dual-band DPA shows similar or even better performance when compared with single-band DPAs, because the design is optimized for the two frequency bands without any significant trade-off. The comparison with recently published dual-band DPAs shows the superior performance of the designed DPA and thereby demonstrates the usefulness of the proposed approach for the design of DPAs for future wireless systems.

This paper is organized as follows. In Sec. II the description of conventional Doherty architecture and the design issues and approaches for a dual band design are extensively discussed. In Sec. III the design strategy is presented, while the designed dual band DPA is discussed in Sec. IV. The experimental results are presented in Sec. V, and conclusions are given in Sec. VI.

II. DESIGN ISSUES IN A DUAL BAND DOHERTY POWER AMPLIFIER

The architecture and operation principle of Doherty amplifiers have been thoroughly discussed in the literature [7], [13], [15], [30]. Fig. 1 shows a block diagram of a conventional DPA, which is composed of the combination of two PAs (Main and Auxiliary), an Input Power Splitter (IPS), a Phase Compensation Network (PCN), an Impedance Inverter Network (IIN), and an Impedance Transformer Network (ITN) at the output to match towards 50Ω terminations.

![Conventional DPA topology](image)

**Figure 1.** Conventional DPA topology. $R_M$ and $R_A$ are the loads seen by the Main and Auxiliary amplifiers.

The Main amplifier is usually biased in Class-AB, while the Auxiliary amplifier is biased in Class-C. The Main and Auxiliary amplifiers are combined through the IIN, usually implemented using a quarter wave transmission line, with the aim to modulate the load impedance of the Main amplifier through the current supplied by the Auxiliary amplifier into the external load [4]. Thus, the DPA operates at a nearly constant efficiency for a targeted output power back-off range, typically of 6 dB.

In order to obtain a dual-band operation in a DPA, the passive structures, such as Main and Auxiliary matching networks, IPS, PCN, IIN, and ITN, must be designed to ensure Doherty behavior simultaneously in both frequency bands.

The different possible dual-band implementations for each passive structure are presented in this section. As it will be pointed out, the dual-band DPA designer has to be careful when combining the different dual-band structures used to realize the DPA since some of these structures are incompatible.

A. Impedance Transformer Network

The Impedance Transformer Network is used to transform the output load (50Ω) to the required resistance value at the DPA common node (C.N.) as shown in Fig. 1. In [31], it is shown that a transformer with two sections can achieve ideal impedance matching at two arbitrary frequencies.

![Impedance Transformer Network](image)

**Figure 2.** Dual-Band impedance transformer network. The load $R_L$ is transformed to a resistance $R_L'$. The transformer scheme, shown in Fig. 2, is represented by two transmission lines with characteristic impedances $Z_1$, $Z_2$ and electrical lengths $\theta_1$, $\theta_2$, respectively. The design equations to transform a resistive load $R_0$ to a different resistive load $R_L'$, at two simultaneous frequencies $f_1$ and $f_2$ are presented in [31].

B. Impedance Inverter Network

The IIN must function as a quarter wave transmission line, at the two frequency bands, independently of the termination impedance. However, the dual section transformer discussed
above cannot be used because it behaves as a quarter wave impedance transformer only for fixed value of the load $R_L$. An example is given to support this statement.

Assuming $R_0 = 25\,\Omega$ and $R_L = 100\,\Omega$, and the two operating frequencies $f_1 = 1.8\,\text{GHz}$ and $f_2 = 2.4\,\text{GHz}$, then this results in transmission lines having $Z_1 = 69.3\,\Omega$, $Z_2 = 36.1\,\Omega$ and $\theta_1 = \theta_2 = 68.3^\circ$. Moreover, assuming that the input impedance $R_0$ is now doubled to $50\,\Omega$ (for example as happen at the common node C.N. in Fig. 1), the load at the other point (e.g. at the Main output) becomes complex at the two frequencies, as depicted in Fig. 3. Consequently, the examined structure cannot realize a proper dual-band IID for the Main device output, while its use as dual-band ITN at the DPA output remains valid.

![Figure 3. Simulated input impedance $R_L$ of the dual-band impedance transformer shown in Fig. 2.](image)

To realize a dual band IID, for a correct load modulation in the DPA architecture, different structures are required. In [32], it is shown that an equivalent quarter-wave length transmission line of characteristic impedance $Z_0$, at two incommensurately frequencies $f_1$ and $f_2$, can be realized by using a T- or a Π-network, as shown in Fig. 4.

![Figure 4. Dual-Band impedance inverter network: a) T-network; b) Π-network.](image)

The design equations for both T-network and Π-network are given in [32] as function of the operating frequencies, $f_1$ and $f_2$, and of the equivalent characteristic impedance $Z_0$. Moreover, due to the periodical behavior of these structures, the solution depends also by two integers, $n$ and $m$ [33], that should be selected for physical constraints, i.e. realizability and dimension of the resulting transmission lines. Finally, the phase response of the IID may be different at the operating frequencies, depending on the selected topology and value of $n$ [25], [33]. As a consequence, to ensure proper Doherty operation, the phase shift introduced at the two frequencies by the IID has to be compensated by suitable IPS-PCN structure.

C. Input Power Splitter

To compensate for the different turn-on behavior of the main and auxiliary amplifiers, the input power should be split unevenly [13], [18]. Consequently, a wideband or dual-band uneven power splitter is required. The Wilkinson divider [34] and the Branch-Line Coupler (BLC) [33] are the most used power dividers to equally or unequally divide the input power. The main difference between the two dividers is the phase relationship between the output ports. The Wilkinson divides the output power in phase while the BLC introduces a $90^\circ$ phase shift. In principle, to create a dual-band divider [35], [32], it is sufficient to replace each quarter-wave transmission line with the equivalent dual-band T- or Π-network shown in Fig. 4.

Usually the dual-band approaches for the IPS design are narrow-band solutions, whose matching and coupling factors are strictly frequency dependent. To reduce the design sensitivity related to practical frequency shifts occurring in the realization of the other passive networks, a wide-band topology for the IPS is preferred because it ensures satisfactory matching condition in the vicinity of the selected operating frequencies. However, the separation between the operating bands can create a limitation for using a wideband topology since it is challenging to design such splitter for band separation greater than one-octave. In the latter case, a dual-band BLC should be adopted to overcome this limitation.

D. Phase Compensation Network

To ensure in-phase addition of the output signals from the Main and Auxiliary amplifiers at the common node (C.N.), the phase response introduced by the output IID has to be properly compensated for in the Auxiliary branch. Such a compensation must be performed accounting for the phase response of the input power splitter. In fact, if such IPS is realized through a BLC, then the phase compensation is directly integrated in this element, providing the correct output port connections. Conversely, if Wilkinson structure is adopted, then a suitable PCN is required at the input of the Auxiliary or Main amplifiers. In these cases, the required PCN network can be realized by using one of the dual-band structures presented in Section II-A.

E. Dual-Band DPA Topologies

In this section, the possible configurations to implement a dual-band DPA will be enumerated. The configuration that most closely resembles the general topology shown in Fig. 1, is certainly the one that requires the presence of a dual-band Wilkinson input divider, two dual-band quarter-wave transmission lines to realize the IID and the PCN, and a two-section transformer to realize the ITN.

However, in this case the overall structure of the DPA is very cumbersome, due to the simultaneous presence of a dual-band Wilkinson divider and two impedance inverters. A more
compact solution can be obtained adopting a Branch-Line splitter, whose phase relation of the outgoing signals avoids the need of the phase shifter at the input of the Auxiliary amplifier. However, the designer must pay attention to the structures adopted for the realization of Branch-Line and IIN to allow a proper phase relation between Main and Auxiliary branches. Again, referring to the discussion above, the possible configurations for realizing dual-band DPA are summarized in Table II.

### III. DUAL-BAND DPA DESIGN

The design of a dual-band DPA for 1.8 GHz and 2.4 GHz is presented in this section. These frequencies are arbitrarily chosen and the presented design approach is applicable to any desired combination of two frequency bands. For both Main and Auxiliary amplifiers, a 3.6 mm GaN bare-die device, Cree CGH60015DE [36], has been used. The device has a breakdown voltage of 100 V, a knee voltage of 5 V, a pinch-off voltage of -3.2 V, and a saturation drain current of 2.3 A, approximately. A nonlinear model of the device, supplied by the manufacturer and optimized for Class-AB biasing condition, has been used for the design.

The DPA parameters have been theoretically inferred from the DC-IV curves of the device by applying the design approach in [13]. The values of the design parameters and their symbols are listed in Table III, where "Break" refers to the turn-on of the Auxiliary device, and "Saturation" refers to the saturation of the DPA. It is important to stress that the parameters reported in Table III are numerically computed by the device data mentioned above and not related to the frequency of operation. Moreover, the parameters $R_{MB}$, $R_{MS}$, and $R_{AS}$ refer to the intrinsic current source of the active device [13], while $R_L$ refers to the resistance at the output connection node.

#### A. Matching Networks

The first step to design the dual-band Main PA was to perform load/source-pull simulations to find the optimum load and source impedances fulfilling the intrinsic load conditions (i.e. at the device intrinsic current source), reported in Table III: $R_{MB} = 58 \Omega$ and $R_{MS} = 26 \Omega$, at 1.8 GHz and 2.4 GHz, respectively.

Since the efficiency of the Doherty amplifier at the break condition is equal to that of the Class-AB PA, to further improve the efficiency, harmonic load-pull/source-pull simulations were performed to find the second and third harmonic load impedances of 1.8 GHz and 2.4 GHz. The simulations have shown that the effects of the second harmonic at the input and the third harmonic at the output on the efficiency was very small. Therefore, and in order to decrease the complexity of the matching networks, only the fundamental and the second harmonic have been considered in the design of the output matching network, while only the fundamental frequencies have been considered in the design of the input matching network. The resulting optimum load impedances at fundamental and second harmonic frequencies, at break and saturation conditions, are shown in Fig. 5. The stars represent the purely resistive loading values at the device intrinsic reference plane (i.e. across the device output current source). The empty symbols are the loads identified by load/source-pull simulations, while the filled symbols are the final impedance values synthesized by a distributed approach [37]. Similarly, in Fig. 6 are reported the optimum source impedances at fundamental frequencies at the break and saturation conditions, identified by load/source-pull simulations (stars) and realized by a distributed approach (filled circle), at the two operating
frequencies. In the design of the input matching network, a 56 Ω series resistance in parallel with a 2.4 pF capacitance and a 270 Ω shunt resistance are added in order to ensure the small signal stability of the DPA.

B. Branch-Line Coupler

In this design, due to the fact that the two operating frequencies are separated by 600 MHz only, a wide-band BLC design was adopted instead of a dual band BLC. The design approach adopted is based on the conventional wide-band BLC proposed in [38]. Considering that the proposed BLC in [38] is for equal power division, the characteristic impedances of the transmission lines have been optimized to infer the desired splitting factor given in Table III. For the realization, using the Rogers 5870 substrate with εr = 2.33 and thickness of 0.8 mm, the resulting element parameters are summarized in Table IV, while the photo of the realized BLC is shown in Fig. 7.

![Figure 6. Simulated optimum source impedances of the main device at the transistor input reference plane.](image)

![Figure 7. Photograph of the realized wide-band Branch Line Coupler.](image)

![Figure 8. Simulated and measured S11 and S41 of the Branch Line Coupler.](image)

![Figure 9. Simulated and measured S21 and S31 of the Branch Line Coupler.](image)

Figs. 8 and 9 show the simulated and measured S-parameters of the manufactured BLC. As it can be noted, the measured return loss and isolation are better than 24 dB and 25 dB at 1.8 GHz and 2.4 GHz, respectively. The magnitude of the measured insertion loss are S21 = -3.5 dB and S31 = -2.8 dB at 1.8 GHz and 2.4 GHz. These measurements satisfy the required splitting factor, reported in Table III, where 45 % (−3.5 dB) of the input power must go to the Main amplifier, while 55 % (−2.8 dB) goes to the Auxiliary.

Fig. 10 reports measured and simulated phase response of the fabricated coupler. The phase differences between the output ports are −90.1° at 1.8 GHz and −90.2° at 2.4 GHz.

C. Impedance transformation and inverting networks

As shown in Table III, an ITN that transforms the standard 50 Ω termination load to RL = 13 Ω at 1.8 GHz and 2.4 GHz is required. Therefore, the two section dual-band impedance transformer discussed in Sec. II-B is adopted.

Conversely, for the IIN, the selected structure should introduce the same phase-shift imposed by the BLC at the two operating frequencies. Moreover, referring to Table III, the IIN

### Table IV

<table>
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<th>TL</th>
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<th>Physical parameter</th>
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</tr>
<tr>
<td>TL2</td>
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<td>83</td>
</tr>
<tr>
<td>TL3</td>
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</table>

Consequently, two sections dual-band dual-section impedance transformers are used for the realization. The measured and simulated scattering parameters are shown in Figs. 8 and 9.

![Figure 10. Measured and simulated phase response of the fabricated coupler.](image)
The designed BLC has $-90^\circ$ phase-shift at both operating frequencies (Fig. 10).

Fig. 11 shows the simulation results of the designed ITN and IIN. As can be noted, the ITN performs the impedance transformation from 50 $\Omega$ to a resistive value $R_L \approx 13$ $\Omega$ at $f_1 = 1.8$ GHz and $f_2 = 2.4$ GHz, while having a negligible imaginary part.

Similarly, the IIN realizes the required impedance transformation. In fact, for $R_L = 13$ $\Omega$ the transformed impedance is $Z_M \approx 52$ $\Omega$ (required 58 $\Omega$) at both frequencies, with a negligible imaginary part. When $R_L = 26$ $\Omega$, the transformed impedance becomes $Z_M \approx 26$ $\Omega$ (as required) with negligible imaginary part, at both frequencies again. The resulting element parameters of the IIN and ITN networks are summarized in Table V.

### IV. DUAL-BAND DPA IMPLEMENTATION

The same structure adopted for the Main amplifier was replicated for the Auxiliary, and connected through the BCL and ITN at the input and output, respectively. The resulting circuit diagram of the complete designed dual-band DPA is shown in Fig. 12.

The space between the transistor and the PCB lines is reduced as much as possible by careful alignment to avoid undesirable parasitics that will reduce the bandwidth. Two inductances $L_{bwg}$ and $L_{bwd}$ are used to model the input and output bond-wire inductances, respectively, whose values were estimated to be 0.15 nH each.

A dual-band design approach has been adopted in the design of the matching networks. The impedance buffer methodology, already proposed in [37], has been used for the matching of harmonics. Such an approach allows arbitrary reactive loads to be synthesized for an unlimited number of arbitrary frequencies.

The output matching network consists of two subnetworks, used to control the second harmonics loading conditions (the distributed network surrounded by the dashed rectangle in Fig. 12) and the two fundamental impedances (solid rectangle). For the harmonics, the parallel $\lambda/4@f_2$ short-circuited stub at the output provides a short circuit at $2f_2$ at the connecting point A, while the parallel $\lambda/8@f_1$ open-circuited stub provides a short circuit at $2f_1$ at the connecting point B. This way, the optimization of fundamental and second harmonic impedances can be performed independently. The widths and lengths of $TL_1$ and $TL_2$ are used for realize the required second harmonic impedances of $f_1$ and $f_2$ at the output. Taking into account the effect of the network controlling the harmonics, a dual-band ad-hoc matching network, (dashed box in Fig. 12), has been designed and optimized to provide the matching at the two fundamental frequencies $f_1$ and $f_2$.

The input matching network consists of the stabilizing network (dashed box) and the distributed network surrounded by the solid rectangle designed to provide the input matching simultaneously at the two fundamental frequencies $f_1$ and $f_2$.

In order to study the impact of components variability and uncertainty on the DPA performance, Monte-Carlo simulations have been performed. In these simulations, the uncertainties introduced by the manufacturing process, the lumped components, and $+/-100$ mV DC bias points of the Main and Auxiliary devices have been considered. As shown in Fig. 13, the design is robust and not very sensitive to these deviations. The variations of the PAE and gain are less than 5% and 0.5 dB, respectively.

The PA was implemented on a Rogers 5870 substrate with $\varepsilon_r = 2.33$ and thickness of 0.8 mm. Its size is $30 \times 10 \text{ cm}^2$. A photo of the manufactured dual-band DPA, using bare-die GaN-HEMT CGH60015DE devices, is shown in Fig. 14.

### Table V

<table>
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<th>Element Values of the IIN and ITN</th>
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<td>$Z_1$ ($\Omega$)</td>
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V. MEASUREMENT RESULTS

The DPA has been characterized by small-signal, large-signal, and modulated measurements to evaluate its performance.

A. Small-Signal Measurements

The realized dual band DPA was characterized in small signal conditions (S-parameters) to check its frequency behavior. A drain bias of $V_{DD} = 28\, V$ was used for both devices. The main amplifier was biased for a quiescent drain current of 150 mA (gate voltage of $-3.0\, V$) while the auxiliary amplifier was biased below pinch-off (gate voltage of $-5.5\, V$). The measured and simulated S-parameters are reported in Fig. 15, showing a very good agreement. The input match is better than 10 dB between 1.8 GHz and 2.4 GHz due to the wideband BLC at the input. Moreover, the measurement shows the correct behavior of the DPA in the vicinity of 1.8 GHz and 2.4 GHz, with roughly 14 dB of small signal gain ($S_{21}$).
B. Large-Signal Measurements

Large-signal continuous wave (CW) measurements have been performed in order to evaluate the dual-band DPA under steady-state conditions. In this measurement, the same biasing, as for the S-parameters measurement, is used. Under these conditions, about 27 dBm of input power was required to turn on the Auxiliary device.

The DPA was first characterized versus frequency between 1.6 GHz and 2.6 GHz to study its frequency response under large-signal conditions. Fig. 16 shows simulated and measured drain efficiency and output power versus frequency of the dual-band DPA under a constant input power of 33 dBm, corresponding to saturated operation.

From Fig. 16, it can be noted that the frequency response of the DPA is well predicted by simulations. The measured output power is slightly higher than 43 dBm in the two bands, with a measured drain efficiency of 69% at 1.8 GHz and 61% at 2.4 GHz. The drain efficiency is maintained higher than 55% in 100 MHz bandwidth around the 1.8 GHz-band.

Fig. 17 shows measured power gain and PAE versus output power at 1.8 GHz and 2.4 GHz, respectively. It can be easily noticed that a Doherty region resulting in high, almost constant, efficiency across OBO range of 6 dB is observed.

For the 1.8 GHz band, the measured PAE is 64% at an output power of 43 dBm, and 60% at an output power of 37 dBm (6 dB OBO). Similarly, for the 2.4 GHz band, a 54% of PAE is measured at 43 dBm output power, and 44% at 6 dB OBO. The gain compression in the Doherty region is limited to 1 dB for 1.8 GHz and 1.2 dB for 2.4 GHz.

C. Modulated Measurements

Linearized modulated measurements have been performed to show that the DPA is linearizable and to evaluate its performance when used with modern wireless communication signals. The linearized modulated measurements were performed using the memory polynomial model with nonlinear order 7 and memory depth 3 [39]. The DPA has been tested first in non-concurrent mode using one modulated signal at the time. The signals used are 5 MHz WCDMA, 10 MHz LTE signals both with 7 dB Peak-to-Average-Ratio (PAR), and WiMAX signal with 8.5 dB PAR.

Then the DPA has been tested in concurrent mode where two modulated signals are applied at the input of the DPA at the same time. The linearization was performed with the 2-D-DPD technique presented in [27]. In the first experiment, the WCDMA and the LTE signals were applied at 1.8 GHz and 2.4 GHz bands respectively. In the second experiment the LTE signal is applied at 1.8 GHz band while the WiMAX signal is applied at the 2.4 GHz band. The measured output spectrum at 1.8 GHz and 2.4 GHz (second experiment), before and after DPD, for an average input power of 22 dBm, are shown in Fig. 18 and Fig. 19, respectively.

Average output power, PAE, and ACLR, with and without DPD of all experiments, at the two operating bands, are summarized in Table VI. As expected, we notice that in concurrent mode the average PAE is degraded by 10-20% compared to
the case where the PA is driven by one modulated signal at the time. Yet, these results show that standard DPD methods can be used to linearize the DPA in non-concurrent and concurrent modes to meet modern wireless communication system standards.

VI. CONCLUSIONS

In this paper, an extensive design procedure for highly efficient dual-band DPA has been presented. In particular, the procedure concentrates on the design of the passive structures, presenting several possible topologies for the dual-band DPA. Moreover, the procedure uses a load/source-pull methodology combined with second harmonic tuning to maximize the efficiency performance.

The proposed design procedure has been demonstrated by implementing a hybrid GaN-HEMT dual-band DPA. The success of the presented method was verified by experimental results that show, at 1.8 GHz, a PAE between 60% and 64% in a 6 dB of OBO for CW measurement. At 2.4 GHz and for the same OBO, a PAE between 44% and 54% was recorded. The measured saturated output power exceeds 43 dBm in both bands. Moreover, linearized concurrent modulated measurements using 5 MHz WCDMA and 10 MHz LTE and WiMAX signals demonstrate that the DPA achieves high average efficiency in both bands and is easily linearizable to meet wireless communication system standards.

The excellent performances obtained demonstrate the advantage and potential of the proposed approach for the design of dual-band DPA for future wireless systems, combining multi-band, high efficiency, and linearity design techniques.

ACKNOWLEDGEMENT

The authors would like to thank H. Cao, department of Microtechnology and Nanoscience, Chalmers University of Technology, Gothenburg, Sweden and J. Moon, department of Electrical Engineering, Pohang University of Science and Technology (POSTECH), Pohang, Korea, for their technical support during measurements.

REFERENCES

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